



US005487040A

United States Patent [19]

[11] Patent Number: **5,487,040**

Sukegawa et al.

[45] Date of Patent: **Jan. 23, 1996**

[54] **SEMICONDUCTOR MEMORY DEVICE AND DEFECTIVE MEMORY CELL REPAIR CIRCUIT**

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[57] ABSTRACT

To provide a type of semiconductor memory device characterized by the fact that the area occupied by the redundant memory address decoder on the chip is minimized without reducing the redundancy of the defective memory, and hence the cost of the semiconductor memory device can be cut.

[21] Appl. No.: **90,848**

[22] Filed: **Jul. 12, 1993**

[30] Foreign Application Priority Data

Jul. 10, 1992 [JP] Japan 4-207332

[51] Int. Cl.⁶ **G11C 13/00**

[52] U.S. Cl. **365/200; 365/230.03; 365/225.7; 365/230.06; 395/182.05**

[58] Field of Search **365/200, 230.03, 365/210, 233, 225.7, 230.06; 371/10.1, 10.2, 10.3**

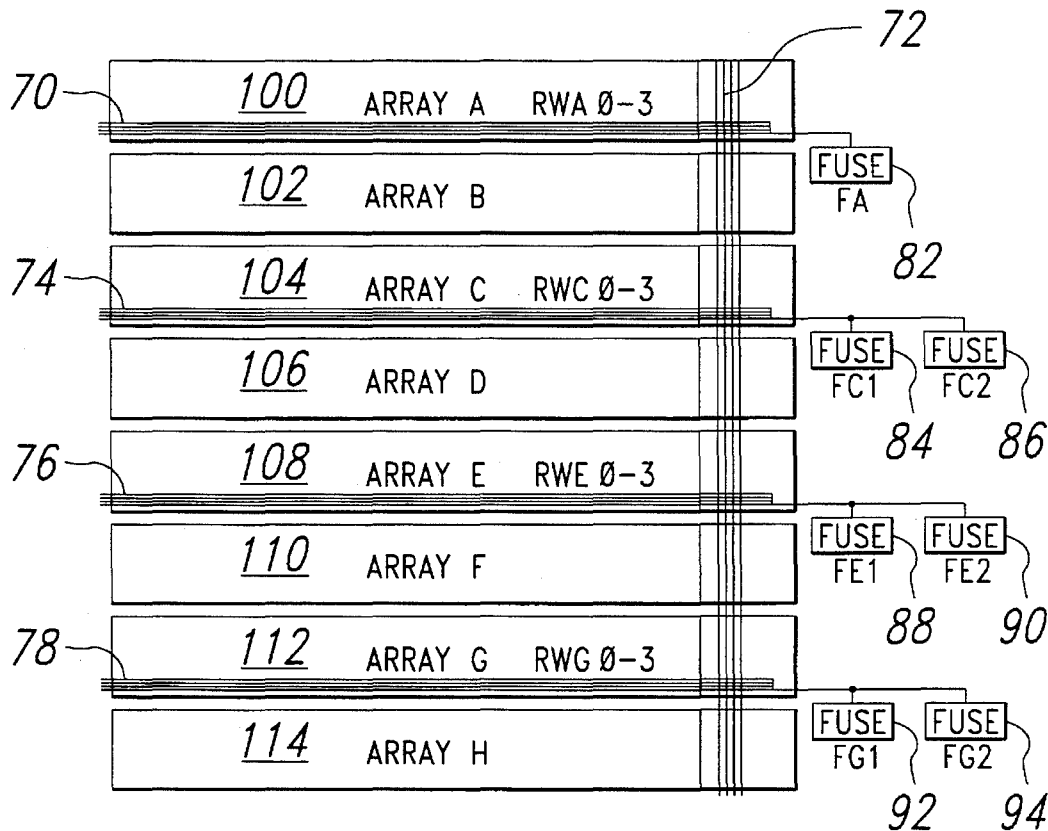
It has both redundant decoders that select the redundant memory in response to the all address bits and the redundant decoders which select the redundant memory group in response to a portion of the address bits, so as to increase the efficiency in saving the defective memory.

[56] References Cited

U.S. PATENT DOCUMENTS

5,272,672 12/1993 Oghara 365/200

6 Claims, 9 Drawing Sheets



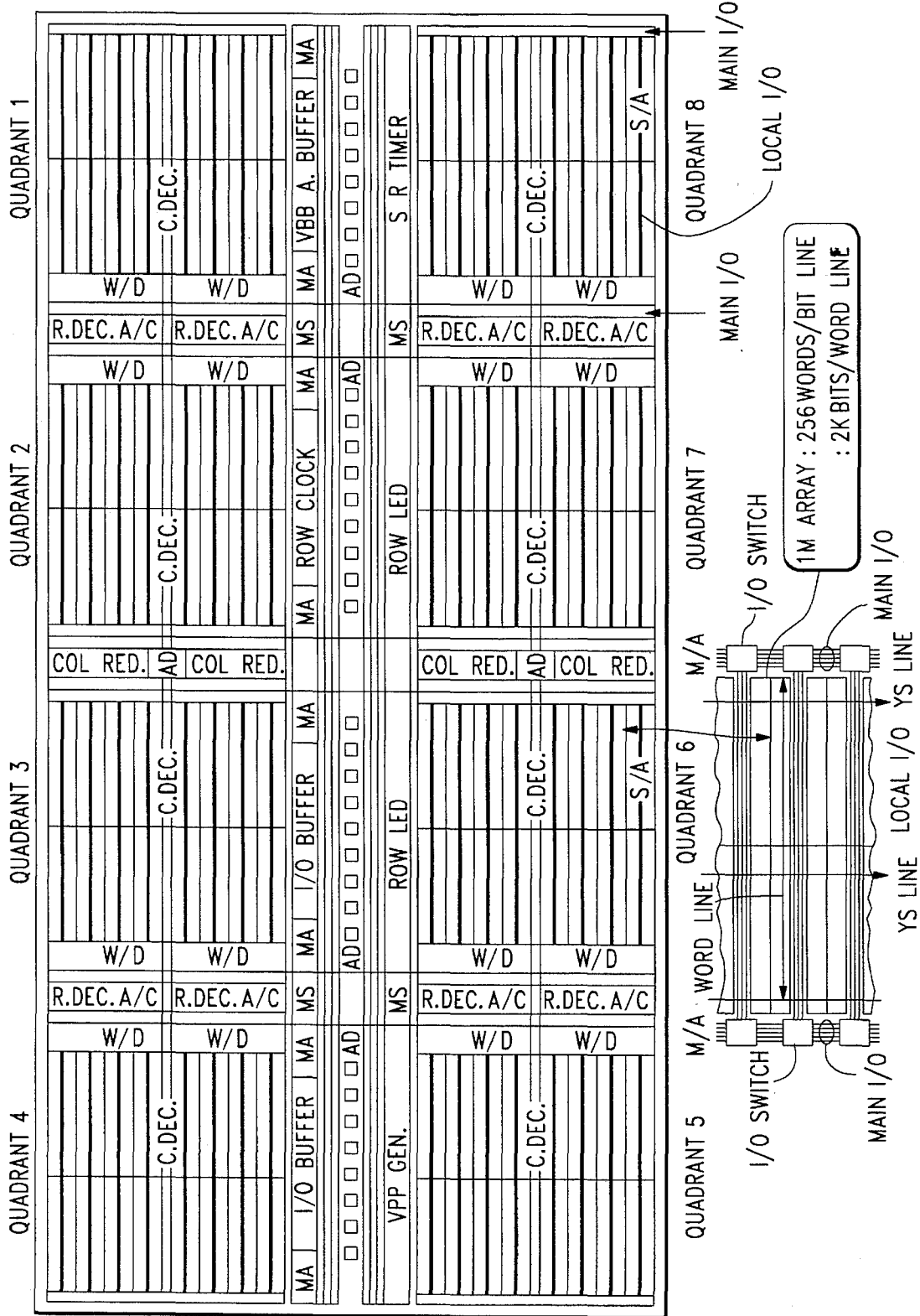


Fig. 1

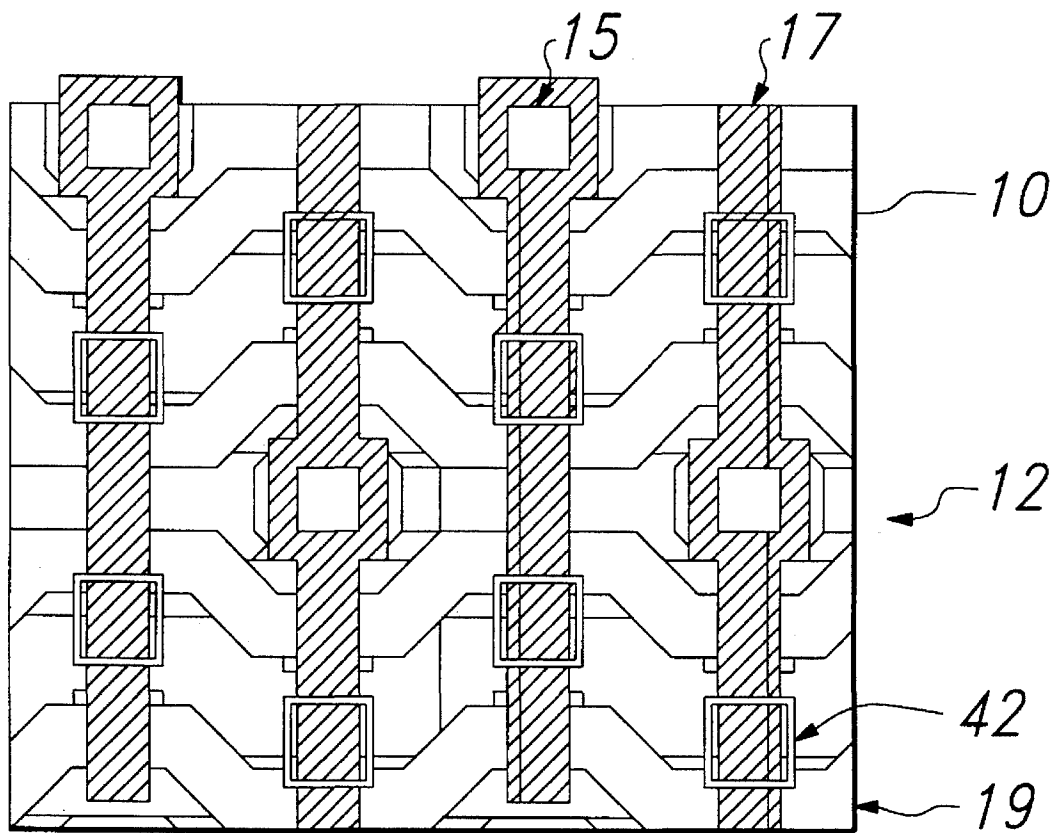
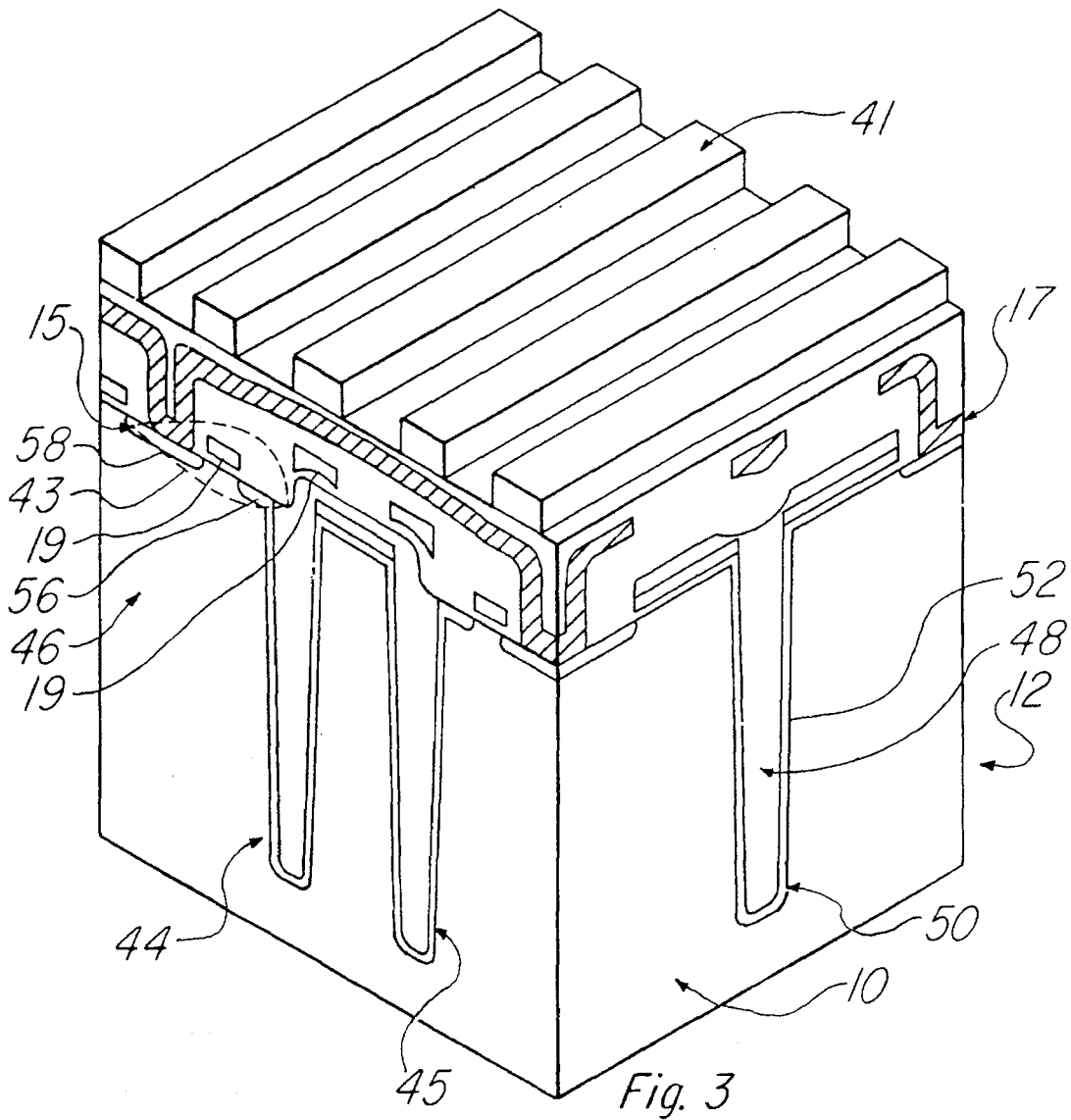


Fig. 2



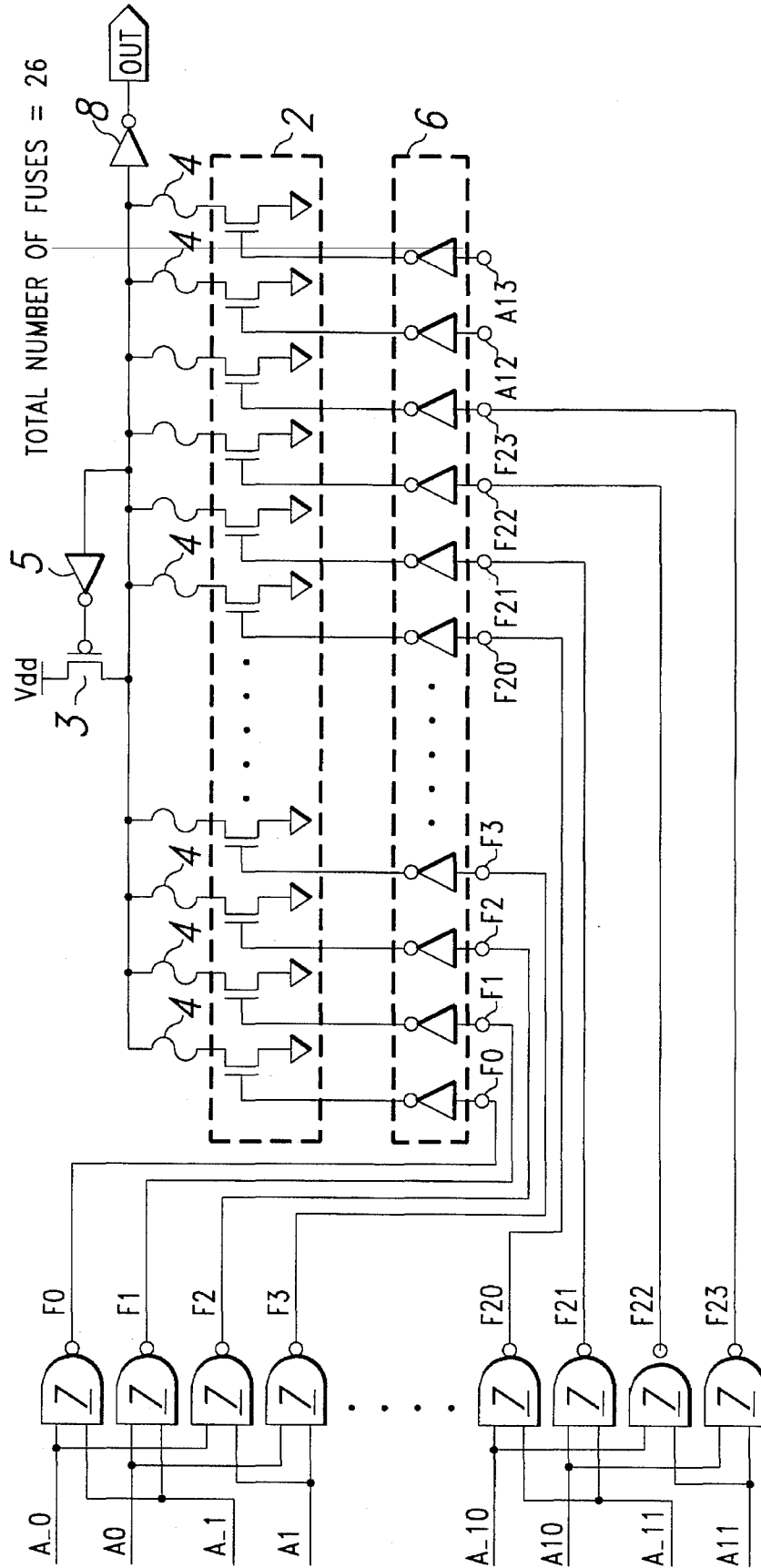


Fig. 4

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