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Lee et al.

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[54] MEMORY DEVICES HAVING A FLEXIBLE REDUNDANT BLOCK ARCHITECTURE

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[30] Foreign Application Priority Data

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[51] Int. Cl.⁶ G11C 7/00; G11C 8/00

[52] U.S. Cl. 365/200; 365/230.03; 365/189.08; 365/225.7

[58] Field of Search 365/200, 230.02, 365/230.03, 189.02, 189.08, 225.7

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Primary Examiner—David C. Nelms

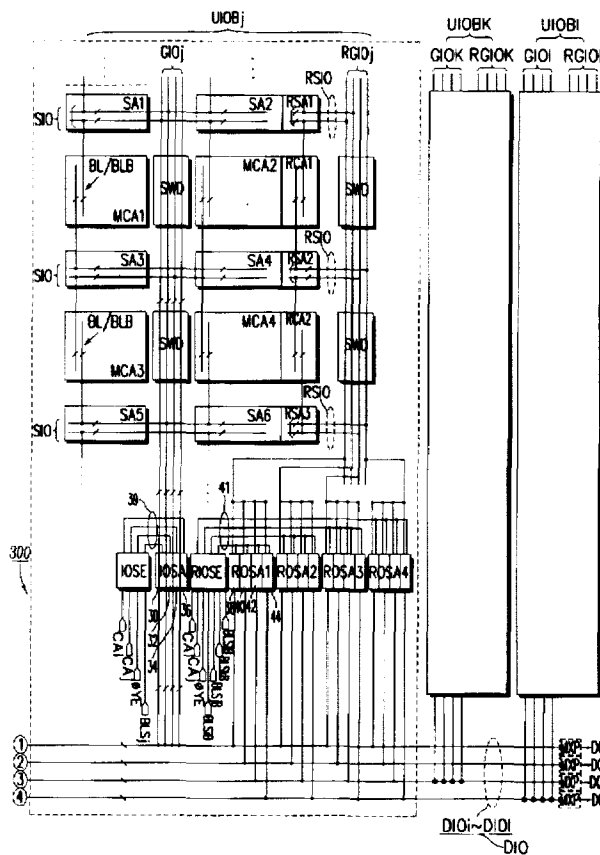
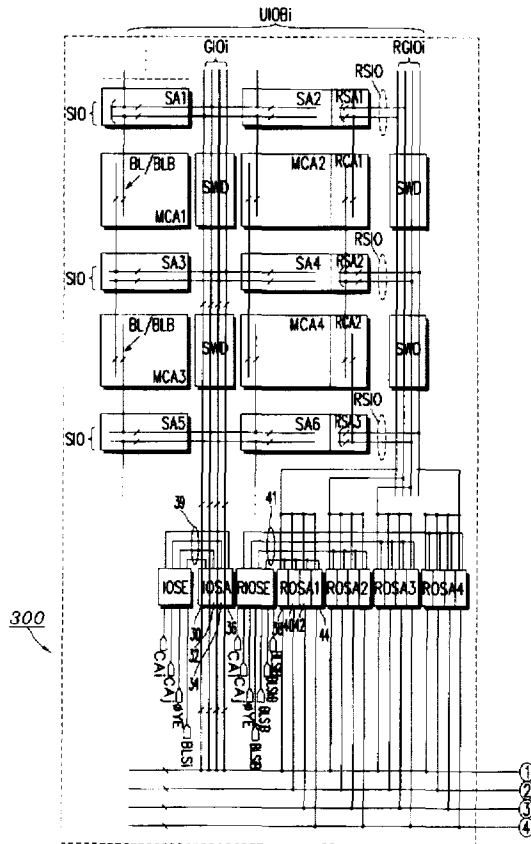
Assistant Examiner—Trong Phan

Attorney, Agent, or Firm—Myers Bigel Sibley & Sajovec

[57] ABSTRACT

A memory device includes a plurality of data input/output (I/O) lines and means for receiving a column address. The memory device also includes a plurality of primary memory cells, a selected primary memory cell of the plurality of primary memory cells being connected to a primary global I/O line in response to receipt of one column address, and a plurality of redundant memory cells, a selected redundant memory cell of the plurality of redundant memory cells being connected to a redundant global I/O line in response to receipt of the one column address. One of the primary global I/O line and the redundant global I/O line are selectively connected to one of the plurality of data I/O lines such that one of the selected primary memory cell and the selected redundant memory cell is connected to the one data I/O line to thereby enable data transfer therebetween, preferably by enabling one of a primary I/O sense amplifier and a redundant I/O sense amplifier connected to the primary and redundant global I/O lines, respectively.

12 Claims, 7 Drawing Sheets



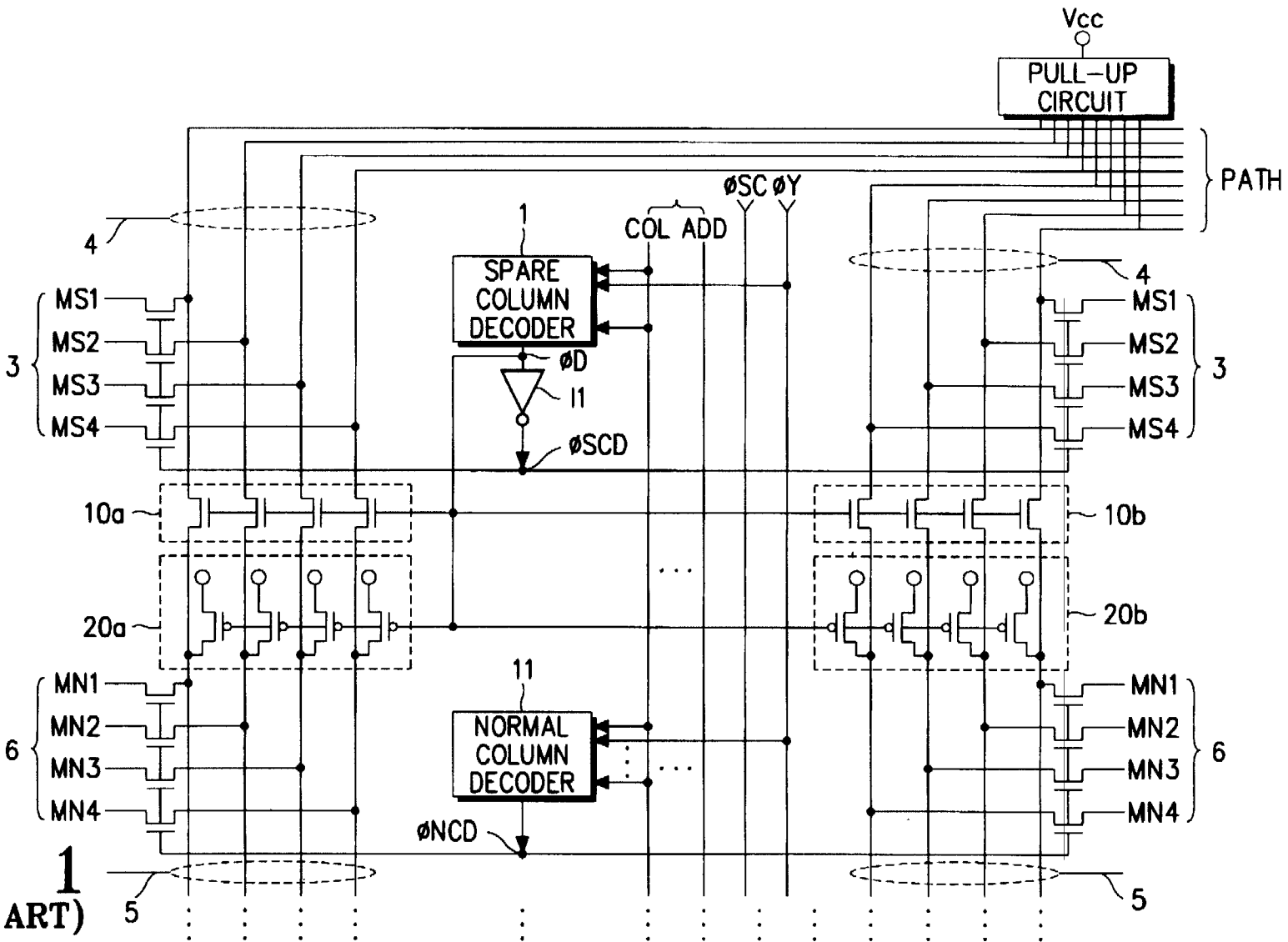


FIG. 1
(PRIOR ART)

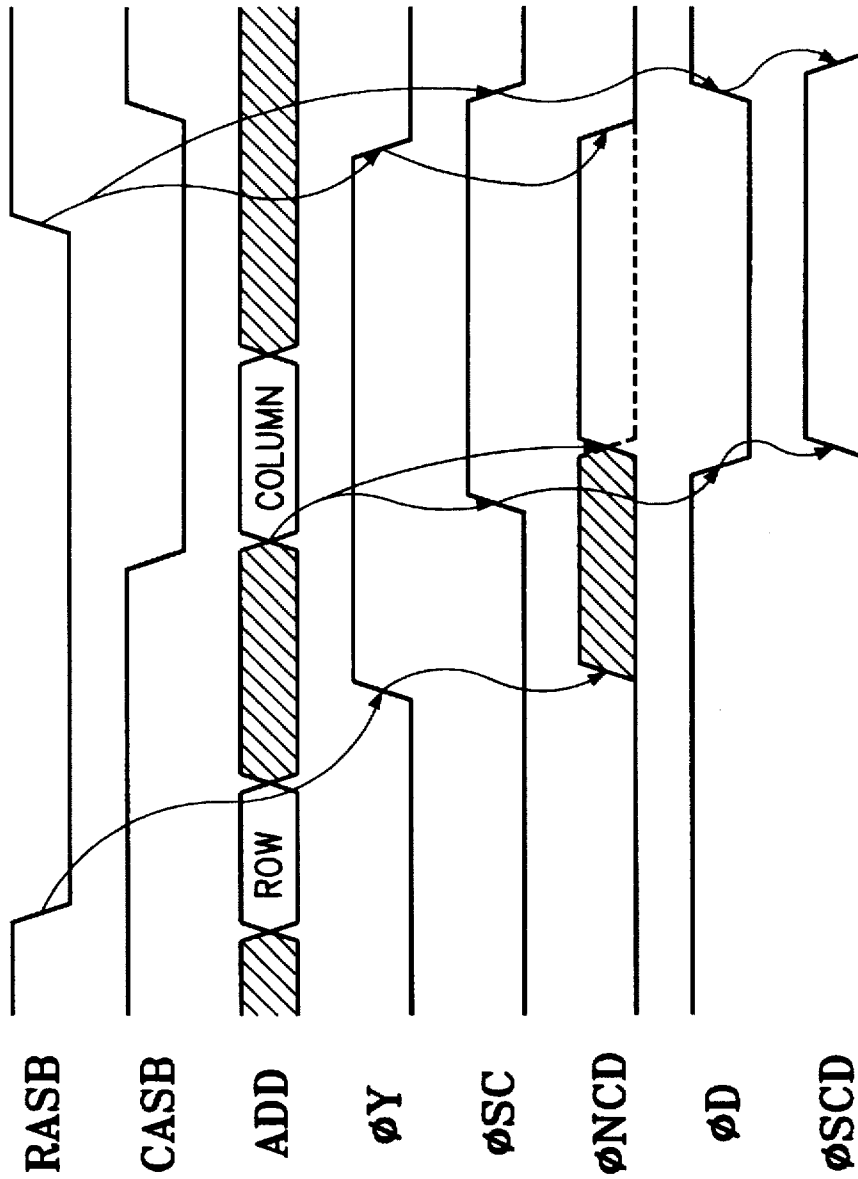


FIG. 2
(PRIOR ART)

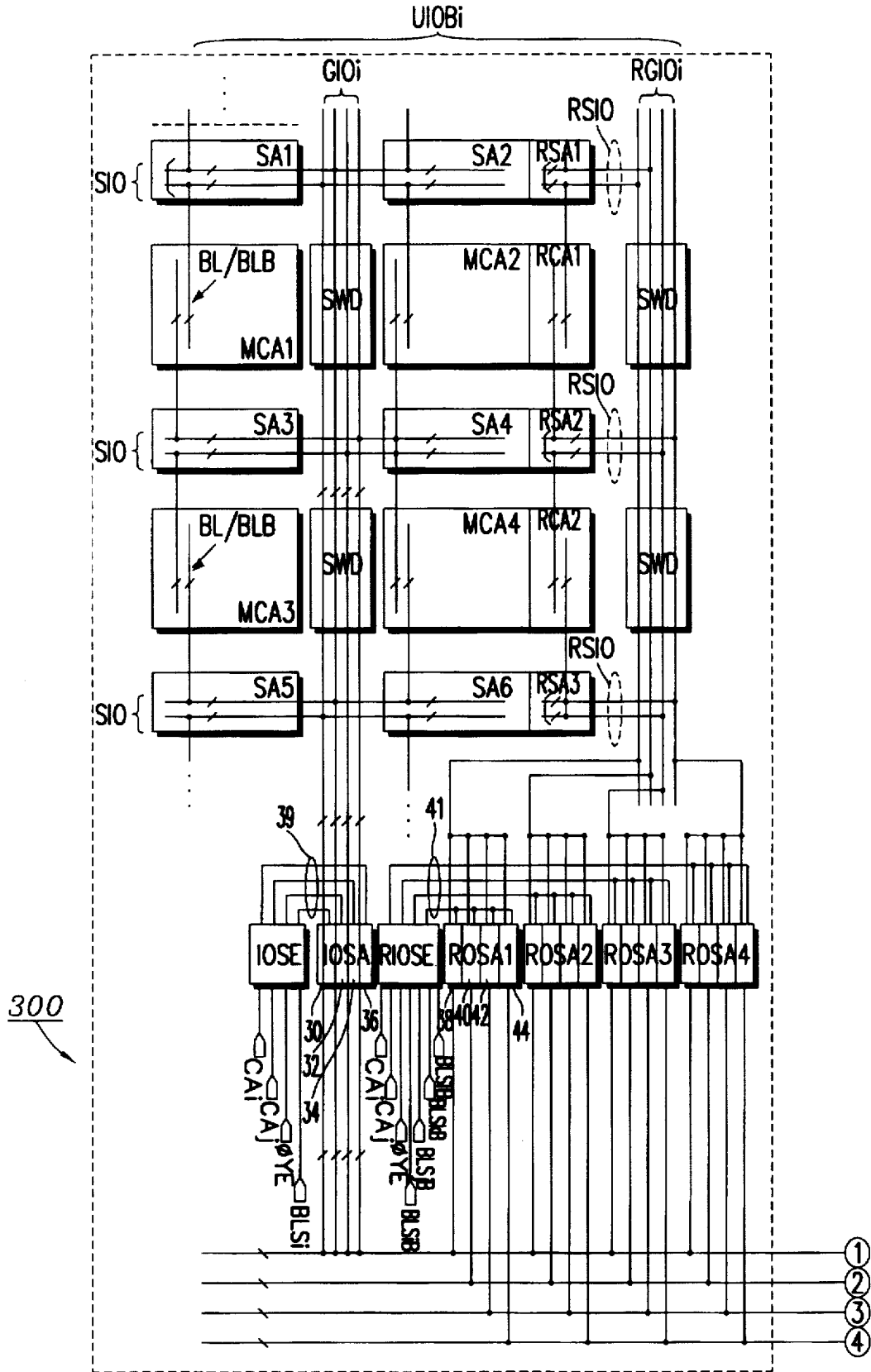
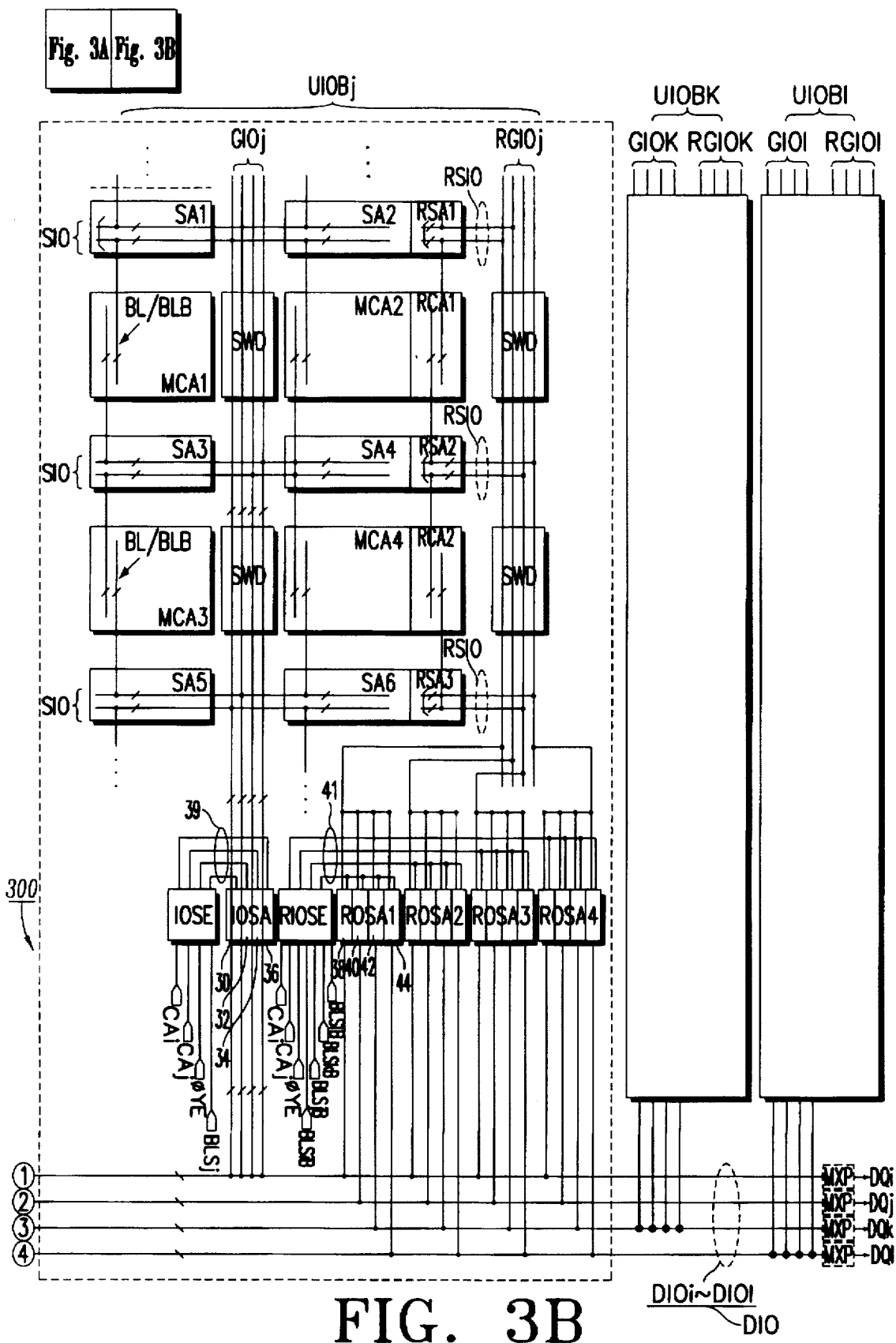


FIG. 3A



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