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(12) **United States Patent**  
**Hidaka**

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(54) **SEMICONDUCTOR MEMORY DEVICE WITH IMPROVED FLEXIBLE REDUNDANCY SCHEME**

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\* cited by examiner

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(\* ) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Oct. 15, 1998 (JP) ..... 10-293421

(51) **Int. Cl.<sup>7</sup>** ..... **G11C 7/00**

(52) **U.S. Cl.** ..... **365/200; 365/230.03; 365/190; 365/225.7**

(58) **Field of Search** ..... 365/200, 230.03, 365/190, 208, 225.7

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(57) **ABSTRACT**

A spare memory array having spare memory cells common to a plurality of normal sub-arrays having a plurality of normal memory cells is provided. A spare line in the spare array can replace a defective line in the plurality of normal sub-arrays. The defective line is efficiently repaired by replacement in an array divided into blocks or sub-arrays.

**7 Claims, 31 Drawing Sheets**

X0	NORMAL MEMORY SUB-ARRAY	MA#0	} RBX#0
SPDX	SPARE ARRAY	SPX#	
X1	NORMAL MEMORY SUB-ARRAY	MA#1 ; RBX#1	} RBX#1
X2	NORMAL MEMORY SUB-ARRAY	MA#2 ; RBX#2	
.	.	.	} RBX#m
.	.	.	
Xm	NORMAL MEMORY SUB-ARRAY	MA#m ; RBX#m	

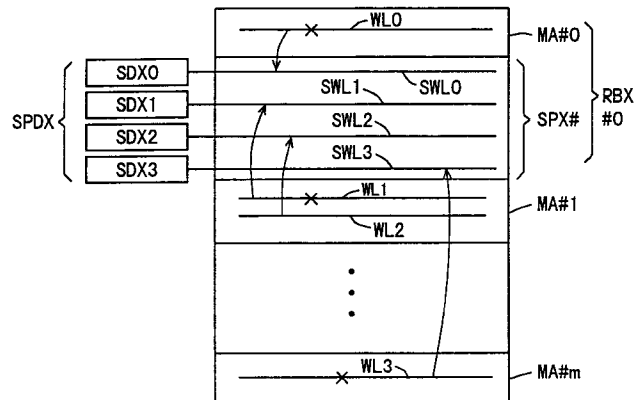
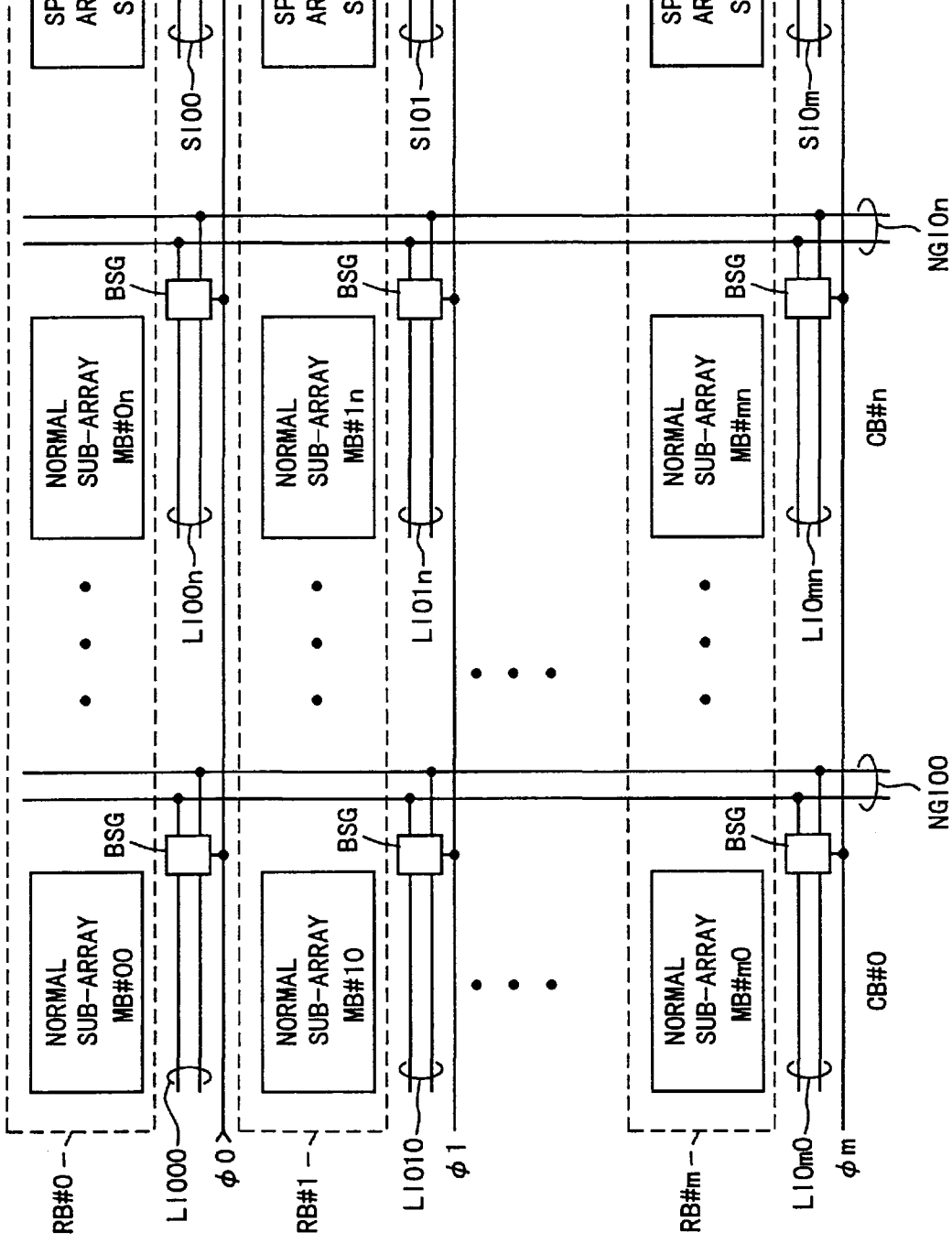


FIG. 1



MICRON-1001.002

FIG. 2A

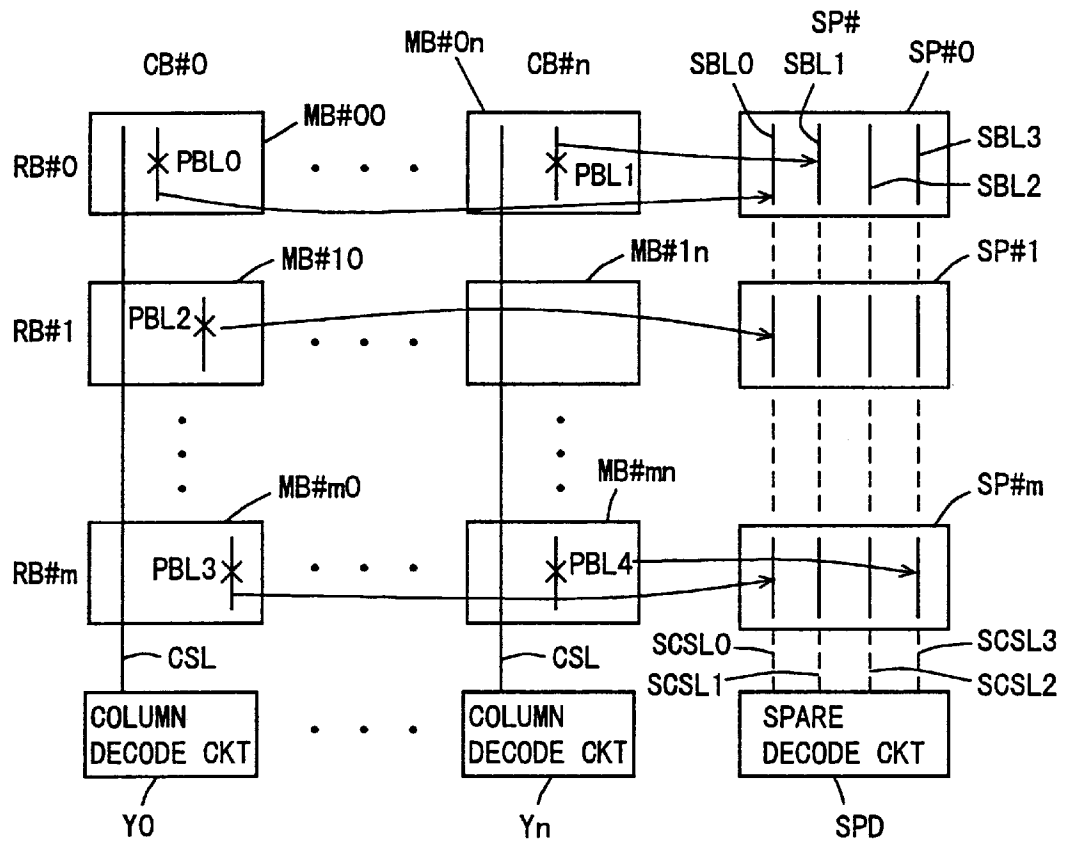


FIG. 2B

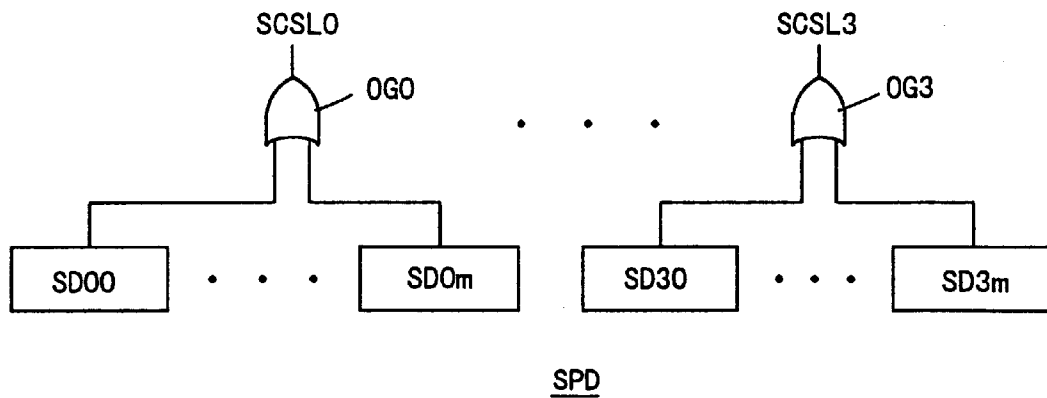


FIG. 3A

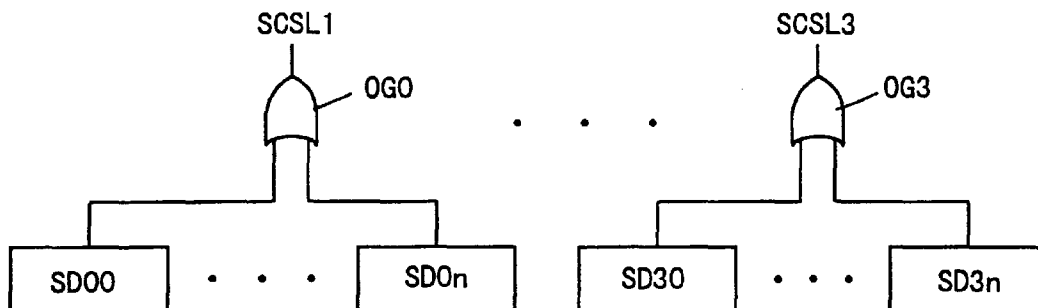


FIG. 3B

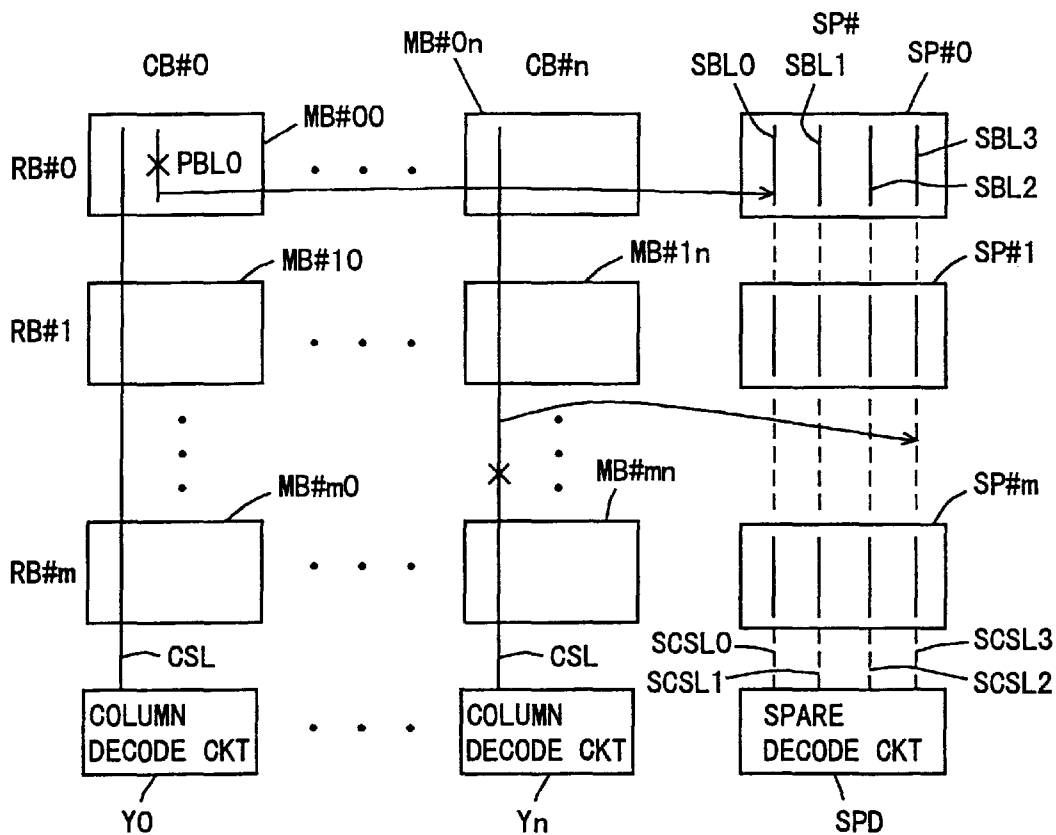


FIG. 4

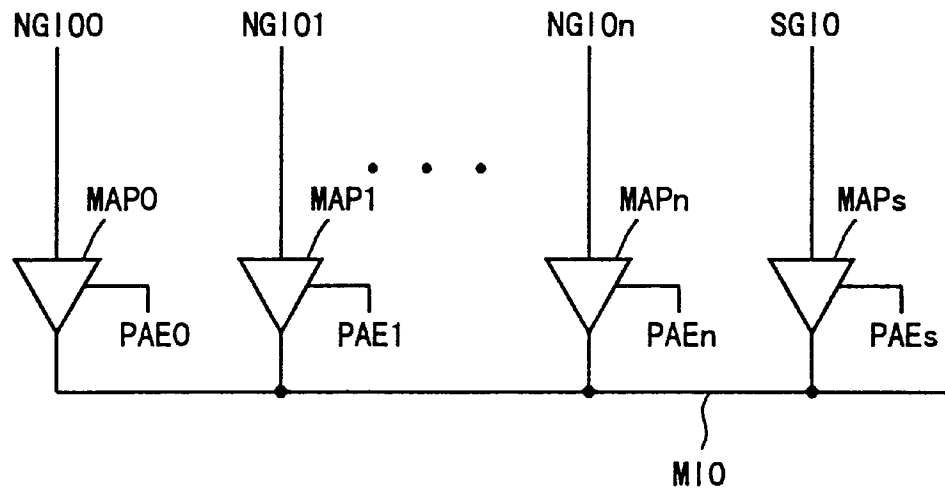
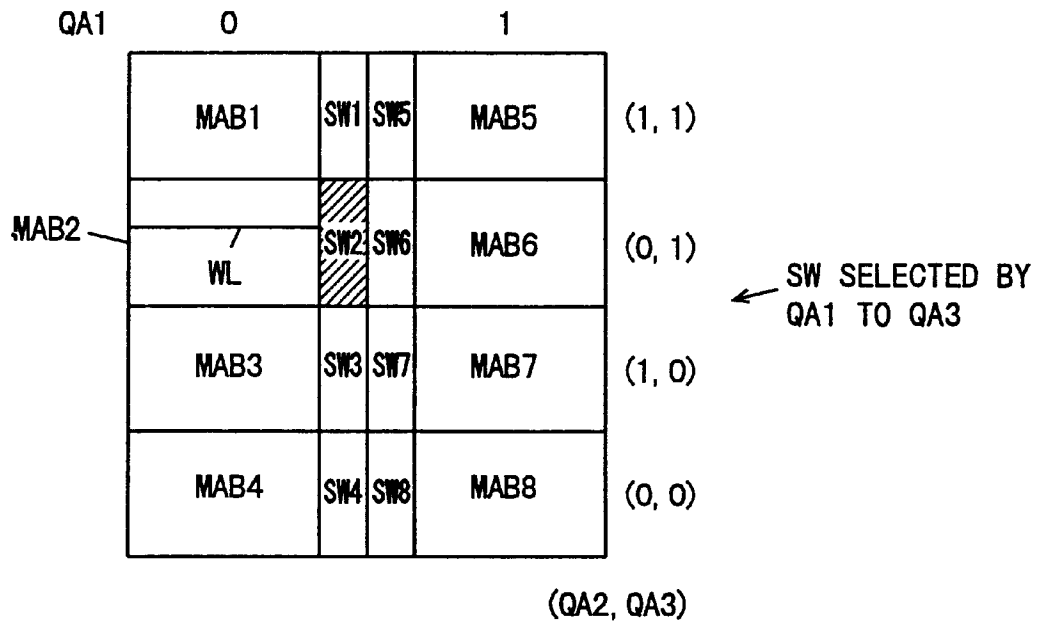


FIG. 24



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