(19) Japan Patent Office (JP)

(12) **Japanese Unexamined Patent Application Publication** (A)

(11) Japanese Unexamined Patent Application Publication Number

H06-52696

(43) Publication date February 25, 1994

(51) Int. Cl.[5]	Identification codes	JPO Internal No.	FI		Theme codes (reference)
G11C 29/00	301 B	6741-5L			
11/401					
		6741-5L	G11C 11/34	371 D	

Request for examination Not Requested Number of claims 6 (Total of 10 pages)

(21) Application number: Japanese Patent Application H04-204765

(22) Date of application: July 31, 1992

(71) Applicant: Identification no. 000003078
Toshiba Corp.
72 Horikawacho, Saiwai-Ku, Kawasaki City, Kanagawa Prefecture, Japan

(72) Inventor: MINAMI Naoaki,
c/o Toshiba Corp., Semiconductor Systems Technology Center, 580-1 Horikawacho, Saiwai-Ku, Kawasaki City, Kanagawa Prefecture, Japan

(72) Inventor: WATANABE Shigeyoshi c/o, Toshiba Corp., Central Research Institute, 1 Komukaitoshibacho, Saiwai-Ku, Kawasaki City, Kanagawa Prefecture, Japan

(74) Agent: SUZUE Takehiko

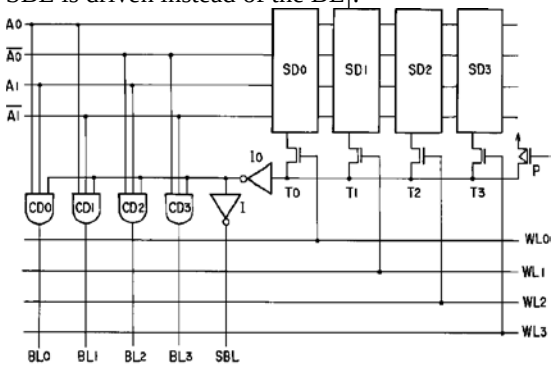
54 TITLE OF THE INVENTION

SEMICONDUCTOR MEMORY DEVICE

57 ABSTRACT

PURPOSE: A contrivance at reducing the chip area and improving the yield by raising rescue efficiency and the success rate of rescue of defective memory cells.

CONSTITUTION: This semiconductor memory device is provided with plural regular memory cells arranged in a matrix, plural regular word lines WL_i connected to regular memory cells, plural regular bit lines BL_j connected to regular memory cells, plural spare memory cells connected to regular word lines WL_i, and a spare bit line SBL connected to the spare memory cells, characterized by when reading/ writing is executed on the normal regular memory cell connected to the regular bit lines BL_j including a defective memory cell, the BL_j is driven, and when reading/writing is executed on the defective regular memory cell connected to the regular bit lines BL_j including a defective memory cell, the spare bit line SBL is driven instead of the BL_j.



Scope of the Patent Claims

Claim 1

A semiconductor memory device equipped with plural regular memory cells arrayed in a matrix, and plural regular word lines connected to these regular memory cells, and plural regular bit lines connected to said regular memory cells, and plural spare memory cells connected to said regular word lines, and spare bit lines connected to these spare memory cells, characterized by the regular bit line being driven when there is the performance of write-in or read-out to/from a normal regular memory cell connected to a regular bit line including a defective memory cell, and a spare bit line being driven to replace the regular bit line when there is the performance of write-in or read-out to/from a defective regular memory cell connected to a regular bit line including a defective memory cell.

Claim 2

The semiconductor memory device claimed in claim 1 characterized by when there are plural defective memory cells, and no two of these are on the same regular word line, then normally the same spare bit line is driven instead of the regular bit line connected to the defective memory cell.

Claim 3

A semiconductor memory device equipped with plural regular memory cells arrayed in a matrix, and plural regular word lines connected to these regular memory cells, and plural regular bit lines connected to said regular memory cells, and plural spare memory cells connected to said regular word lines, and spare word lines connected to these spare memory cells, characterized by the regular word line being driven when there is the performance of write-in or read-out to/from normal regular memory cells connected to a regular word line including a defective memory cell, and a spare word line being driven to replace the regular word line when there is the performance of write-in or read-out to/from a defective regular memory cell connected to a regular word line including a defective memory cell.

Claim 4

The semiconductor memory device claimed in claim 3 characterized by when there are plural defective memory cells, and no two of these are on the same regular bit line, then normally the same spare word line is driven instead of the regular word line connected to the defective memory cell.

Claim 5

A semiconductor memory device equipped with plural regular memory cells arrayed in a matrix, and plural regular word lines connected to these regular memory cells, and plural regular bit lines connected to said regular memory cells, and a first spare memory cell connected to said regular word line, and a spare bit line connected to the first spare memory cell, and a second spare memory cell connected to said regular bit line, and a spare word line connected to the second spare memory cell, characterized by driving the regular bit line and the regular word line connected to a normal regular memory cell when there is the performance of write-in or read-out to/from said normal regular memory cell, and driving a regular word line and a spare bit line connected to a defective memory cell when performing write-in/read-out to/from said defective memory cell.

Claim 6

A semiconductor memory device providing peripheral circuits comprising an m unit configuration of unit circuits connected to one each of k types of circuits, characterized by said peripheral circuits being comprised of a matrix disposing m + n units of the same type of circuit in the line direction, and disposing different k types of circuits in the row direction, and switching circuits which switch over the row direction disposed before/after each circuit, and connecting k types of circuits in the row direction detouring past the defective circuit by means of said switching circuit.

Detailed Description Of The Invention

[0001]

Technical Field Of The Invention

The present invention relates to semiconductor memory devices such as dynamic RAM (DRAM), in particular to semiconductor memory devices providing defect rescue functions of memory cells and peripheral circuits.

[0002]

Prior Art

Plural memory cells are arrayed in a matrix in DRAM memory cells, and the selection of memory cells is performed by means of the selection of the line (word line) and row (bit line). Defective cells generated in memory cell arrays are rescued by means of replacement by spare cells prepared in advance. Conventionally, as this rescue method, the replacement was performed for row or line units and replacement was not performed at the cell unit level. In other words, columns or lines which included even one defective cell were treated as an entirely defective row or line (hereafter, this kind of row and line are called defective rows and defective lines), and a method was used where they were changed out for spare rows (reserve columns) or spare line (reserve lines).

[0003]

Hereafter, the conventional method of performing the rescue of defects at the row unit level is explained. Now, the rescue of defects at the line level was performed in the same manner. In Fig. 12, the redundancy circuit means in order to perform relief of defects at the row unit level in DRAM is represented. Memory cell arrays have four regular bit lines BL_0, BL_1, BL_2, BL_3, and a spare bit line SBL, in addition to comprising four regular word lines WL_0, WL_1, WL_2, WL_3. The regular memory cell selected by means of the word line WL_i and the regular bit line BL_j, and the spare memory cell selected by the spare bit line SBL comprise the SC_i. The row address is input from the address lines A_0,/A_0, A_1,/A_1 (/A is an inverted output), and one of the regular bit lines is selected by means of the column decoders CD_0, CD_1, CD_2 and CD_3 in correspondence with the input address. When there is a defect in a regular bit line, that address is recorded in the spare decoder SD.

[0004]

Because the spare decoder SD is comprised of a MOS transistor and a fuse and the like, the recording of the address of the defective bit line is performed by severing the fuse in correspondence with the address. Then, when the input address correspondence to the defective line address, a current or voltage V_{CC} is output in respect of the inverter I_0, and when there is no correspondence, then 0V is output. When V_{CC} is input, the inverter I_0, outputs 0V to each column decoder to inactivate the regular bit lines, as well as to activate the spare bit line SBL via the inverter I_1, and

when 0V is input, the spare bit lines are inactivated, and the regular bit lines selected by the column decoder are activated.

[0005]

The conventional defect relief methods as explained above have the following problems. Firstly, because containing even one defective cell is treated as an entirely defective row, unnecessary relief is performed in respect of normal cells in the defective row. For example, as illustrated in Fig. 13 (a), when the cell C_{11} is defective, the bit line BL_1 is treated as defective in its entirety, and is changed out for the spare bit line SBL. For that reason, the C_{01}, C_{21} and C_{31} cannot be used, even if they are normal.

[0006]

Moreover, because the spare row is employed for the relief of specific defective cells, depending on the distribution of the defects, as illustrated in Fig. 13 (b), there is a requirement for the same number of spare bits lines as the number of defective cells. In addition, as illustrated in Fig. 13 (c), when there are defective cells even in the spare columns, the rescue of the defects of regular cells is not enabled.

[0007]

On the other hand, in tandem with the densification of the DRAM and the miniaturization of elements, the fluctuation of the threshold of the transistors as a result of the short channel effect or the fluctuation in the distribution of impurities becomes great, and because there is an additional increase in the number of circuits and the number of elements, defects can be expected to be generated not only the memory cells, but also in the peripheral circuits. The peripheral circuits are comprised of sense amp drivers, DQ buffers, sense amp equalizers, column decoders, and spare decoders, and in particular the sense amp drivers, DQ buffers, sense amp equalizers are mutually connected and perform operations in series. Therefore, the defect relief of these circuits is not merely the changing out of the defective circuits for spare circuits, the connections between the circuits must be maintained. For example, in the event that there is a change out of a DQ buffer, the spare DQ buffer employed as the replacement must be connected to the sense amp driver and the sense amp equalizer which was connected to the defective DQ buffer.

[0008]

Fig. 14 represents an embodiment of the redundancy format of the peripheral circuits by means of the conventional methods. One each of a sense amp driver, a DQ buffer and a sense amp equalizer are connected in one circuit unit for use, and Fig. 14 (a) represents the situation where one spare unit is provided. Because the defects of a memory cell are rescued by the rescue of a bit line or a word line unit, and not by cell units in this embodiment, rescue is not performed for sense amp driver units, DQ buffer units or sense amp equalizer units.

[0009]

In this type of conventional redundancy format, as illustrated in Fig. 14 (b), when there is distribution of defects, three units of the circuits connecting one each of the sense amp driver, the DQ buffer and a sense amp equalizer are necessary, increasing the chip area by a large margin.

[0010]

Problems To Be Solved By The Invention

In this manner, in the rescue methods of conventional memory cells, because there is change out with spare cells for the unnecessary relief of normal cells, and a large volume of spare cells are required in respect of all of the defective cells which should be rescued, the rescue efficiency is very poor. Furthermore, because not even one defective cell can be permitted in the spare column, the success rate of relief is also poor. Moreover, even in the relief method of the peripheral circuits, there is change out using spare circuits in respect of peripheral circuits which do not need to be relieved, resulting in poor rescue efficiency.

[0011]

Because the present invention was conceived of in consideration of these facts, the object of the invention is the provision of a semiconductor memory device enabling high rescue efficiency and rescue success rates of defective memory cells and periphery circuits, enabling miniaturization of the surface area of chips and improved yields.

[0012]

Means for Solving the Problem

The core of the present invention is the replacement of defective memory cells or peripheral circuits with spare cells or spare circuits, and not the replacement of normal memory cells or peripheral circuits which do not need to be relieved.

[0013]

In other words, the present invention (Claim 1) is a semiconductor memory device equipped with plural regular memory cells arrayed in a matrix, and plural regular word lines connected to these regular memory cells, and plural regular bit lines connected to said regular memory cells, and plural spare memory cells connected to said regular word lines, and spare bit lines connected to these spare memory cells, characterized by the regular bit line being driven when there is the performance of write-in or read-out to/from a normal regular memory cell connected to a regular bit line including a defective memory cell, and a spare bit line being driven to replace the regular bit line when there is the performance of write-in or read-out to/from a defective regular memory cell connected to a regular bit line including a defective memory cell.

[0014]

Moreover, the present invention (Claim 3) is a semiconductor memory device equipped with plural regular memory cells arrayed in a matrix, and plural regular word lines connected to these regular memory cells, and plural regular bit lines connected to said regular memory cells, and plural spare memory cells connected to said regular word lines, and spare word lines connected to these spare memory cells, characterized by the regular word line being driven when there is the performance of write-in or read-out to/from normal regular memory cells connected to a regular word line including a defective memory cell, and a spare word line being driven to replace the regular word line when there is the performance of write-in or read-out to/from a defective regular memory cell connected to a regular word line including a defective memory cell.

[0015]

Furthermore, the present invention (Claim 5) is a semiconductor memory device equipped with plural regular memory cells arrayed in a matrix, and plural regular word lines connected to these regular memory cells, and plural regular bit lines connected to said regular memory cells, and a first spare memory cell connected to said regular word line, and a spare bit line connected to the first spare memory cell, and a second spare memory cell connected to said regular bit line, and a spare word line connected to the second spare memory cell, characterized by driving the regular bit line and the regular word line connected to a normal regular memory

cell when there is the performance of write-in or read-out to/from said normal regular memory cell, and driving a regular word line and a spare bit line connected to a defective memory cell when performing write-in/read-out to/from said defective memory cell.

[0016]

In addition, the present invention (Claim 6) is a semiconductor memory device providing peripheral circuits comprising an m unit configuration of unit circuits connected to one each of k types of circuits, characterized by said peripheral circuits being comprised of a matrix disposing m + n units of the same type of circuit in the line direction, and disposing different k types of circuits in the row direction, and switching circuits which switch over the row direction disposed bore/after each circuit, and connecting k types of circuits in the row direction detouring past the defective circuit by means of said switching circuit.

[0017]

Effects

By means of the present inventions (Claims 1, 3 and 5), on the occasion of reading-out and writing-in to a normal cell on a regular row (line) including a defective cell, that regular row (line) is activated, and there is no replacement with a spare row (line). Moreover, even if there are defective cells in multiple regular rows (lines), when no two of those defective cells are in the same line (row), one spare row (line) is sufficient for the rescue of the defects of multiple regular rows, by means of replacing with a regular row (line) using a spare row (line) in correspondence with the selected line (row) is enabled.

[0018]

In this manner, because there is no unnecessary replacement by spare cells with respect to normal cells on the defective row (line), the normal cells can be used efficiently. In addition, because the rescue of the defects of multiple regular rows (lines) is enabled with one spare row (line), good efficient rescue using very few spare rows (lines) is enabled. Furthermore, even if there are defective cells in the spare rows (lines) the performance of the rescue of the defects of regular cells is enabled.

[0019]

Moreover, by means of the present invention (Claim 6), when there are k types of circuits A, B, … K, and when there are m + n units each including n units of spares of the same kind of circuit for each, an m unit configured circuit connecting one each of k types of circuits while avoiding n units of defects in each line is enabled.

[0020]

Embodiments

Hereafter the present invention is explained based on the attached figures.

[0021]

Fig. 1 is a circuit configuration diagram representing the redundancy circuit means of DRAM related to the first embodiment of the present invention. In this embodiment, a regular memory cell array comprised of four lines by four rows and one spare row and the circuit for the control thereof are represented.

[0022]

The memory cell array is comprised of memory cells arrayed in a matrix, four regular bit lines BL_J (BL_0, BL_1, BL_2, BL_3) and a spare bit line SBL, in addition to comprising four regular word lines (WL_0, WL_1, WL_2, WL_3). The regular memory cells C_{ij} selected by means of the word line WL_i and the regular bit line BL_j, and the spare memory cell SCi selected by the word line WLi and the spare bit line SBL. The row address is input from the address lines A_0,/A_0, A_1,/A_1 and one of the regular bit lines is selected by means of the column decoders CD_0, CD_1, CD_2 and CD_3 in correspondence with the input address. When there is a defect in a regular bit line, that address is recorded in the spare decoder SD.

[0023]

The spare decoder SD, unlike the conventional device represented in Fig. 12, is set for each word line WL_i. The output of the spare decoders SD_i (SD_1, SD_2, SD_3 and SD_4) is supplied to the inverter I_0 via the NMOS transistors T_i (T_0, T_1, T_2, T_3) input by the word line WL_i to the gate. Moreover, the input terminal of the inverter I_0 is precharged with the power source voltage V_{CC} by means of the PMOS transistor P. For that reason, when the input address corresponds to a defective line address, and when the word line of the defective cell is selected, the power source voltage V_{CC} is output respect to the inverter I_0, and when there is no correspondence then 0V is output. In other words, each spare decoder SD_i records the address of defective regular cells on WL_i.

[0024]

The inverter I_0 not only inactivates the regular bit lines by outputting 0V to each column decoder when V_{CC} is input, but also activates the spare bit line SBL via the inverter I_1. Moreover, when 0V is input, the spare bit line is deactivated, and the regular bit line selected by the column decoder is activated.

[0025]

The specific configuration of the spare decoders is as illustrated in Fig. 2. Each of the NMOS transistors T_{i0},/T_{i0}, T_{i1},/T_{i1} are connected by gates to the address lines A_0,/A_0, A_1,/A_1, and the drain of each transistor and the output node of SD are connected by the fuses F_{i0},/F_{i0}, F_{i1},/F_{i1}. The output node is connected to the input of the invertor I_0, and precharged with the V_{CC} by means of the PMOS transistor P_i. The recording of the address of the defective bit line is performed by means of the severance of the fuse connecting the transistor to the address line whose potential becomes V_{CC} when that bit line is selected.

[0026]

For example, if the C_{11} connected to the bit line BL_1 is defective, because the BL_1 selection to input V_{CC} to the address line A_0 and /A_1, the fuses F_{10} and /F_{11} are switched over. When the input address corresponds to the address of a defective bit line, in addition to when the word line WL_1 of a defective cell is selected, because the output node is not grounded, the inverter I_0 outputs V_{CC}, and because the output node is grounded when the input address does not correspond, the Inverter I_0 outputs 0V.

[0027]

Next, an explanation is provided of the operations of this embodiment. When the word line WL_i is selected, the transistor T_i becomes conductive and there is connection of the output of the spare decoder SD_i and the input of the inverter I_0. When there is a defective cell C_{IJ} on the word line WL_i, and the spare decoder SD_i records the address of the bit line BL_j. When the bit line BL_j is selected, there is no grounding of the input of the inverter I_0 and the output of the spare decoder SD_i, and the potential thereof is maintained at V_{CC}. Therefore in this situation, instead of the regular bit line BL_j, the spare bit line SBL is activated, and read-out and

writing-in is performed to the spare cell SC_i. When the other bit line $BL_{j'}$ ($j \neq j'$) is selected, the output of SD_i and the input of I_0 are grounded, and the potential thereof becomes 0V. Therefore in that situation, the regular bit line BL_j is selected and read out on writing in to C_{ij} is performed.

[0028]

A specific embodiment of the rescue of a defect by means of the method described above is represented in Fig. 3. In this embodiment, there are three defective cells C_{01}, C_{10} and C_{22} in the regular cell array comprised of four lines and four rows. In the conventional method, there was a requirement for three spare bits lines as illustrated in Fig. 13 (b), but if this embodiment is employed, one spare bit line is sufficient. In other words, as illustrated in Fig. 3 (a), when WL_0 and BL_1 are selected, because C_{01} is defective, SBL is activated in place of BL_1, and read-out and write-in is performed in respect of SC_0. Here, the replacement of BL_1 by SBL is not something which normally occurs, as illustrated in Fig. 3 (b), when WL_3 and BL_1 are selected, BL_1 is activated and read-out and write-in is performed to the normal cell C_{31}.

[0029]

Moreover, SBL can also rescue defects on bit lines other than BL_1. As illustrated in Fig. 3 (c), when WL_2 and BL_2 are selected, SBL is activated instead of BL_2, and read out and write-in is performed to SC_2. In other words, each of the spare cells SC_i of the spare bit line can rescue any of the defective cells of the word line WL_i. Moreover, because there are no defective regular cells on WL_3, even if the spare cell SC_3 is defective, there is no failure of the rescue.

[0030]

By means of this type of embodiment, when reading out or writing in to a normal cell on the regular bit line BL_j including a defective cell, that regular bit line BL_j is activated, and there is no replacement by the spare bit line SBL. Moreover, even if there are defective cells in multiple regular bit lines BL_j, when no two of those defective cells are on the same regular bit line BL_j, one spare bit line SBL enables the rescue of defects on multiple regular bit lines BL_j by means of changing out the regular bit line BL_j by means of the spare bit line SBL in correspondence with the selected word line WL_i. As a result of this, because there is no wasteful change out of spare cells in respect of normal cells on defective bit two lines, the efficient use of normal cells is enabled. Moreover, because the rescue of defects of multiple regular bit lines using only one spare bit line, efficient and good rescue is enabled with very few spare bits lines. Furthermore, even if there are defective cells in the spare bit lines, the performance of the rescue of defects of regular cells is enabled.

[0031]

Fig. 4 is a circuit configuration diagram representing the second embodiment. This embodiment combines multiple word lines in one block (BWL_0, ~, BWL_m), and provides one spare decoder (SD_0, ~, SD_m) to each of the blocks. When the probability of the occurrence of defects in memory cells is low, and when defective memory cells are not generated one to each word line, this method reduces the area of the spare decoder, and a more efficient and good rescue of defects is enabled.

[0032]

Fig. 5 is a circuit diagram representing the third embodiment of the present invention. This embodiment does not provide spare memory cells in the spare bit line, but provides spare memory cells in the spare word line.

[0033]

The switching circuits SW_j (SW_0, SW_1, SW_2, SW_3) are connected to the column decoder CD_j, and every SW_j is controlled by a spare line decoder SRD_j (SRD_0, SRD_1, SRD_3, SRD_3). Each spare line decoder SRD_j records the line address of the defective regular cells replaced by spare cells on the spare word line SWL found on the bit line BL_j. Each regular bit line is divided in two, and one half is connected to a regular memory cell, and the other half is connected to a spare memory cell on the spare word line SWL. Then, SW_j can more easily selectively activate either.

[0034]

If the configuration is as described above, when each spare line decoder SRD_j has an input line address which corresponds to its own recorded address, the SW_j operates, and the column decoder CD_j is connected to the spare cell side of the bit line BL_j. When another address is input, the CD_j is connected to the regular cell side of the BL_j.

[0035]

In other words, when there is read-out/write-in to normal cell on a regular word line WL_j including a defective cell, that regular word line WL_j is selected, and there is no replacement by the spare word line SWL, and only when there is read-out/write-in to/from the defective cell on the regular word line WL_j including a defective cell is there replacement performed by the spare word line SWL. By this means, the rescue of the defects of plural regular word lines WL_j with only one spare word line SWL is enabled, such that the same good efficiency as in embodiment 1 is enabled.

[0036]

Fig. 6 is a circuit diagram representing the fourth embodiment of the present invention. The configuration of the memory cell array, column decoder, inverter and the address line are the same as that represented in the embodiment of Fig. 1. Spare column decoders SCD_j (SCD_0, SCD_1, SCD_2, SCD_3) are connected with respect of the regular word line WL_j in the same manner as in embodiment 1, and the output thereof is connected to the inverter I_0 via the NMOS transistor T_i. Each spare column decoder SCD_i records the row address of defective regular cells replaced with spare cells on the spare bit line SBL which is on the regular word line WL_i. The input of the inverter I_0 is precharged to the power source voltage V_{CC} by means of a PMOS transistor.

[0037]

A switching circuit SW_j is connected to each column decoder, and each SW_j is controlled by means of a spare line decoder SRD_j, Each spare line decoder SRD_j records the defective regular cell line address replaced by a spare cell on the spare word line SWL which is on the bit line BL_j. Each regular bit line BL_j is divided into two, and one side is connected to a regular memory cell, and the other is connected to a spare memory cell on a spare word line SWL. Then, the selection of the regular memory cell or the spare memory cell is performed by the SW_j.

[0038]

In this embodiment, two types of rescue are possible by means of the spare bit line and the spare word line, but firstly the rescue of defects by means of the spare bit line SBL is explained. When a regular word line WL_i is selected, the transistor T_i conducts and there is the connection of the output of the spare decoder SD_i and the input of the inverter I_0. When there is a defective cell C_{ij} on the regular word line WL_i, the spare column decoder SD_i records the address of

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.