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United States Patent [19]

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McAdams

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[54] **MEMORY DEVICE HAVING A NON-UNIFORM REDUNDANCY DECODER ARRANGEMENT**

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[75] Inventor: **Hugh McAdams, Houston, Tex.**

Primary Examiner—Glenn Gossage
Attorney, Agent, or Firm—Robby T. Holland; Lawrence J. Bassuk; Richard B. Havill

[73] Assignee: **Texas Instruments Incorporated, Dallas, Tex.**

[21] Appl. No.: **928,634**

[57] ABSTRACT

[22] Filed: **Aug. 13, 1992**

A memory device including a non-uniform redundancy decoder has one or more data blocks with each data block having an array of memory cells arranged in addressable rows and columns along row lines and column lines. Each array is configured into sub-blocks with each sub-block comprising a plurality of the memory cells. A given number of repair columns is allocated to a data block. A plurality of column repair decoder circuits are each connected to a repair column. These column repair decoder circuits are programmable with column and row address information corresponding to a section of an array column containing a defective memory cell to replace the defective cell with a memory cell in one of the repair columns. Different numbers of column repair decoder circuits are connected to the first and second column repair circuits, thereby creating a nonuniform distribution of column repair circuits. A method of assigning the nonuniform redundancy decoders is also disclosed.

Related U.S. Application Data

[63] Continuation of Ser. No. 714,321, Jun. 11, 1991, abandoned, which is a continuation of Ser. No. 501,064, Mar. 29, 1990, abandoned.

[51] Int. Cl.⁵ **G11C 7/00; G11C 29/00; G06F 11/20**

[52] U.S. Cl. **365/200; 365/230.06; 365/230.03; 371/10.1; 371/10.3**

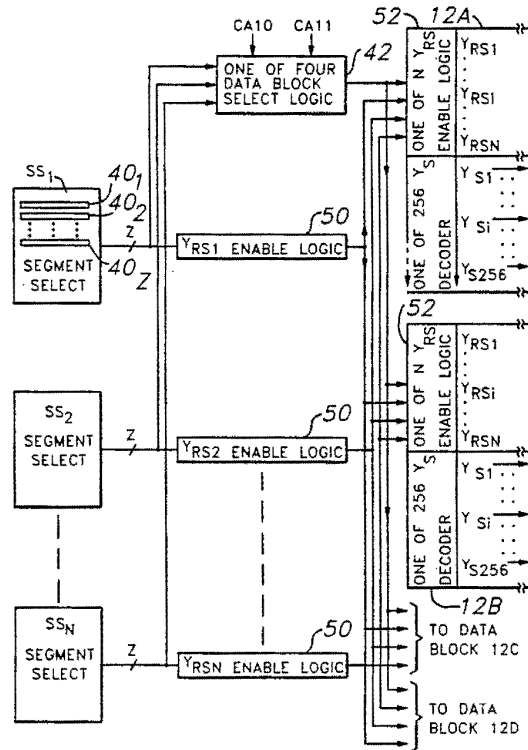
[58] Field of Search **365/200, 230.03, 230.06; 371/10.1, 10.2, 10.3**

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8 Claims, 16 Drawing Sheets



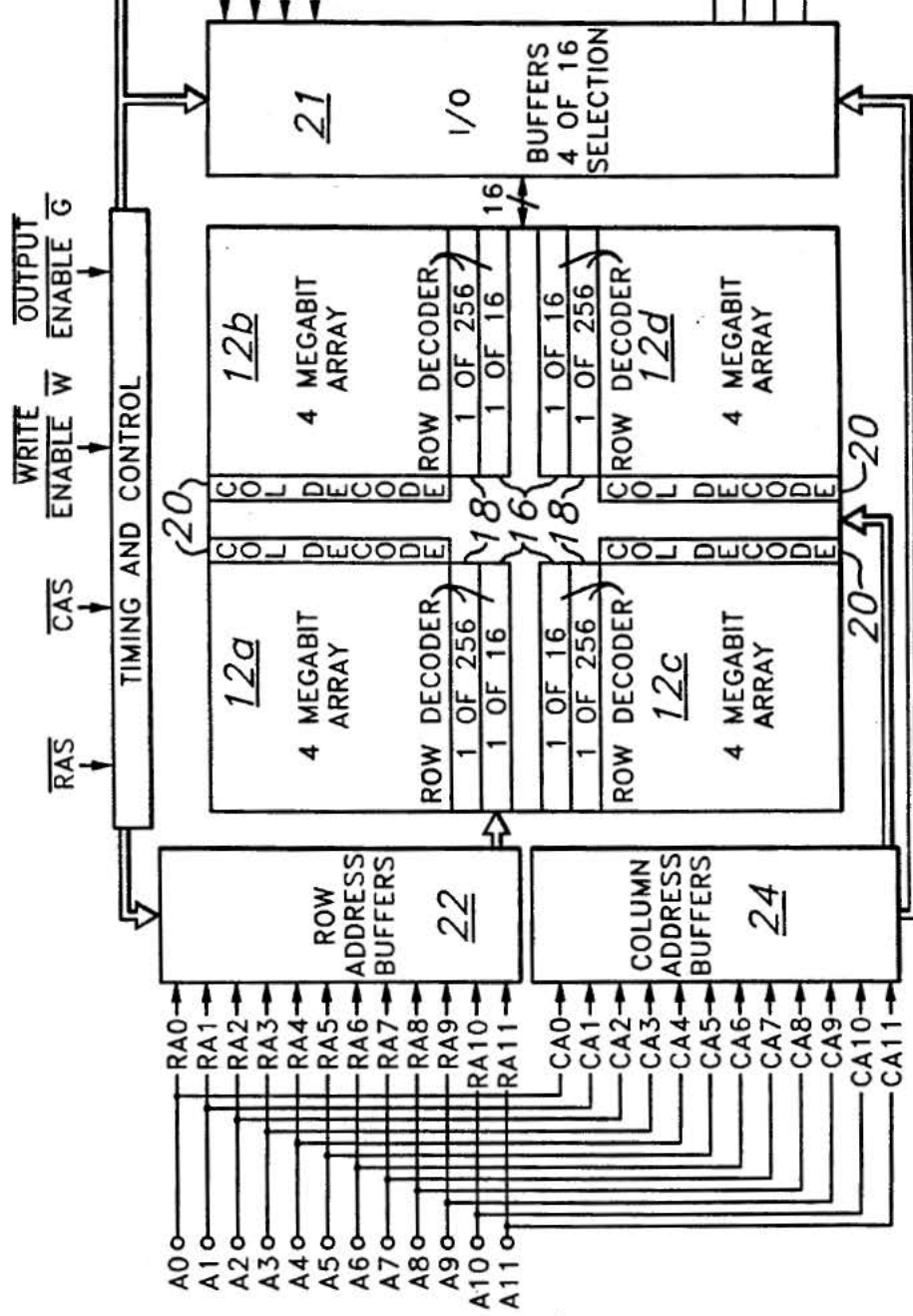


Fig. 1

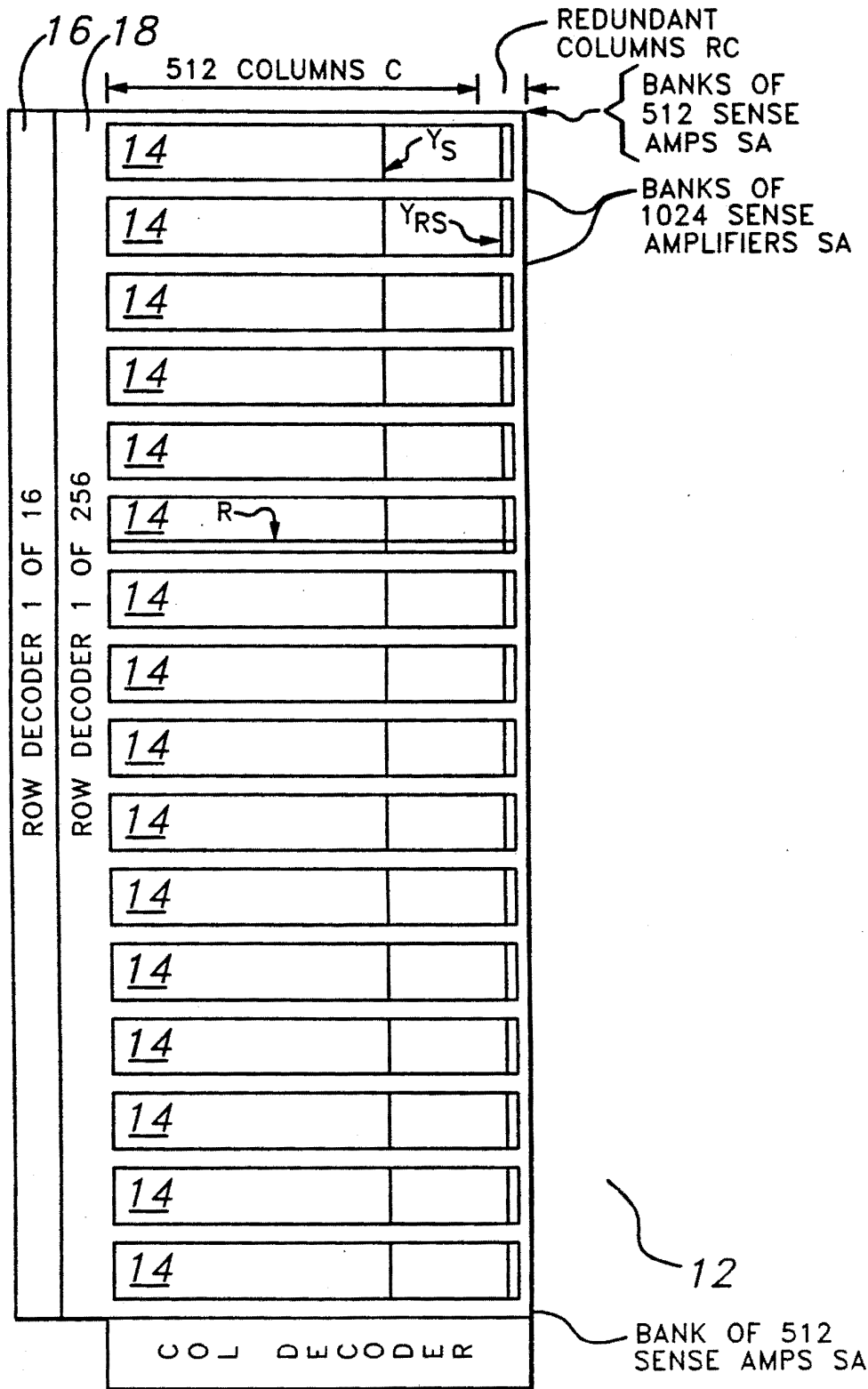


Fig. 2

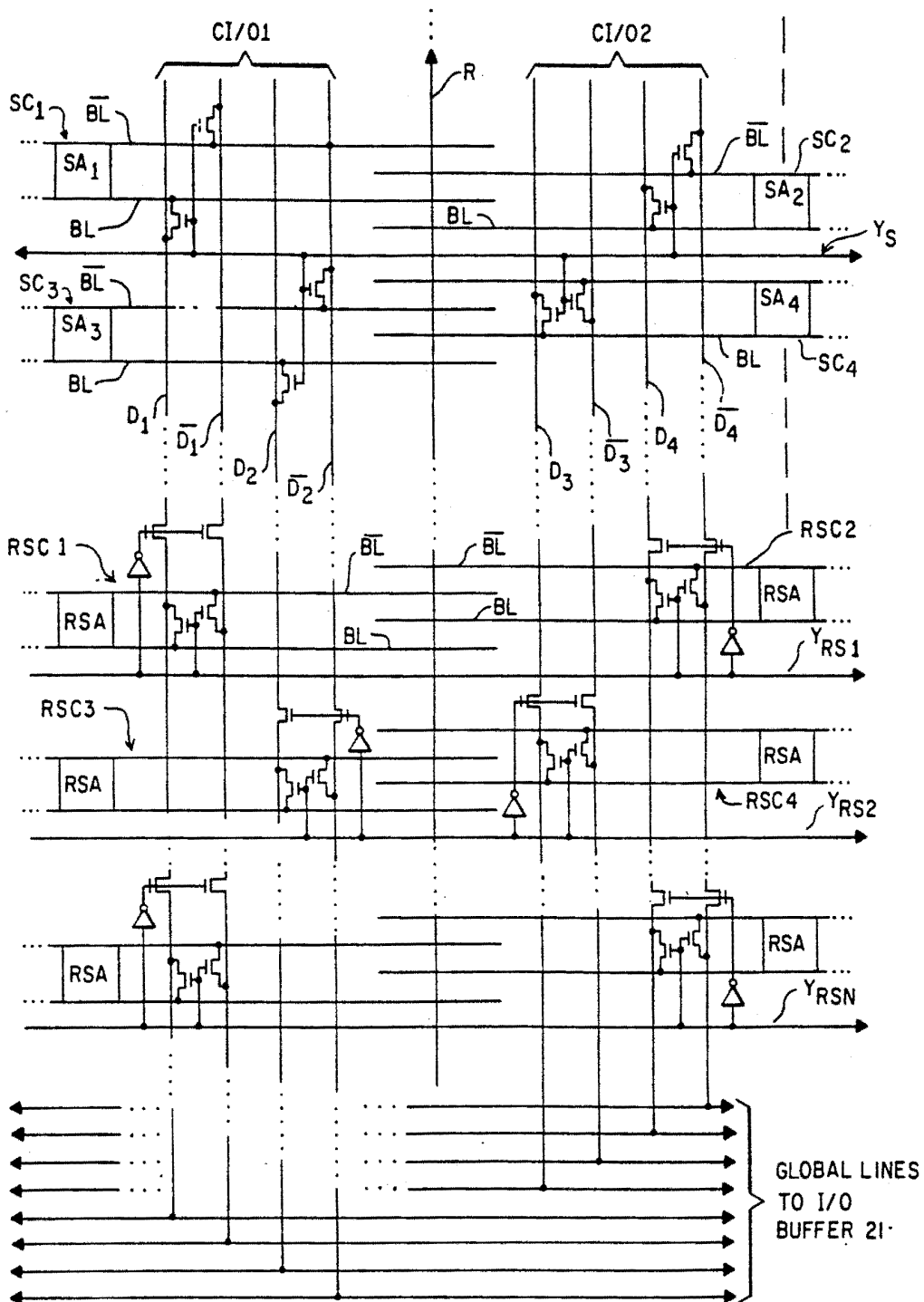


FIG. 3

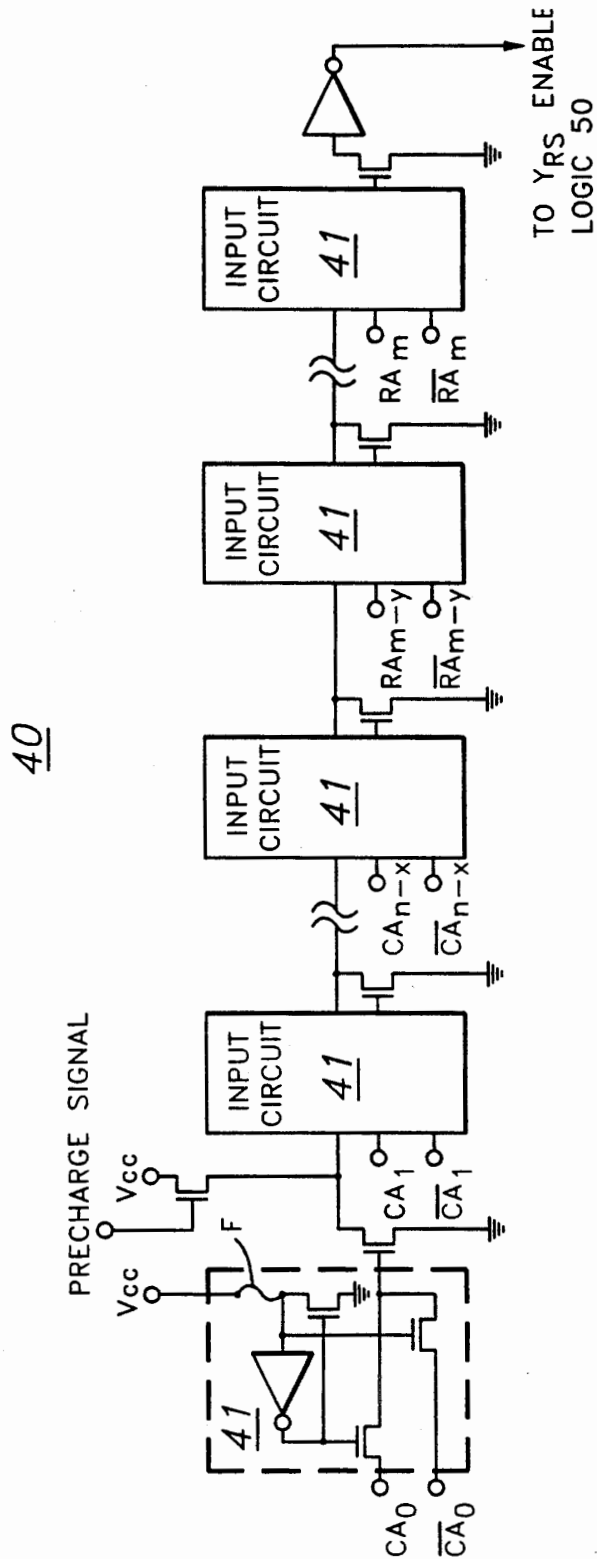


Fig. 4

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