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SUMMARY

- Extensive leadership experience including:
  - Chair, Electrical and Computer Engineering Department, Boise State University;
  - Dealing with conflict, problems, and limited resources;
  - Leading the department through ABET accreditation;
  - Creation and implementation of both Master and Doctoral programs in ECE.
- Active scholar (h-index > 30 and an i10-index > 80) whose research is focused on:
  - High-speed interfaces for electro-optic, mixed-signal, and analog integrated circuits;
  - Design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide);
  - Analog and mixed-signal circuit techniques for nanometer CMOS; 3D packaging techniques
  - The design of instrumentation for scientific research
  - Delivery of circuit design education to off-campus students/engineers via the Internet.
- Mentor to:
  - Approximately 75 graduate students (major professor), http://CMOSedu.com/jbaker/students/students.htm
  - Electrical and Computer Engineering Department faculty;
  - Engineers locally, nationally, and internationally;
  - New and established companies.
- Inventor with 137 granted US patents
- Experienced integrated circuit designer and educator with significant industry experience. See additional information at http://cmosedu.com/jbaker/projects/fund.htm
- Textbook authorship and Internet contributions (see http://CMOSedu.com), that have helped tens of thousands of engineers around the world.
- Recognized by the IEEE Power Electronics Society with the Best Paper Award in 2000 (*IEEE Transactions on Power Electronics*) from PhD dissertation work.
- International known in the field of integrated circuit design, recipient of many honors including the Terman Award, the IEEE CAS Education Award, and IEEE Fellow.

EDUCATION

Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*

M.S. and B.S. in Electrical Engineering: May 1986 and 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

ACADEMIC EXPERIENCE

January 1991 - Present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, and the Air Force Research Lab.
- Current research interests are:
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories
  - Analog and mixed-signal circuit design for communication systems, synchronization, energy storage, and data conversion
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
  - Reconfigurable electronics design using nascent memory technologies
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Methods to deliver circuit design education to industry and off-campus students, see videos here
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

INDUSTRIAL EXPERIENCE

2013 - present: Working with Freedom Photonics and Attolo Engineering in the Santa Barbara area on the integration of optics with CMOS integrated circuits including Avalanche Photodiodes. Work has resulted, and should continue to result in, support via the SBIR and STTR programs.

2013 - present: Working with National Security Technologies, LLC,) on the Design of Integrated electrical/photonic application specific integrated circuit (ASIC) design.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors with memory for very high-speed consumer imager products.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (now Oracle) VLSI research group. Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power and 3D packaging.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project between Micron and HP labs in magnetic memory using the MJT memory cell. Worked on numerous projects (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing (35 nm technology node).

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1998: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns risetime and 8 ns falltime for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble shooting electric motors on mining equipment.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services are listed below. I have been deposed eight times and given testimony at one trial.

Paul Hastings LLP (New York City, NY and Washington, DC)

Case – *Samsung, Inc.* v. Elbrus International Limited
Case Numbers - IPR2015-01523 and IPR2015-01524. Filed on June 26, 2015.
Case Subject Matter – High-speed, low-power data transfer.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for *SK hynix*, Inc. on matters relating to investigation of certain patents owned by Longitude Licensing Ltd.
Case Subject Matter – Semiconductor random access memory and communication interfaces.
Work Performed – Provided expert consulting services in 2015.

Ropes & Gray LLP (New York City, NY)

Case – *Samsung, Inc.* v. Imperium IP Holdings (Cayman), Ltd.
Case Number – IPR2015-01233. Filed on May 21, 2015.
Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – *Silergy Corporation* v. Monolithic Power Systems, Inc.
Case Numbers – IPR2015-00803 and IPR2015-00804. Filed on February 24, 2015.
Case Subject Matter – Microelectronic packaging.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Jones Day LLP (San Diego, CA)

Case – *Micron Technology, Inc.* v. eDigital Corp.
Case Number - IPR2015-00519. Filed on December 31, 2014.
Case Subject Matter – Methods for memory management in non-volatile flash memories.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (Atlanta, GA and Washington, DC)

Case – *Micron Technology, Inc.* v. MLC Intellectual Properties and BTG USA/International Inc.
Case Number - IPR2015-00504. Filed on December 24, 2014.
Case Subject Matter – Multi-level non-volatile floating gate memory, e.g. EPROM, EEPROM, and flash technologies.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Skadden, Arps, Slate, Meagher & Flom LLP & Affiliates (Palo Alto, CA)

Case – ALFRED T. GIULIANO, Chapter 7 Trustee of the Ritz Estate; CPM ELECTRONICS INC.; E.S.E. ELECTRONICS, INC. and MFLASH, INC., on Behalf of Themselves and All Others Similarly Situated v. *SanDisk Corp.*
Case Number – California, ND (Oakland) 4:10-cv-02787. Fourth amended complaint filed on September 24, 2014.
Case Subject Matter – Non-volatile semiconductor flash memory.
Work Performed – Provided expert consulting services.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Monolithic Power Systems v. Inc. *Silergy Corporation*
Case Number - California, ND 3:14-cv-01745. First amended complaint filed on July 7, 2014.
Case Subject Matter – Microelectronic packaging.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Ropes & Gray LLP (East Palo Alto, CA, New York City, NY, and Washington, DC)

Case – Macronix International Co., Ltd. v. *Spansion, Inc.*, *Aerohive Networks*, *Allied Telesis*, *Ciena*, *Delphi Automotive*, *Polycom*, *Ruckus Wireless*, *ShoreTel*, *Tellabs*, and *TiVo*
Case Number – ITC Investigation No. 337-TA-922. Complaint filed on June 27, 2014.
Case Subject Matter – Devices containing non-volatile memory and products containing the same.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, Markman tutorial, and expert report.

Ropes & Gray LLP (Boston, MA and New York City, NY)

Case – Imperium IP Holdings (Cayman), Ltd. v. *Samsung, Inc.*
Case Number – Texas, ED 4:14-cv-00371. Complaint filed on June 9, 2014.
Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Quinn Emanuel Urquhart & Sullivan, LLP (San Francisco, CA and Washington, DC)

Case – Freescale Semiconductor, Inc. v. *MediaTek, Inc.*, et. al.
Case Number – ITC Investigation No. 337-TA-920. Amended complaint filed on May 27, 2014.
Case Subject Matter – Semiconductor integrated circuits and devices containing the same.
Work Performed – Provided expert consulting services.

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