UNITED STATES PATENT AND TRADEMARK OFFICE
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BEFORE THE PATENT TRIAL AND APPEAL BOARD
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MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

_____

Case IPR. No. **Unassigned**
U.S. Patent No. 5,894,441
Title: SEMICONDUCTOR MEMORY DEVICE
WITH REDUNDANCY CIRCUIT

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**Declaration of R. Jacob Baker, Ph.D. in Support of
Petition For Inter Partes Review
of U.S. Patent No. 5,894,441
Under 37 C.F.R. § 1.68**

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I, R. Jacob Baker, hereby declare as follows:

I.   INTRODUCTION

1.   My name is R. Jacob Baker. My findings, as set forth herein, are based on my education and background in the fields discussed below.

2.   I have been retained on behalf of Petitioner Micron Technology, Inc. ("Micron") to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition ("Petition") concerning U.S. Patent No. 5,894,441 ("the 441 Patent," MICRON-1001). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3.   I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

4.   My compensation is not based on the resolution of this matter.

II.   BACKGROUND AND QUALIFICATIONS

5.   I currently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor Electrical Engineering between 1998 and 2000 and Assistant Professor of

Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

6.   I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

7.   As described in my CV (MICRON-1004), I am a licensed Professional Engineer in the state of Idaho and have more than 25 years of experience, including extensive experience in circuit design and manufacture of Dynamic Random Access Memory (DRAM) integrated circuit chips and CMOS Image Sensors (CISs) at Micron in Boise, Idaho. I also spent considerable time working on the development of Flash Memory while at Micron. My efforts resulted in more than a dozen Flash-memory related patents. Among other experiences, I led development of the delay-locked loop (DLL) in the late 90s so that Micron products could transition to the DDR memory standard. I have worked as a consultant at other companies designing memory chips, including Sun, Oracle, and Contour Semiconductor. I have also worked as a consultant at other companies designing CIS's, including OmniVision and Lockheed Martin.

8.   I have taught courses in integrated circuit design (analog, digital, mixed-signal, etc.), linear circuits, microelectronics, communication systems, and

fiber optics. As a professor, I have been the main advisor to five Doctoral students and over 50 Masters students.

9.   I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (three editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and co-authored, more than 75 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on over 135 granted U.S. patents in integrated circuit designs including flash memory and DRAM.

10.   I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educators in recognition of the educator's contributions to the profession.

11.   I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

12.   I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State

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