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United States Patent [19]
Nakazawa

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[45] **Date of Patent:** **Apr. 13, 1999**

[54] **SEMICONDUCTOR MEMORY DEVICE WITH REDUNDANCY CIRCUIT**

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[21] Appl. No.: **09/050,354**

[57] **ABSTRACT**

[22] Filed: **Mar. 31, 1998**

A semiconductor memory device which enhances the relief efficiency of defective bit lines by means of redundant bit lines is disclosed. To a column redundancy decoder are supplied not only a Y address but also a part of an X address. When a Y address corresponding to a defective bit line is supplied to the column redundancy decoder, the column redundancy decoder generates a detection signal. In this case, replacement by means of a redundant bit line is carried out if the part of the X address indicates a region where the defective bit line exists, and the replacement by means of a redundant bit line will not take place if it indicates a region where the defective bit line does not exist.

[30] **Foreign Application Priority Data**

Mar. 31, 1997 [JP] Japan 9-081203

[51] **Int. Cl.⁶** **G11C 7/00**

[52] **U.S. Cl.** **365/200; 365/230.03; 365/230.06**

[58] **Field of Search** 365/200, 201, 365/230.03, 230.06

[56] **References Cited**

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15 Claims, 8 Drawing Sheets

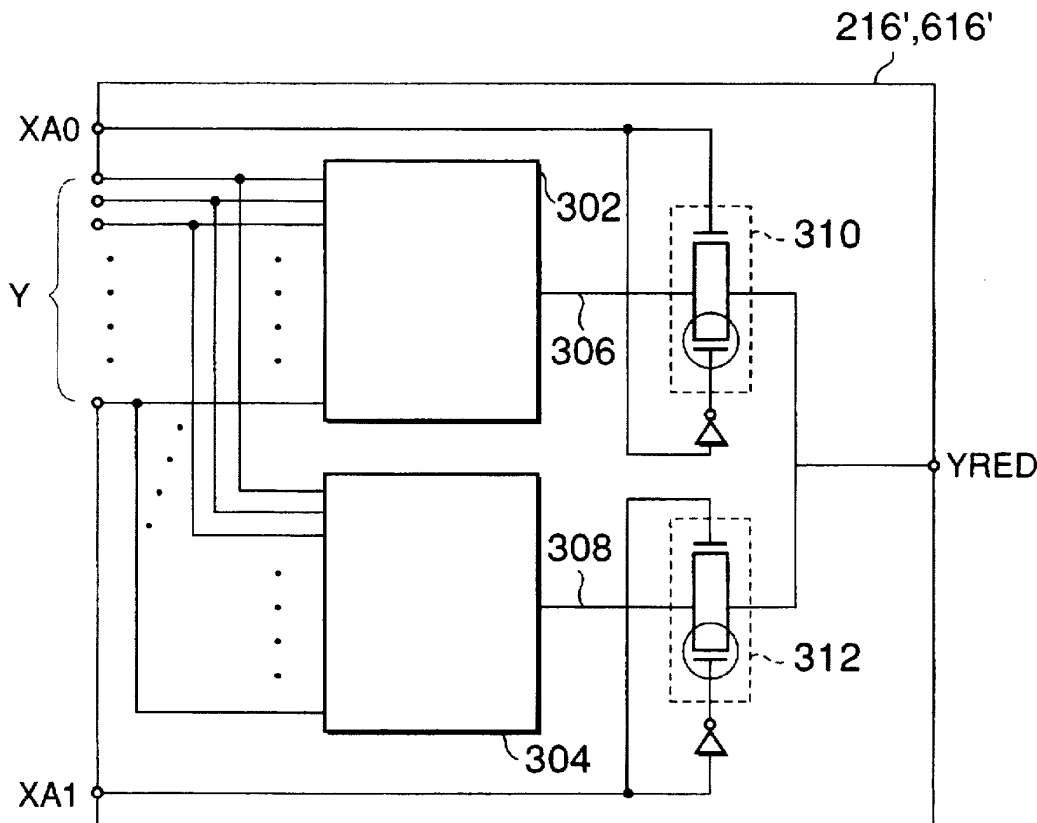


FIG. 1

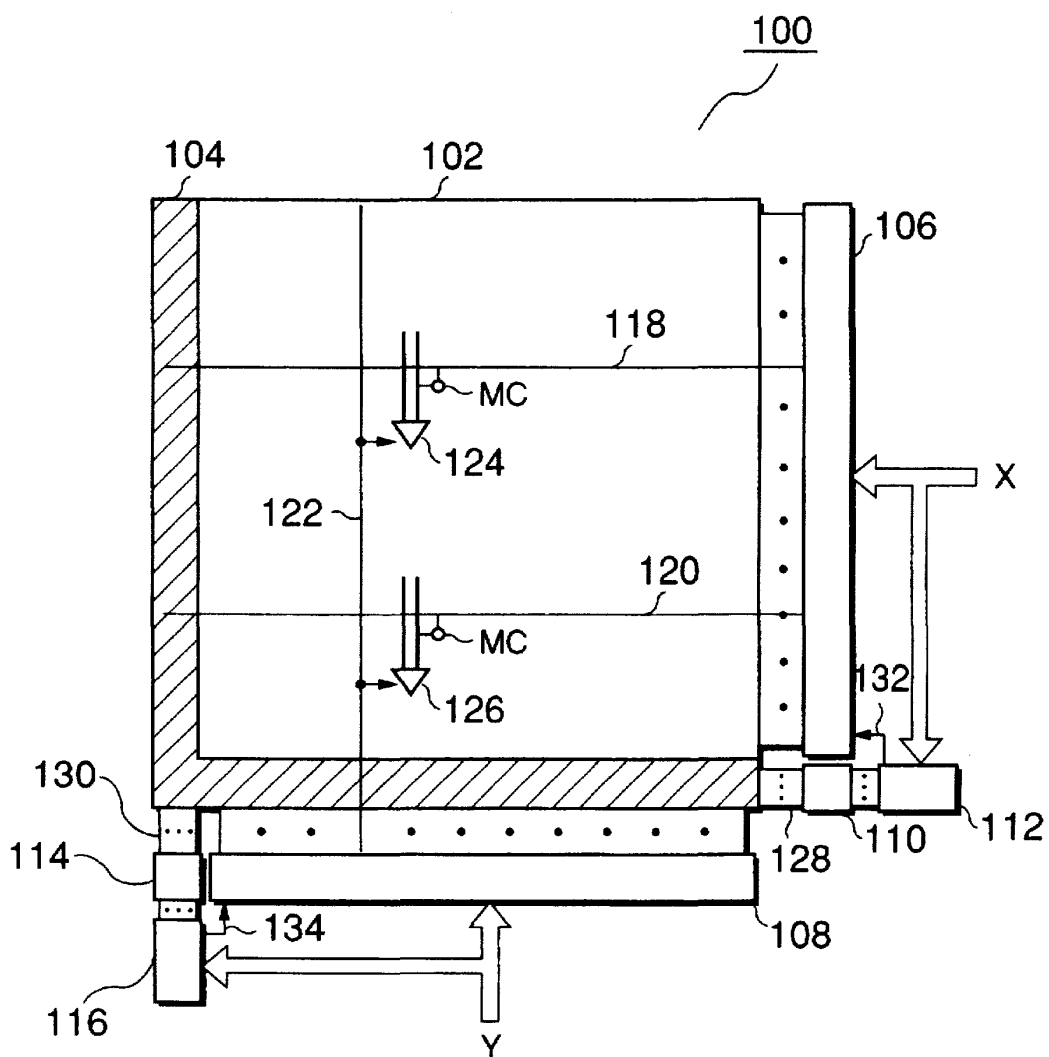


FIG.2

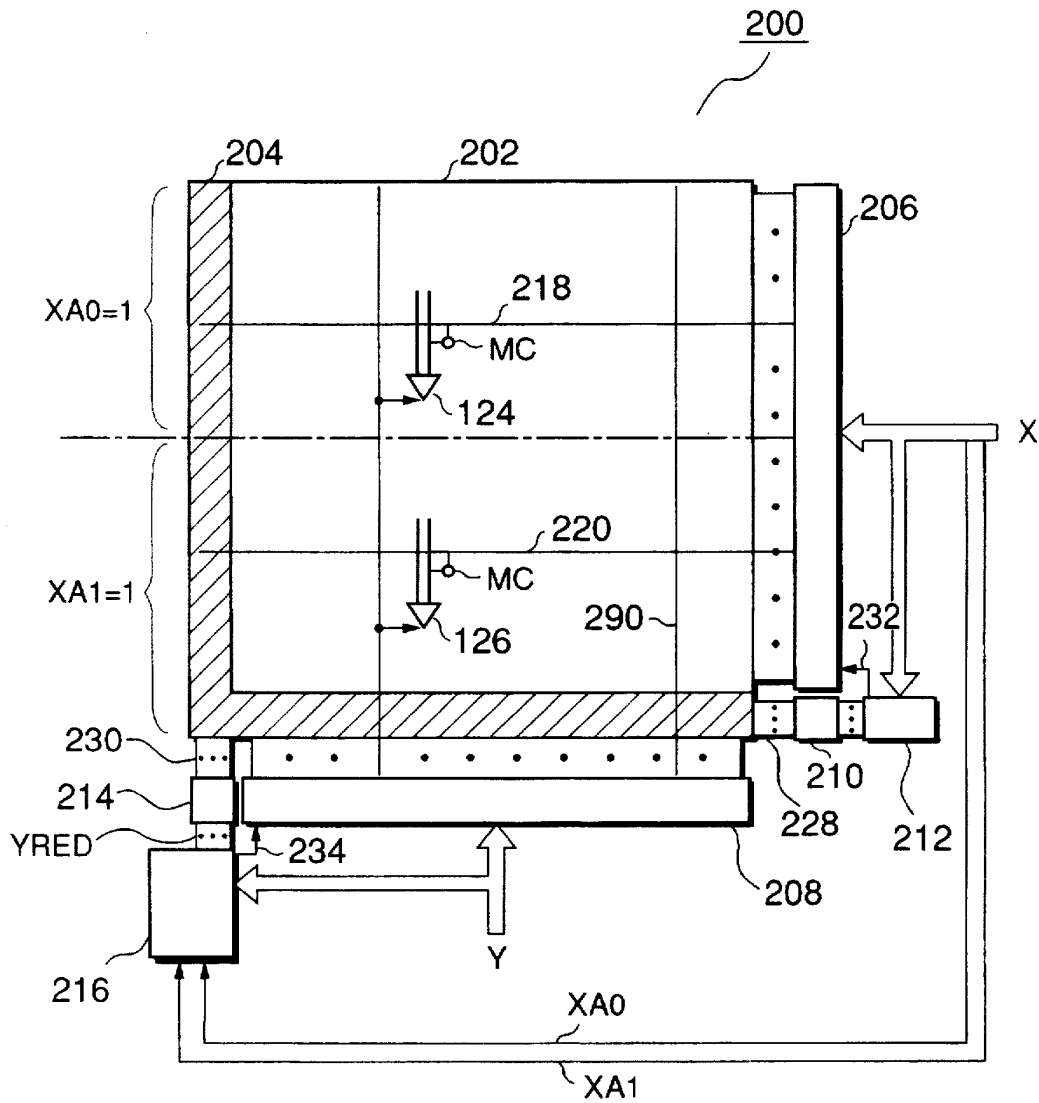


FIG.3

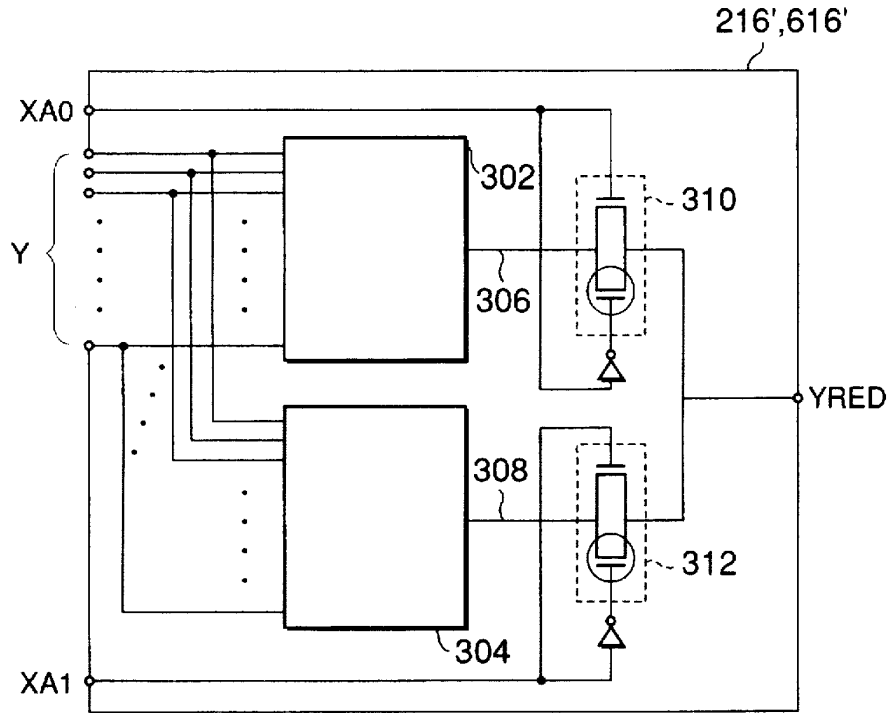


FIG.4

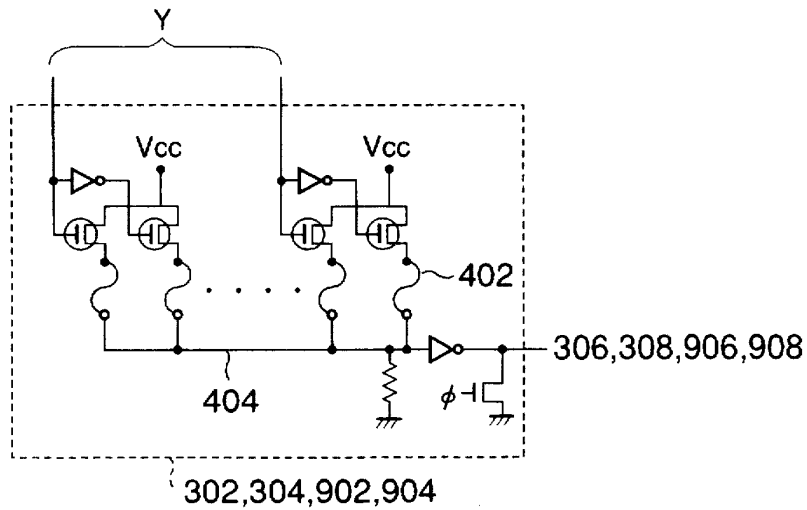
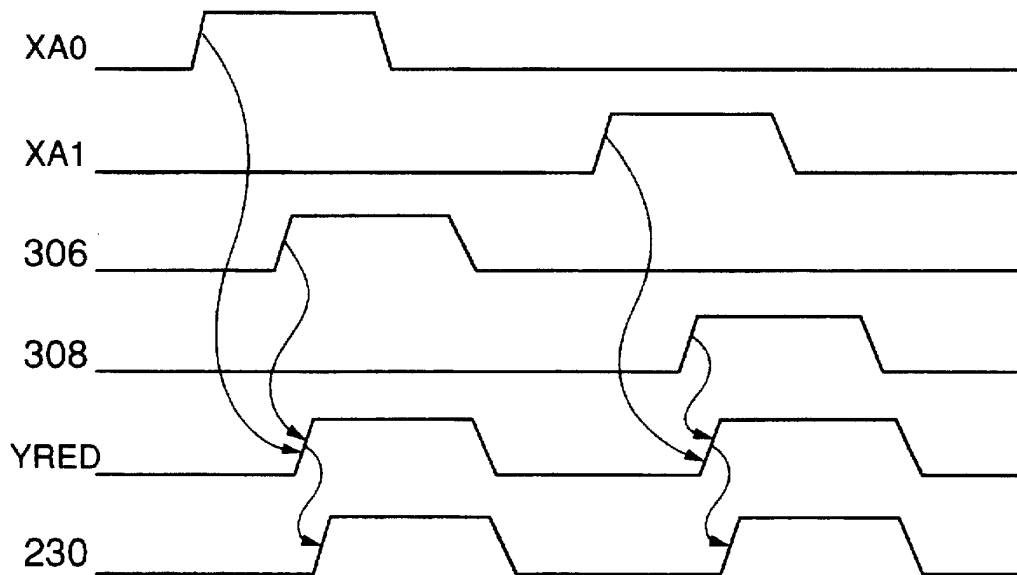


FIG.5



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