UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

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Case IPR. No. 2016-00094
U.S. Patent No. 5,894,441
Title: SEMICONDUCTOR MEMORY DEVICE
WITH REDUNDANCY CIRCUIT

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**Petitioner's Request For Rehearing
Under 37 C.F.R. § 42.71(d)**

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Patent Trial and Appeal Board
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

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I.   INTRODUCTION

On April 12, 2016, the Board issued a Decision denying institution of *Inter Partes* Review of U.S. Pat. No. 5,894,441 ("441 Patent") on Petitioner's Ground 2. Paper 8, Decision ("Dec."). This Ground contends that claims 6-15[1] are invalid under (pre-AIA) 35 U.S.C. § 103 because they are obvious over U.S. Pat. No. 5,270,975 ("McAdams") in view of JP Pat. Appl. No. H06-052696 ("Minami"). Petition ("Pet."), Paper 1 at 4. First, the Board concluded that McAdams in view of Minami does not teach the last limitation of claim 6, *i.e.*, "the column redundancy decoder limitation." Dec. at 8-13. Second, the Board found that the Petition does not provide sufficient reasoning with some rational underpinning to support the legal conclusion of obviousness. *Id.* at 13-16.

This Request for Rehearing seeks reconsideration of Ground 2 for claims 6-15. Petitioner respectfully submits that the Board overlooked or misapprehended (1) the complete teachings of and contentions regarding McAdams that are set forth in the Petition and Declaration of Dr. Jacob Baker (MICRON-1003) ("Baker Decl."), and instead incorrectly relied on passages from McAdams "alone" and "by itself," and (2) the relevant teachings of Minami with respect to claim 6 and the specific rationale for combining these teachings with McAdams for claim 6.

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[1] Ground 2 also included claim 3, but Patent Owner disclaimed it. Dec. at 2.

The column redundancy decoder limitation recites "a column redundancy decoder activating said redundant column selection line in response to said first column address when said second word line is activated." Dec. at 9. By way of example, the Board found that:

> The indication that each decoder is programmable 'with column and row address information corresponding to a section of an array column containing a defective memory cell' (*id.*), does not **by itself** indicate that the redundant column selection line is activated in response to the first column address (which is the same address that activates the first column selection line) when 'said second word line is activated,' as recited in claim 6.

Id. at 10 (emphasis added). By viewing a snippet from McAdams "by itself," the Board misapprehended or overlooked that McAdams discloses that its redundant decoder is programmable—**with any address**—including (1) the first column address (which also activates the first column selection line) and (2) the second word line address (which activates the second word line), such that it activates a redundant column selection line in response to this address. Also, the Board overlooked or misapprehended that Minami supplements McAdams for claim 6 by confirming that it would have been obvious for McAdams to use the conventional DRAM addressing scheme, *i.e.*, a word line is <u>first</u> activated using a word line address and the column line is <u>then</u> activated using the column address ("conventional row-then-column approach"). Thus, McAdams in view of

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