IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Conley:	Petition for *Inter Partes* Review
U.S. Patent No. 7,818,490	Attorney Docket No.: 337722-000080.490
Issued: October 19, 2010	Customer No.: 26379
Title: PARTIAL BLOCK DATA PROGRAMMING AND READING OPERATIONS IN A NON-VOLATILE MEMORY	Petitioner: Apple Inc.
	Real Party in Interest: Apple Inc.

DECLARATION OF DR. VIVEK SUBRAMANIAN

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EXHIBITS

Exhibit Number	Description
1201	U.S. Patent 7,818,490 to Conley
1202	File History for U.S. Patent 7,818,490
1204	CV for Dr. Vivek Subramanian
1205	U.S. Patent No. 5,822,781 to Wells (“Wells”)
1206	U.S. Patent No. 5,457,658 to Niijima (“Niijima”)
1208	Flash Memories, edited by Cappelletti, et al (1999) (“Cappelletti”)
1209	PC Card Standard, Volumes 1 and 3 (1999) (“PC Card Standard”)
1210	PCT WO 99/35650 (“Hazen”)
1211	Designing With Flash Memory, Brian Dipert and Markus Levy (1994) (“Dipert”)

A. Introduction

1. I, Vivek Subramanian, declare as follows:

2. I am making this Declaration at the request of Petitioner Apple Inc. regarding its Petitions for *Inter Partes* Review of U.S. Patent No. 7,818,490 (the "'490 patent").

3. I am being compensated for my work at my standard rate of $550 per hour. My compensation does not depend on the outcome of this proceeding.

4. As part of my analysis, I reviewed the following materials:

Exhibit 1201	U.S. Patent 7,818,490 to Conley
Exhibit 1202	File History for U.S. Patent 6,818,490
Exhibit 1205	U.S. Patent No. 5,822,781 to Wells ("Wells")
Exhibit 1206	U.S. Patent No. 5,457,658 to Niijima ("Niijima")
Exhibit 1208	Flash Memories, edited by Cappelletti, et al (1999) ("Cappelletti")
Exhibit 1209	PC Card Standard, Volumes 1 and 3 (1999) ("PC Card Standard")
Exhibit 1210	PCT WO 99/35650 ("Hazen")
Exhibit 1211	Designing With Flash Memory, Brian Dipert and Markus Levy (1994) ("Dipert")

B. Relevant Background and Experience

5. My background and experience is summarized in my curriculum vitae, a true and correct copy of which is submitted as Exhibit 1204. Some of the relevant points are described below as well.

6. I received a B.S. in electrical engineering from Louisiana State University in 1994, an M.S. in electrical engineering from Stanford University in 1996, and a Ph.D. in electrical engineering from Stanford University in 1998.

7. In 1998, I co-founded Matrix Semiconductor, Inc. to develop high density memory technology.

8. I have been teaching in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley since 2000. I was an Assistant Professor from 2000 to 2005, an Associate Professor from 2005 to 2011, and a Professor from 2011 to the present.

9. I have been an adjunct professor at the Sunchon National University in Sunchon, Korea since 2009, leading research in printed electronics.

10. I have been an independent consultant in the semiconductor industry since 2000, focusing on memory technology, flexible electronics, and RFID technology.

11. I have published more than 200 technical papers in journals and at conferences.

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