

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Conley:

U.S. Pat. No. 7,818,490

Issued: October 19, 2010

Title: PARTIAL BLOCK DATA
PROGRAMMING AND READING
OPERATIONS IN A NON-VOLATILE
MEMORY

Petition for *Inter Partes* Review

Attorney Docket No.:
337722-70.490b

Customer No.: 26379

Petitioner: Apple Inc.
Real Party-in-Interest: Apple Inc.

PETITION FOR *INTER PARTES* REVIEW

Mail Stop Patent Board
Patent Trial and Appeal Board
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the provisions of 35 U.S.C. §§ 311-319, Apple Inc. (hereinafter “Petitioner”) hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 34-38 and 40-64 of United States Patent No. 7,818,490 (“the ’490 patent”)

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EXHIBITS

- Ex. 1101 U.S. Patent No. 7,818,490 to Conley (“the ’490 patent”)
- Ex. 1102 Prosecution File History for U.S. Patent No. 7,818,490
- Ex. 1103 Declaration of Dr. Vivek Subramanian
- Ex. 1104 CV for Dr. Vivek Subramanian
- Ex. 1105 U.S. Patent No. 5,822,781 to Wells (“Wells”)
- Ex. 1106 U.S. Patent No. 5,457,658 to Nijima (“Nijima”)
- Ex. 1108 Flash Memories, edited by Cappelletti, et al (1999)
 (“Cappelletti”)
- Ex. 1109 PC Card Standard, Volumes 1 and 3 (1999) (“PC Card
 Standard”)
- Ex. 1110 PCT WO 99/35650 (“Hazen”)
- Ex. 1111 Designing With Flash Memory, Brian Dipert and Markus
 Levy (1994) (“Dipert”)

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