PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11C 16/04	A1	(11) International Publication Number: WO 99/35650
		(43) International Publication Date: 15 July 1999 (15.07.99)

(21) International Application Number: PCT/US98/25217

(22) International Filing Date: 24 November 1998 (24.11.98)

(30) Priority Data:
09/002,649 5 January 1998 (05.01.98) US

(71) Applicant *(for all designated States except US)*: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

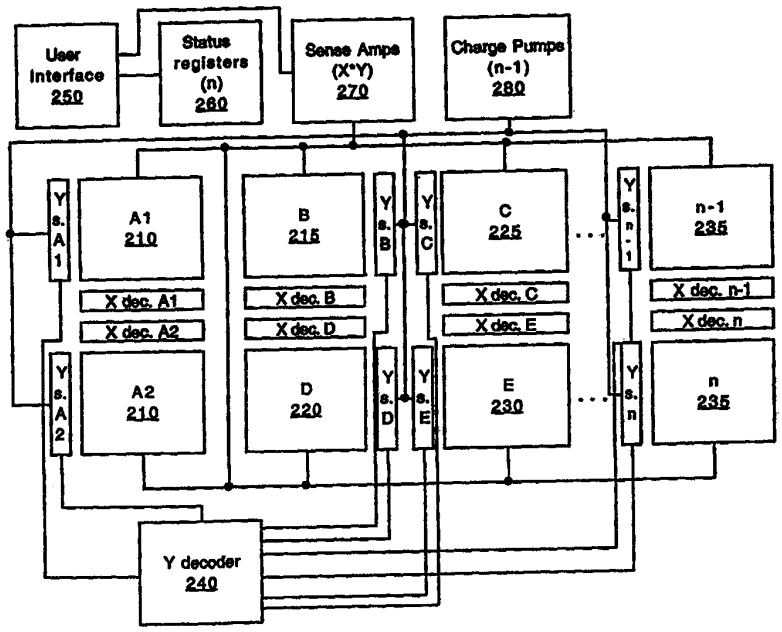
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: HAZEN, Peter, K. [US/US]; 2450 Hidden Oaks Lane, Auburn, CA 95603 (US). ALEXIS, Ranjeet [IN/US]; 101 Alvaston Court, Folsom, CA 95630 (US). LARSEN, Robert, E. [US/US]; 5267 Deerwood Drive, Shingle Springs, CA 95682 (US). BROWN, Charles, W. [US/US]; 123 Hopper Lane, Folsom, CA 95630 (US). TALREJA, Sanjay [IN/US]; 105 Boxcar Way, Folsom, CA 95630 (US).

(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: FLASH MEMORY PARTITIONING FOR READ–WHILE–WRITE OPERATION



(57) Abstract

A method and apparatus for partitioning a flash memory device (20) is provided. The flash memory device includes a plurality of partitions, (210, 215, 220, 225, 230), each partition able to be read, written, or erased simultaneously with the other partitions.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

FLASH MEMORY PARTITIONING FOR READ-WHILE-WRITE OPERATION

FIELD OF THE INVENTION

The present invention relates to flash memory, and more specifically, to partitioning of flash memory.

BACKGROUND

Flash memory devices are special type of EEPROM that can be erased and written to in blocks instead of one byte at a time. Some applications of the flash memory include embedded control code and data of a cellular telephone so that it can easily be updated if necessary. Flash memory may also be used in modems because it enables the modem manufacturer to support new protocols as they become standardized. Flash memory may further be used in computers to provide a basic input/output system (BIOS) that can be upgraded. Other uses are known in the art.

Figure 1 illustrates one prior art flash memory device 100. The memory 110 into which data is written has an X-decoder 160 and a Y-decoder 180 associated with it. The X-decoder 160 and Y-decoder 180 permit addressing the rows and columns of memory. A user interface 120 controls the flash memory device 100. The user interface 120 interfaces with a processor that controls access to the memory 110. A status register 130 stores the current status -- writing, reading, or erasing -- of the memory 110. The processor knows the status of the flash memory from the user interface 120.

Sense amplifiers 140 are associated with the memory 110. In one prior art implementation, the sense amplifiers are used to amplify signals for writing to and reading from the memory 110. For a row divided into sixteen input/outputs (I/Os), sixteen sense amplifiers 140 are used for writing and reading, one for each I/O. A charge pump 150 is further included in the flash memory 100. The charge pump 150 is used to provide the voltage levels needed for reading from, writing to, and erasing the memory 110. Generally, prior art flash memory devices are erased and written to as a block, consisting of a subset of memory 110. There is one set of circuitry, thus a user can not write to

one block of the flash memory while simultaneously erasing or reading another block of the memory.

Simultaneous operation is desired in some applications that are constrained by the erase time (typically 250-500 ms) of a flash memory block. For example, a cellular telephone executes code directly from the flash memory. It is advantageous to be able to erase a separate memory block to reclaim space for data storage at the same time.

One prior art solution to this problem is to have multiple flash memory devices. In that case, one device may be written to, while the other device is being erased. This has numerous disadvantages. The multiple devices take up more real-estate. Because there are multiple devices hardware is duplicated. Additionally, using multiple flash memory devices may cost more, increase power use, and decrease overall system reliability.

SUMMARY OF THE INVENTION

The present invention relates to partitioning of a flash memory device to permit read-while-write operations. The flash memory device includes a plurality of partitions, each partition able to be read, written, or erased simultaneously with the other partitions.

Other features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 illustrates a prior art flash memory device.

Figure 2 illustrates one embodiment of a multi-partitioned flash memory device.

Figure 3 illustrates one embodiment of a three partitioned flash memory device.

Figure 4 illustrates an example of a cellular telephone using a flash memory device.

DETAILED DESCRIPTION

A method and apparatus for partitioning a flash memory for read-while-write operation is described. It is an intended advantage of the present invention to permit simultaneous reading, and/or writing and/or erasing operations on a single flash memory device. It is a further intended advantage of the present invention to permit updating of code stored on a flash memory device while code is being executed.

Figure 2 illustrates a multi-partitioned flash memory device. Partitions A 210, B 215, C 225, D 220, E 230, . . . n-1 235, n 235 are illustrated. Each partition is implemented as a physically separate device on the flash memory device. For one embodiment, each partition is implemented on a different physical plane. Each of the partitions 210, 215, 220, 225, 225, 230, 235, and 240 has associated an X decoder, and a Y selector. Each of the Y selectors are coupled to a Y decoder 240, that controls the Y selectors. For an alternative embodiment, multiple Y decoders 240 may be present in the system. The X decoders and Y selectors enable selection of a specific area within flash memory 200 for access, including reading, writing, or erasing. Having multiple X selectors and Y decoders permits simultaneous access to more than one subsection of the flash memory. For example, while partition A may be erased, partition B may simultaneously be read, and partition C written to. Each of the partitions may include one or more blocks, that may be erased separately. Thus, for example, a memory in partition A may be written to, while a memory block in partition B is being erased.

A user interface 250 permits a user to control the access to the flash memory 200. For one embodiment, the user interface 250 is part of the flash memory itself. For an alternative embodiment, the user interface 250 is located on a separate chip. The interface includes a number of state machines used to control each of the write parallel operations. Thus, if there can be two parallel write operations (writing to the data block while updating the code, for example), there are two state machines. If there can be three parallel write operations, three

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.