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(12) **United States Patent**
Conley

(10) **Patent No.:** **US 7,818,490 B2**
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(54) **PARTIAL BLOCK DATA PROGRAMMING AND READING OPERATIONS IN A NON-VOLATILE MEMORY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(Continued)

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Assistant Examiner—Ngoc V Dinh

(65) **Prior Publication Data**

(74) Attorney, Agent, or Firm—Davis Wright Tremaine LLP

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Related U.S. Application Data

(57) **ABSTRACT**

(63) Continuation of application No. 10/841,388, filed on May 7, 2004, now Pat. No. 6,968,421, which is a continuation of application No. 09/766,436, filed on Jan. 19, 2001, now Pat. No. 6,763,424.

Data in less than all of the pages of a non-volatile memory block are updated by programming the new data in unused pages of either the same or another block. In order to prevent having to copy unchanged pages of data into the new block, or to program flags into superceded pages of data, the pages of new data are identified by the same logical address as the pages of data which they superceded and a time stamp is added to note when each page was written. When reading the data, the most recent pages of data are used and the older superceded pages of data are ignored. This technique is also applied to metablocks that include one block from each of several different units of a memory array, by directing all page updates to a single unused block in one of the units.

(51) **Int. Cl.**
G06F 9/24 (2006.01)

(52) **U.S. Cl.** **711/103; 711/113; 711/115**

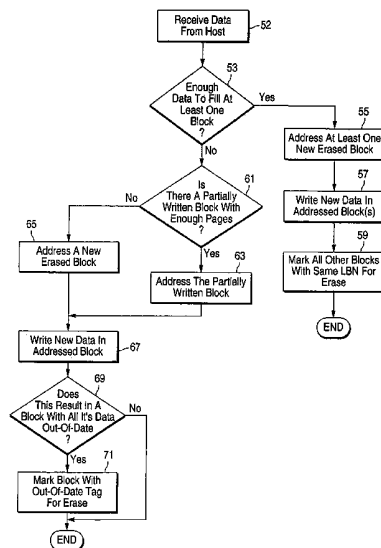
(58) **Field of Classification Search** **711/103**
See application file for complete search history.

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106 Claims, 9 Drawing Sheets



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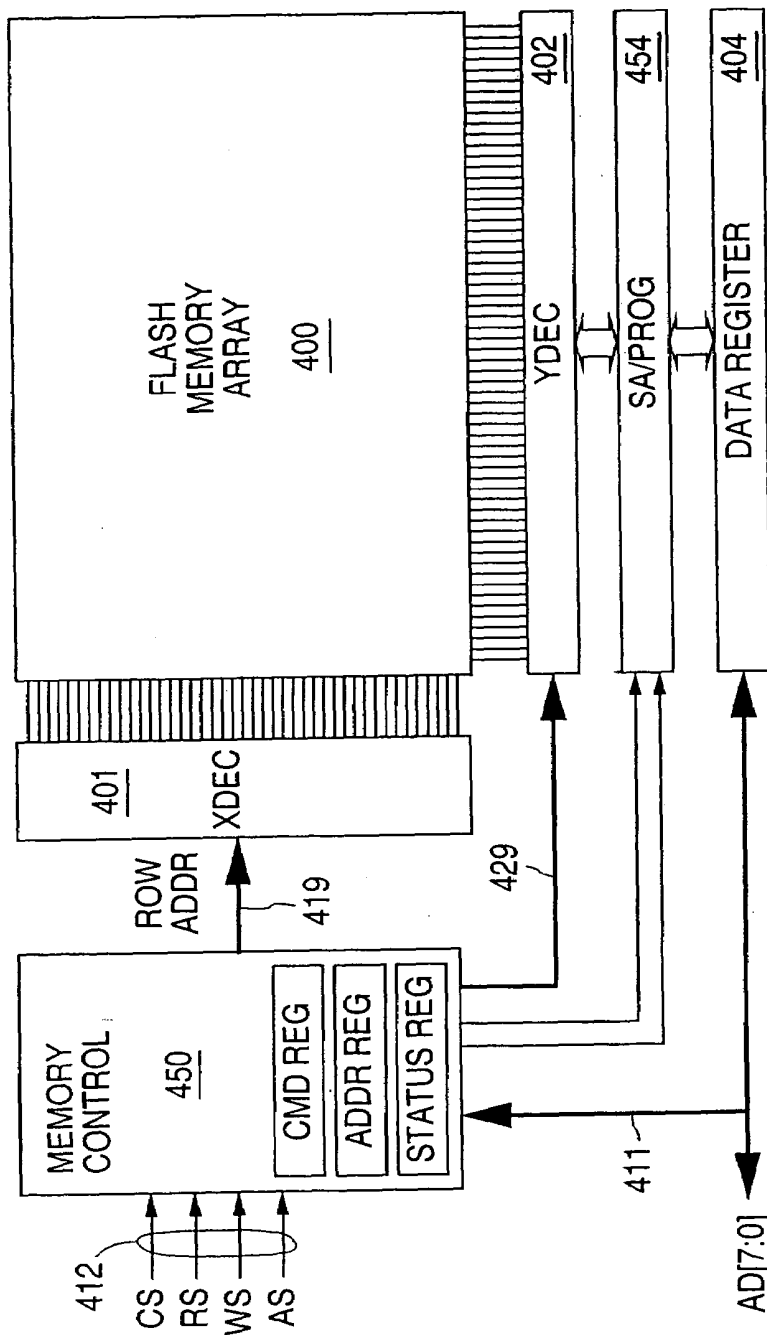


FIG. 1
(PRIOR ART)

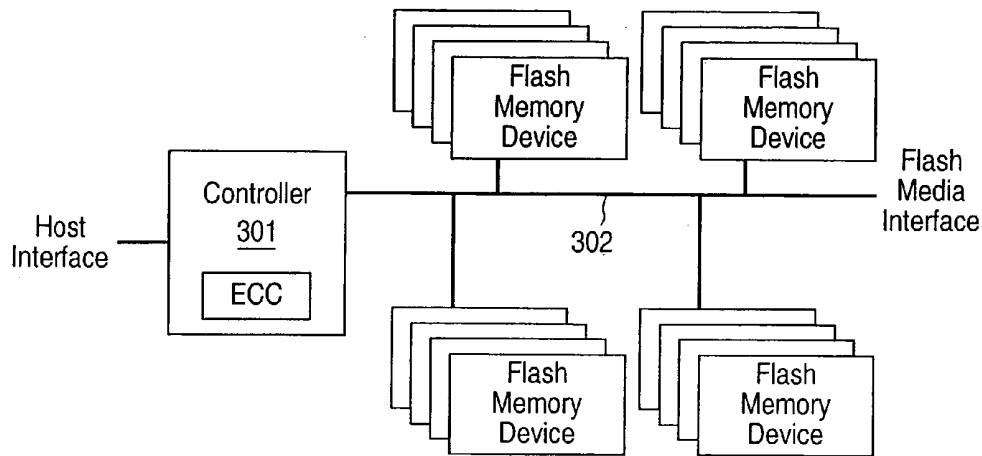


FIG. 2
(PRIOR ART)

LBN	PBN
0	0
⋮	⋮
⋮	⋮
⋮	⋮
⋮	⋮

Original Block 11

FIG. 5A

LBN	PBN
0	1
⋮	⋮
⋮	⋮
⋮	⋮
⋮	⋮

With New Block 15

FIG. 5B

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