PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicants | : | Jefferson Eugene Owen et al. |
| Application No. | : | 13/655,152 |
| Filed | : | October 18, 2012 |
| For | : | ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY |
| Examiner | : | Hau H. Nguyen |
| Art Unit | : | 2677 |
| Docket No. | : | 850063.553C8 |
| Date | : | September 3, 2013 |

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Commissioner for Patents:

In response to the Office Action dated April 1, 2013, please extend the period of time for response two months, to expire on September 1, 2013. Enclosed are a Petition for an Extension of Time and the requisite fee. Please amend the application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks** begin on page 5 of this paper.

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A computing device, comprising:

a central processing unit (CPU);

core logic coupled by a first bus to the CPU, the core logic having a first memory interface coupleable to a shared main memory;

a cache memory coupled to the CPU by the first bus;

a decoder/encoder coupleable to the shared main memory via a second memory interface;

an arbiter configured to receive shared memory access requests from the CPU and the decoder/encoder, the arbiter configured to arbitrate access to the shared main memory; and

a memory bus coupled to the first memory ~~controller~~ interface and the second memory ~~controller~~ interface, the memory bus configured to pass first data in real time between the shared main memory and the CPU via the first memory interface, the memory bus configured to pass second data in real time between the shared main memory and the decoder/encoder.

2. (Original) The computing device according to claim 1 wherein the computing device is a computer.

3. (Original) The computing device according to claim 1 wherein the core logic comprises:

a Peripheral Component Interconnect (PCI) core logic device.

4. (Original) The computing device according to claim 1 wherein the core logic comprises:

an Accelerated Graphics Port (AGP); and

an Enhanced Integrated Device Electronics (EIDE) interface.

5. (Original) The computing device according to claim 4, comprising:

a hard disk drive; and

an optical disk drive, wherein the hard disk drive and the optical disk drive are coupled to the core logic via the EIDE interface.

6. (Original) The computing device according to claim 1 wherein the memory bus is capable of having a bandwidth at least two times greater than the amount of data carried to the decoder/encoder when the decoder/encoder decodes in real time.

7. (Original) The computing device according to claim 6 wherein the memory bus is capable of carrying up to 400Mbytes/s.

8. (Original) The computing device according to claim 1 wherein the arbiter is coupled to the second memory interface and the arbiter and second memory interface are integrated with the decoder/encoder.

9. (Original) The computing device according to claim 1 wherein the decoder/encoder includes a DMA engine coupled to the second memory interface, the DMA engine configured to control data bursts between the decoder/encoder and the shared main memory via the second memory interface.

10. (Original) The computing device according to claim 9 wherein the DMA engine controls priority of data bursts between the decoder/encoder and the shared main memory via the second memory interface.

11. (Original) The computing device according to claim 1, comprising:

refresh logic coupled via a memory interface, the refresh logic configured to maintain the contents of the shared main memory.

12. (Currently Amended) The computing device according to claim 11 wherein the refresh logic, the arbiter, and the second memory ~~controller~~ interface are monolithically integrated into the decoder/encoder.

13. (Original) The computing device according to claim 4, comprising:

a graphics accelerator coupled to the core logic via an Accelerated Graphics Port (AGP) bus and a Peripheral Component Interconnect (PCI) bus; and

a local area network (LAN) controller coupled to the core logic via the PCI bus.

14. (Original) The computing device according to claim 13, comprising:

a frame buffer coupled to the graphics accelerator via a frame buffer memory bus; and

an audio codec coupled to the graphics accelerator.

15. (Currently Amended) The computing device according to claim ~~13~~ 14 wherein the frame buffer memory bus is memory bus coupled to the first memory ~~controller~~ interface and the second memory ~~controller~~ interface.

16. (Original) The computing device according to claim 13 wherein the graphics accelerator is configured to perform video scaling and color space conversions.

17. (Original) The computing device according to claim 1 wherein the decoder/encoder is a cell in an integrated circuit and the CPU is a cell in the integrated circuit.

## REMARKS

This communication is being filed in response to an Office Action having a mailing date of April 1, 2013. Claims 1, 12, and 15 are amended. No new matter is added, and all claims are believed in condition for allowance. Upon entry of the amendments herewith, claims 1-17 remain pending.

### I. Information Disclosure Statement (IDS)

An IDS submitted on December 28, 2012 was considered by the Examiner except for one reference to *Hsing*, "The Challenge of VLSI Technology to Low Bit Rate Video," pages 164-168 because there was no date or year provided.

The *Hsing* reference was published on pages 164-168 of VLSI Technology, Systems and Applications, 1989. Proceedings of Technical Papers from the 1989 International Symposium on May 17-19, 1989. A copy of the reference is resubmitted herewith along with an IDS providing a date of the reference and the requisite fee. It is kindly requested that an initialed copy of the IDS be provided with the next communication so as to confirm that the reference listed therein has been entered and considered.

### II. Telephone Interview Summary

A telephone interview was held between the attorney of record (Thomas J. Satagaj) and the Examiner on August 29, 2013. The substance of the interview is provided below:

Mr. Satagaj and the Examiner discussed certain cases in family of the present case, references applied in the present case, and certain features in the claims of the present case by telephone on August 29, 2013 in detail. The Examiner expressed a willingness to study the Remarks made herein and further consider the case upon submission of a formal written reply to the present final Office Action.

As discussed in detail herein, certain features of independent claim 1 are not disclosed in the applied references. Accordingly, it is respectfully submitted that independent claim 1 is patentable. Dependent claims 2-17 are patentably distinguished over the applied

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