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Wang

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[54] **PROCESS FOR FABRICATING A CONTROL GATE FOR A FLOATING GATE FET**

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[51] **Int. Cl.**[5] **H01L 21/336**

[52] **U.S. Cl.** **437/43**; 437/193; 437/200

[58] **Field of Search** .... 437/200, 43, 193, 192, 437/40, 41, 42, 50; 357/71, 67, 14; 148/DIG. 17, DIG. 147

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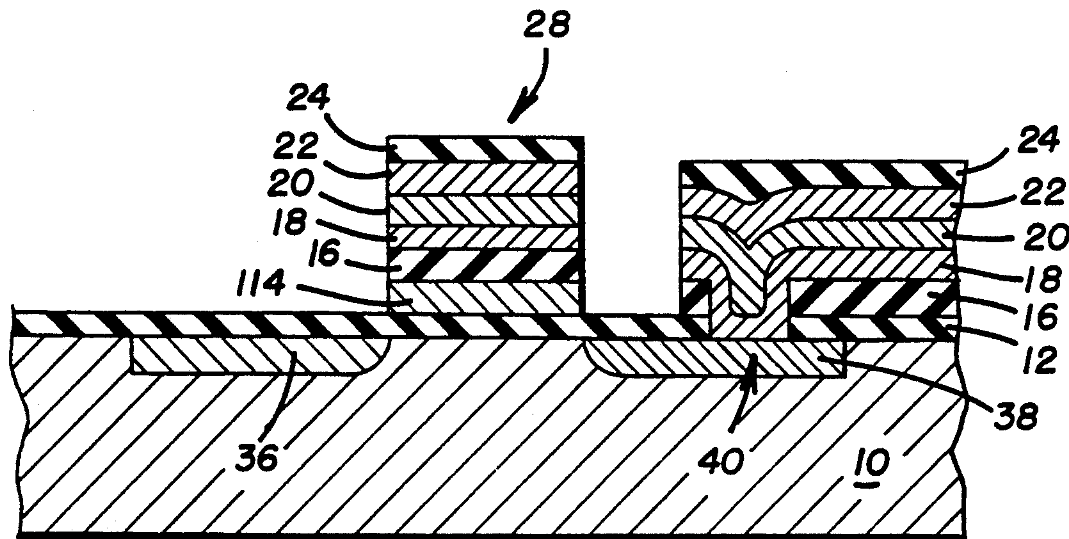
Attorney, Agent, or Firm—Fliesler, Dubb, Meyer & Lovejoy

[57] **ABSTRACT**

A process of forming a floating gate field-effect transistor having a multi-layer control gate line is disclosed. The multi-layer control gate line includes a first polysilicon layer, a silicide layer provided on the first polysilicon layer, and a second polysilicon layer provided on the silicide layer. The first and second polysilicon layers are formed as undoped polysilicon to improve the adhesion of the polysilicon layers to the silicide layers sandwiched therebetween. After all three layers are formed, the polysilicon layers are doped in an environment including $POCl_3$. Because the first and second polysilicon layers are formed as undoped layers, all three layers of the control gate line may be formed using a single pump-down.

15 Claims, 3 Drawing Sheets



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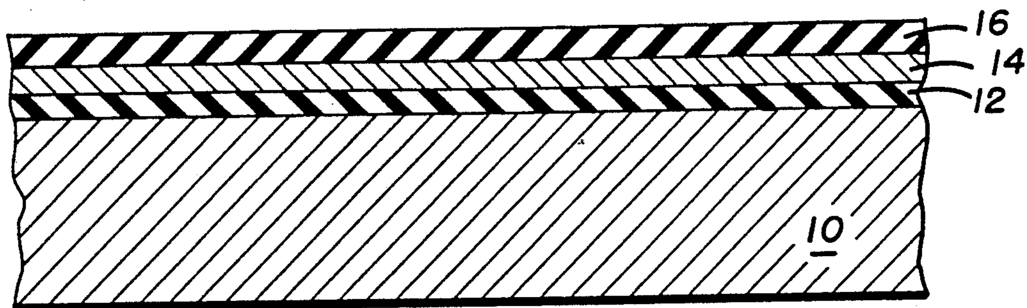

FIGURE 1

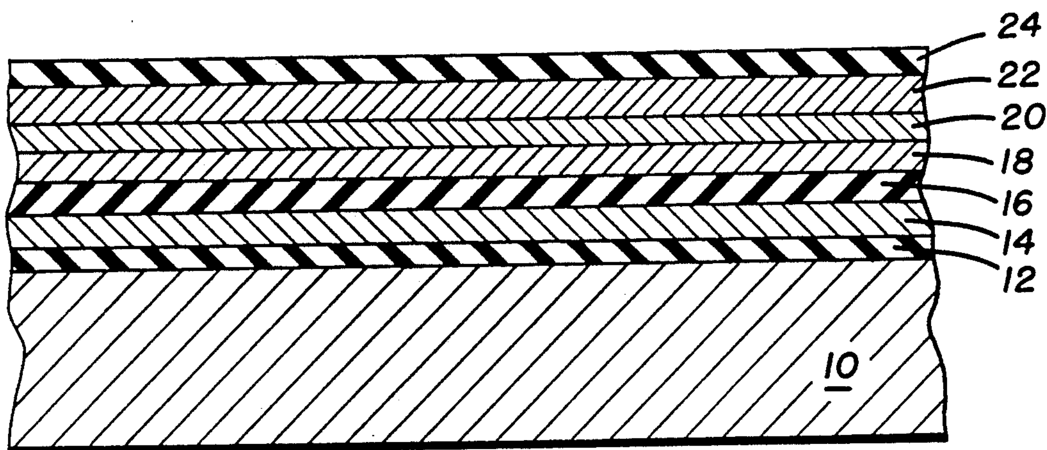

FIGURE 2

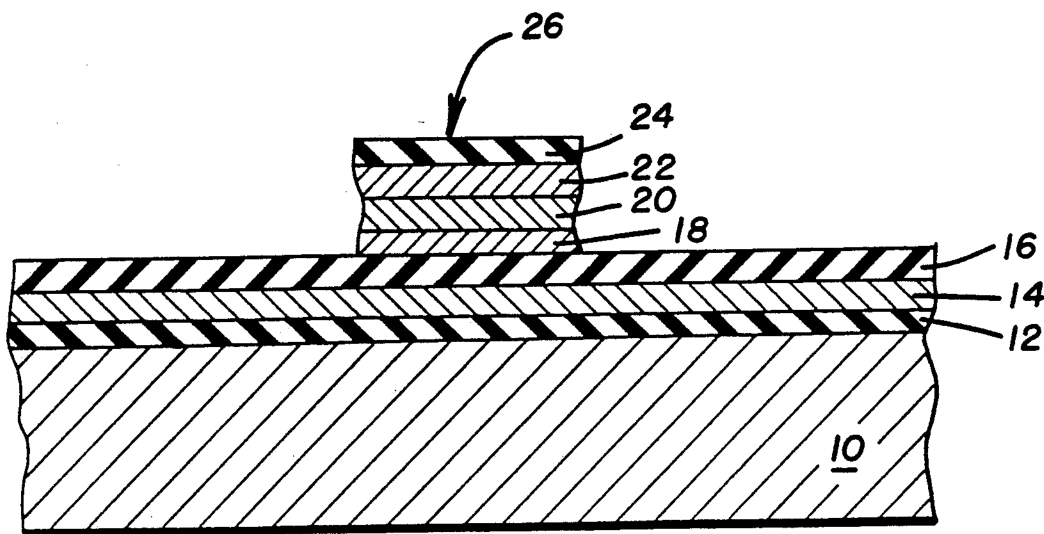

FIGURE 3

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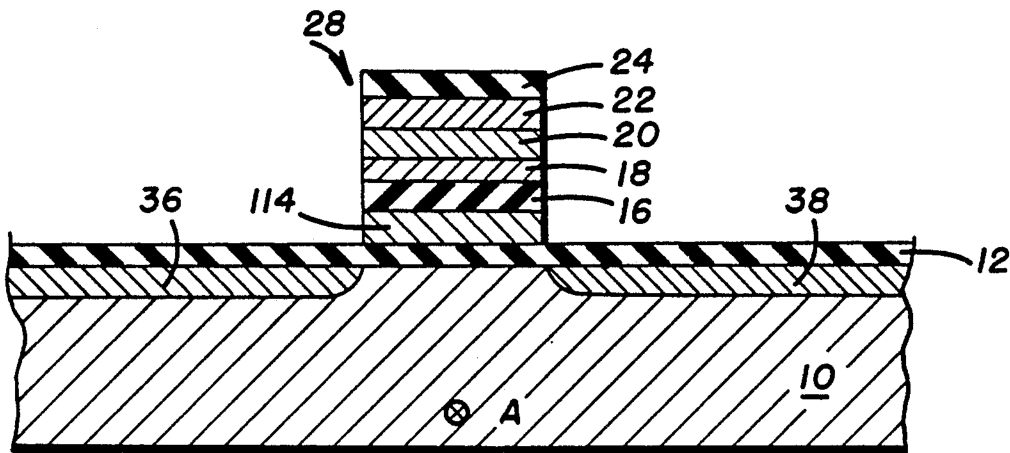

FIGURE 4

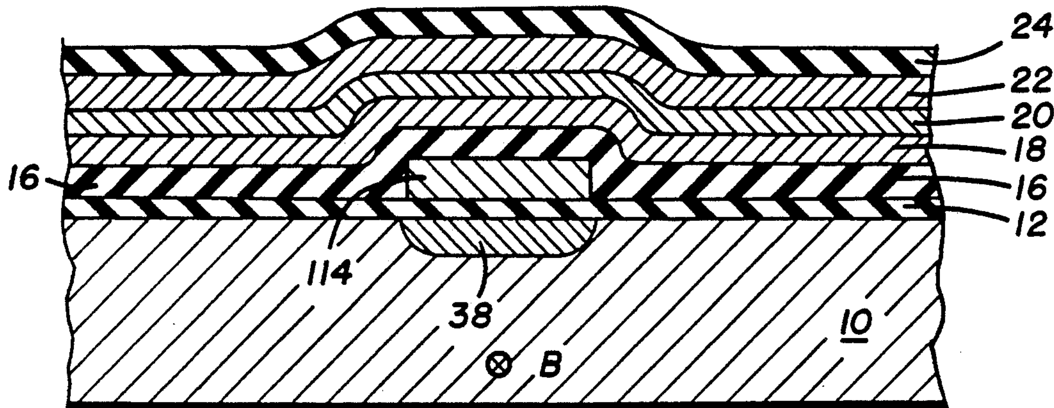

FIGURE 5A

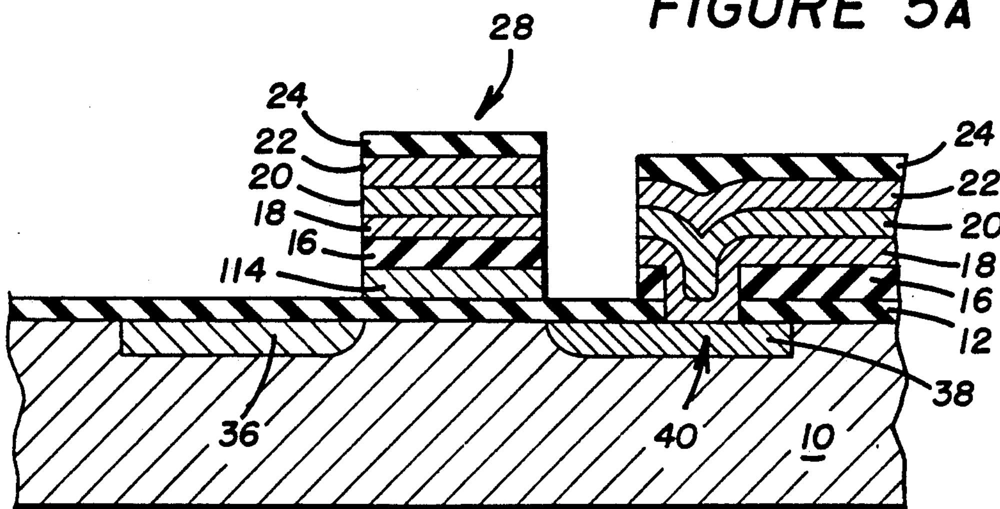

FIGURE 5B

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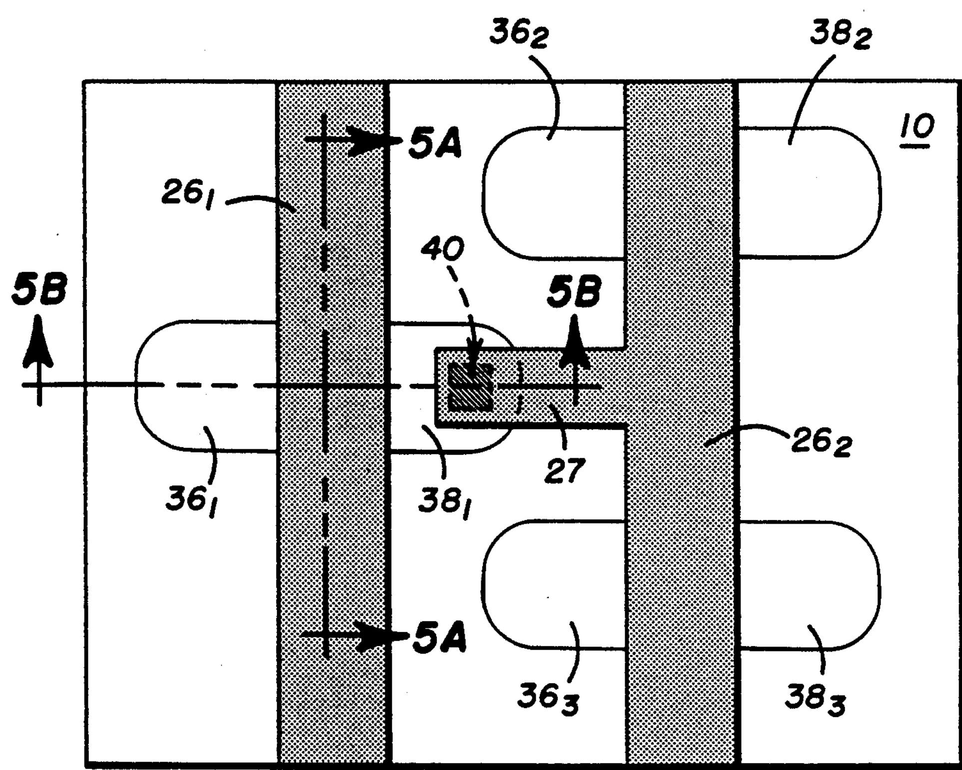

FIGURE 6

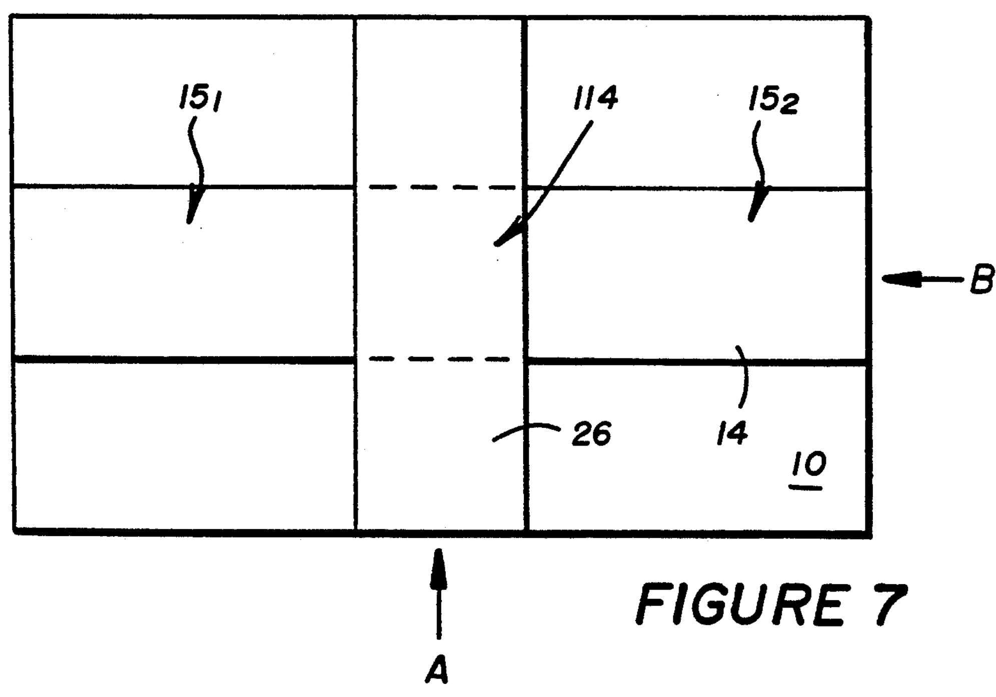

FIGURE 7

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PROCESS FOR FABRICATING A CONTROL GATE FOR A FLOATING GATE FET

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to processes for fabricating semiconductor devices; more particularly, processes for fabricating control gate lines for floating gate field effect transistors.

2. Description of the Related Art

The gate structure of a conventional floating gate field effect transistor (FET) includes a gate oxide layer provided on a substrate, a floating gate provided on the gate oxide layer, and a control gate separated from the floating gate by an inter-gate oxide layer. The control gate has conventionally been formed of a polysilicon layer or a polysilicon layer with a silicide layer overlying the polysilicon layer. The control gate is usually fabricated with a polysilicon layer adjacent to the inter-gate oxide in order to maintain the device characteristics provided by a polysilicon gate.

The desire to increase the speed and to reduce the power consumption of semiconductor devices has prompted the use of multi-layer structures, including a silicide layer overlying the polysilicon layer, to take advantage of the lower resistivity of the silicide. Several problems are associated with forming a silicide layer on a polysilicon layer. One such problem is that the doping level of the polysilicon must be low to insure that the silicide will adhere to the polysilicon. Poor adhesion results in silicide lift-off and device failure. Doping levels up to approximately 5×10^{19} cm^{-3} have been utilized; however, greater doping levels increase the probability of device failures beyond acceptable limits. Doping levels below 5×10^{19} cm^{-3} for the polysilicon layer create a large resistivity and power consumption and reduce speed. Further, since polysilicon is usually doped with an N-type dopant, in the fabrication of CMOS devices, the low doping level of the polysilicon layer allows P-type dopants (used to form the source and drain regions in P-channel devices) to neutralize, or invert, the doping (or conductivity type) of the polysilicon layer. An inversion of the conductivity of the polysilicon layer from N-type to P-type doping radically changes the threshold voltage (V_t) of the device.

A further problem associated with the formation of a multi-layer control gate is that the device must be removed from the furnace tube, or vacuum chamber, after the deposition of the polysilicon layer to allow the polysilicon layer to be doped before the silicide layer is deposited. Each time the device is removed from the furnace tube one of two problems arise. The cooling of the furnace tube to insert the wafers causes the polysilicon accumulated on the tube walls to warp or break the furnace tube due to the divergent coefficients of thermal expansion of polysilicon and quartz. Alternatively, if the tube is maintained at a high temperature and the wafers are inserted into a hot tube there is a high risk of wafer oxidation, even if a flow of an inert gas is provided, which causes yield problems.

The problem of oxidation is more severe if buried contacts are formed. Buried contacts require the removal of the inter-gate oxide and the gate oxide in the region where the buried contact is to be formed. This leaves the substrate exposed and oxidation of the substrate in the buried contact region as the wafer is inserted into a hot furnace tube will ruin a die.

SUMMARY OF THE INVENTION

It is therefore, an object of the present invention to provide an improved method of fabricating a floating gate field effect transistor.

A further object of the present invention is to provide a method of fabricating a floating gate FET having a multi-layer control gate including a highly doped polysilicon layer adjacent to the inter-gate oxide.

Another object of the present invention is to provide a method of fabricating a floating gate FET having a multi-layer control gate which improves the adhesion of a silicide layer to an underlying polysilicon layer.

Another object of the present invention is to provide a method of fabricating a multi-layer conductive line with a single vacuum chamber pump down.

A process for fabricating a floating gate field-effect transistor in accordance with the present invention comprises the steps of (a) providing a gate oxide on the substrate, (b) providing a floating gate line on the gate oxide, (c) providing an intergate oxide layer overlying the gate oxide and the floating gate line, (d) providing control gate layers, including a first undoped polysilicon layer overlying the intergate oxide layer, a silicide layer overlying the first polysilicon layer, and a second undoped polysilicon layer overlying the silicide layer, (e) annealing the control gate layers in an environment including $POCl_3$, (f) etching the control gate layers to form a control gate line, (g) etching the floating gate line using the control gate line as a mask to form a floating gate, and (h) implanting source and drain regions using the control gate line as a mask.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1–4** are cross-sectional views useful for describing the process of the present invention;

FIG. **5A** is a cross-sectional view along line **5A—5A** in FIG. **6** useful in describing the process of the present invention;

FIG. **5B** is a cross-sectional view along line **5B—5B** in FIG. **6** useful in describing an alternative embodiment of the process of the present invention;

FIG. **6** is a simplified plan view of a semiconductor device fabricated in accordance with the process of the present invention; and

FIG. **7** is a simplified plan view useful in describing the process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

The present invention will be described with reference to FIGS. **1–7**. The process of the present invention is particularly useful and is described below in the fabrication of floating gate field effect transistors. However, the process of the present invention is also applicable to the formation of any conductive line for a semiconductor device in either a bipolar or an MOS process. For example, the process of the present invention may be used to fabricate gate structures for non-floating gate field effect transistors or conductive lines for bipolar devices.

With reference to FIG. **1**, the process of the present invention begins with a substrate **10** which is thermally oxidized to form a gate oxide **12**. Alternatively, the gate oxide **12** may be a deposited oxide; however, thermal oxides are considered to be higher-quality oxides more

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