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1765  
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On July 23, 2003

By: Daniel L. Flamm

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Re-Issue Application of U.S. Patent  
No. 6,231,776 B1

Examiner: Anita K. Alanko

Art Unit: 1765

Application No.: 10/439,245

AMENDMENT

Filed: May 14, 2003

For: Daniel L. Flamm

Attn: Mail Stop Amendment  
Commissioner for Patents  
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Sir:

In response to the Office Action mailed Jan. 25, 2005, please enter the following amendments and remarks:

7/2005 MARDELRI 00000036 10439245 510.00 DP  
C:2253

IN THE SPECIFICATION:

Please amend the specification as follows:

At Col. 3, Par. 10:

Fig. 10 is a simplified ~~flow diagram of a heating~~ process according to the present invention.

At Col. 11, Par. 3:

Fig. 4 is a simplified diagram of a resist stripper according to the present invention. The present stripping apparatus includes similar elements as the previous described CVD apparatus. The present stripping apparatus includes a chamber 112, a feed source 114, an exhaust 116, a pedestal 118, which can be an agile temperature controlled chuck, an rf power source 122, a ground 124, a helical resonator 126, and other elements. The helical resonator 126 includes a coil 132, an outer shield 133, a wave adjustment circuit 400, and other elements. The chamber can be any suitable chamber capable of housing a product 119 such as a photoresist coated wafer for stripping, and for providing a plasma discharge therein. The plasma discharge is derived from a plasma source, which is preferably a helical resonator discharge or other inductive discharge using a wave adjustment circuit or other techniques to selectively adjust phase/anti-phase potentials. Of course, in some applications other configurations such as parallel plate capacitive discharges and microwave powered discharges such as electron cyclotron resonance machines, resonant cavities and slow ~~waver~~ wave applicator structures may also be suitable. The present stripping apparatus provides for stripping or ashing photoresist, e.g., implant hardened, etc. Further examples of such a stripping apparatus are described in the experiments section below.

At Col. 14, Par. 2:

Fig. 6 is a simplified block diagram of a substrate holder 600 according to the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The substrate holder 600 or ~~sueceptor~~ susceptor includes, among others, a lower or backside surface 608, which includes a plurality of concentric zones 608A, 608B, 608C, and 608D. In a specific embodiment, each of the zones can be in fluidic communication with each other and can be partly separated from each other. Each of the zones can have an inlet 613 and an outlet 611. Fluid enters the inlet, traverses in an annular manner in the zone, and leaves the

outlet. A baffle can separate the inlet from the outlet. Each of the zones can have an inlet and outlet, which are independent from the other inlets and outlets. Alternatively, the inlet and outlets can be in fluid communication with each other.

At Col. 15, Par. 3:

The substrate holder has an upper surface, which holds an object in a secure manner during processing. The upper surface is generally made of a suitable material that has desirable heat transfer characteristics. In a specific embodiment, the upper surface is made using a low thermal mass, high conductivity material. As merely an example, the upper surface can be a diamond-like or diamond film overlying a copper or copper-like substrate. Of course, the type of surface used depends upon the application.

At Col. 15, Par. 4:

In a specific embodiment, the substrate holder also has temperature sensing units 615 such as the one shown in "SIDE-VIEW C." The temperature sensing unit can be any suitable unit that is capable of being adapted to the upper surface of the substrate holder. Alternatively, the temperature sensing unit can measure the temperature of the fluid or lower surface of the substrate holder. As merely an example, the temperature sensing unit is a "fluoroptic" sensor unit made by a company called Luxtron in Santa Clara, California. Alternatively, the sensing unit can be a band edge IR sensor or the like. The sensing unit is capable of measuring a variety of spatial locations along the upper or lower surface of the substrate holder. The substrate holder can be implemented using a variety of systems for heating and/or cooling applications such as the one described below, but can be others.

At Col. 18, Par. 2:

Fig. 10 is shows a simplified ~~flow diagram of a heating~~ process according to the present invention. This ~~diagram~~ process is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, there is an isotropic breakthrough step during which an SF<sub>6</sub> plasma is used to remove very thin native oxide can be conducted at a low temperature such as room temperature. Ordinarily the breakthrough step is conducted at a high temperature. High temperatures have a serious disadvantage in that the etching rate of both oxide and tungsten silicide by SF<sub>6</sub> may be isotropic. Therefore the duration of the breakthrough step, especially if the native oxide layer is thin, must often be limited to a few seconds to avoid undesired

undercut. At low temperature the etching rate is slower and therefore the extent to which materials under the native oxide are etched is easier to control.

At Col. 19, Par. 1:

At the end of the room temperature breakthrough step, at time BB, the control program increases within several seconds to a higher steady state value at time B which, as shown in Fig. 10, is typically more than 99°C. The tungsten silicide is etched at this temperature until this layer is breached at random locations on the wafer. This endpoint is conveniently observed by a change in the slope of intensity of an optical light emission from the plasma such as optical emission at 530nm (point C in Fig. 10). The complete removal of the unmasked tungsten silicide areas is similarly signaled by a change in light emission such as that shown at point D (at time D all "patches" of the tungsten silicide are "cleared" from unmasked polysilicon areas; the signal begins to rapidly decrease at time D because at constant temperature, polysilicon consumes chlorine more rapidly than tungsten silicide (e.g. a faster etch rate) and optical emission at this wavelength originates from a chlorine species.

At Col. 19, Par. 2:

Since it is not practical to change chuck temperature, at this point the etch rate would increase rapidly. As a consequence it can often be difficult to detect and terminate the polysilicon etching step when the thin oxide layer is reached. Another problem associated with the use of a single temperature for both silicide and polysilicon layers is that chlorine etching processes often undercut (etch along the mask direction, sideways- e.g. the etch is partly isotropic) silicon at the elevated temperatures suitable for a low residue tungsten silicide etch. Therefore it is highly desirable and advantageous to reduce the etching temperature during the polysilicon etch. The wafer temperature is gradually reduced at point D in order to achieve a slower and more anisotropic polysilicon etching step. The temperature necessary to etch tungsten silicide and polysilicon during this temperature programmed sequence are schematically compared in Fig. 10. As shown, the ~~The~~ emission signal intensity increases when the temperature is lowered because the rate of consumption of chlorine species by the etching process is slowed (the rate decreases with decreasing temperature). Stopping the etch process beyond the endpoint where all of the silicon has "cleared," denoted by E is also easier and less critical because attack on the oxide has also slowed. Fig. 10 shows temperature changes between BB and B and between points D and E occurring over intervals which

subtend significantly less than 15 percent of the total stack etching time and well under 40 percent of the total process time.

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