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Muller et al.

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(54) **HIGHLY INTEGRATED MULTI-LAYER SWITCH ELEMENT ARCHITECTURE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 17 days.

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Primary Examiner—Dang Ton

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(51) **Int. Cl.**⁷ **H04L 12/56**

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(52) **U.S. Cl.** **370/389; 370/395; 370/412**

(57) **ABSTRACT**

(58) **Field of Search** 370/389, 428, 370/355, 356, 357, 359, 360, 362, 367, 372, 375, 379, 380, 328, 400, 401, 402, 465, 468, 418, 434, 395, 386, 396, 398, 408, 412, 419, 429

An architecture for a highly integrated network element building block is provided. According to one aspect of the present invention, a network device building block includes a network interface with multiple ports for transmitting and receiving packets over a network. The network device building block also includes a packet buffer storage which is coupled to the network interface. The packet buffer storage acts as an elasticity buffer for adapting between incoming and outgoing bandwidth requirements. A shared memory manager may also be provided dynamically allocate and deallocate buffers in the packet buffer storage on behalf of the network interface and other clients of the packet buffer storage. The network device building block further includes a switch fabric which is coupled to the network interface. The switch fabric provides forwarding decisions for received packets. A given forwarding decision includes a list of ports upon which a particular received packet is to be forwarded. A central processing unit (CPU) interface is also included in the network device building block. The CPU interface is coupled to the switch fabric and is configured to forward packets received from the CPU based upon forwarding decisions provided by the switch fabric.

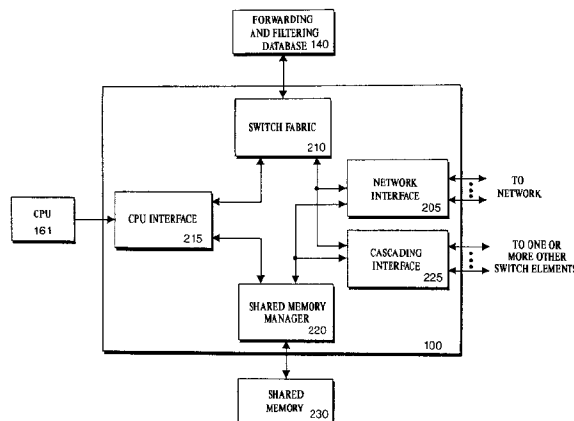
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12 Claims, 3 Drawing Sheets



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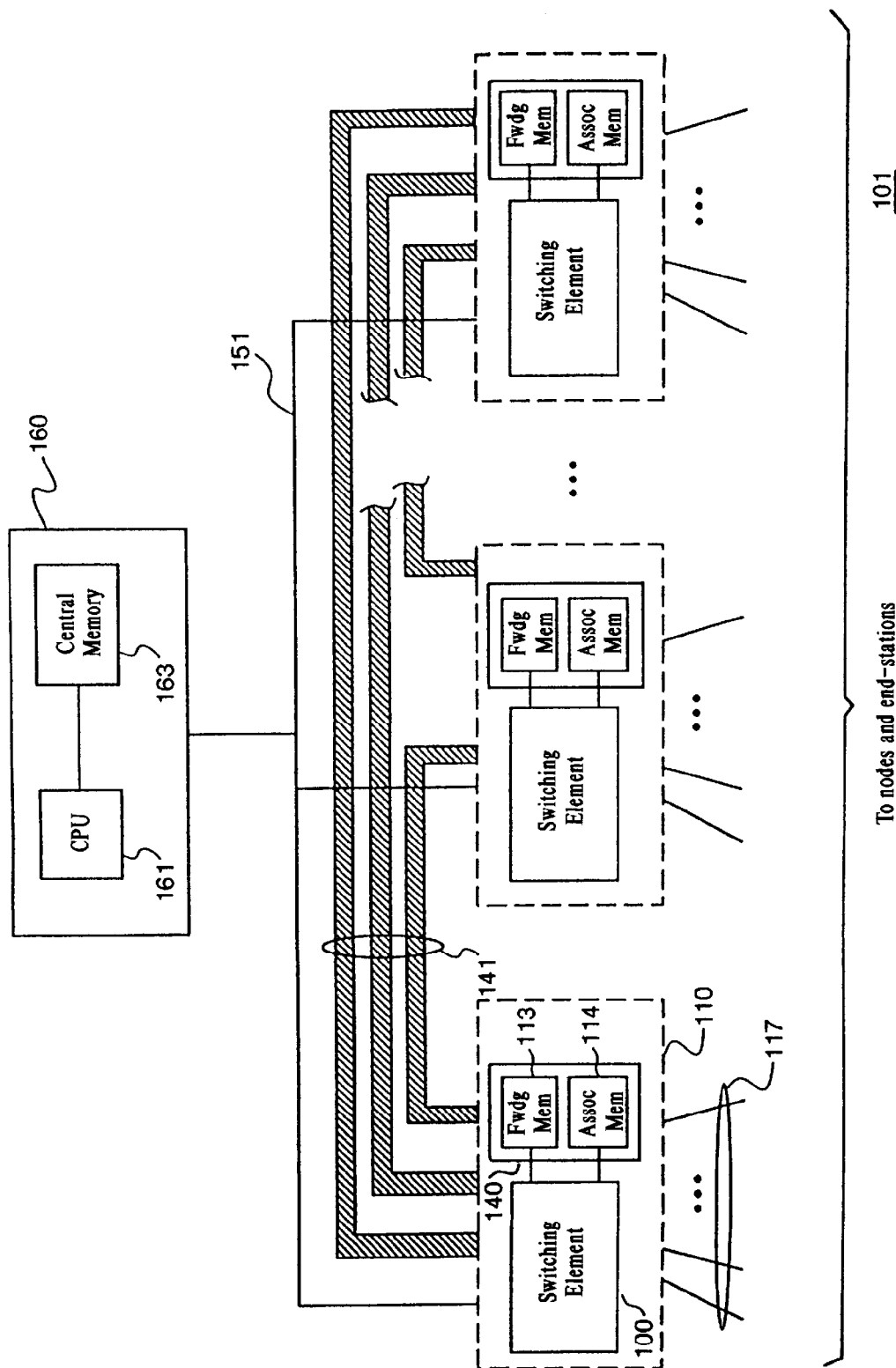
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To nodes and end-stations

FIG. 1

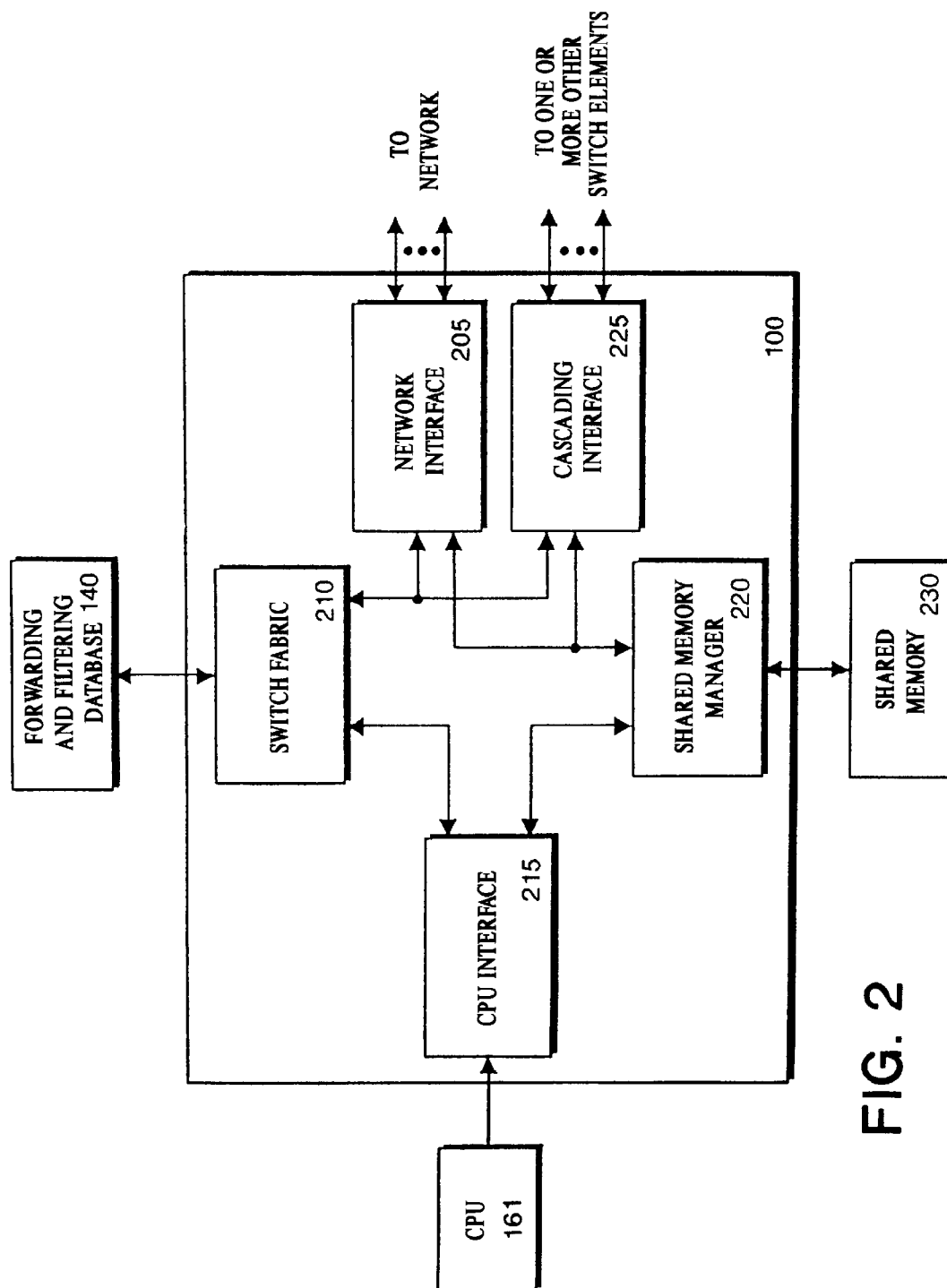


FIG. 2

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