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United States Patent [19]

Toda et al.

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[54] **SEMICONDUCTOR MEMORY DEVICE WITH CLOCK TIMING TO ACTIVATE MEMORY CELLS FOR SUBSEQUENT ACCESS**

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[21] Appl. No.: **912,071**

[22] Filed: **Aug. 15, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 720,309, Sep. 27, 1996, Pat. No. 5,737,637, which is a continuation of Ser. No. 427,270, Apr. 24, 1995, Pat. No. 5,587,963, which is a division of Ser. No. 223,222, Apr. 5, 1994, Pat. No. 5,500,829, which is a division of Ser. No. 775,602, Oct. 15, 1991, Pat. No. 5,313,437.

[30] **Foreign Application Priority Data**

Oct. 15, 1990 [JP] Japan 2-273170
Oct. 2, 1991 [JP] Japan 3-255354

[51] **Int. Cl.**[6] **G06F 13/16**

[52] **U.S. Cl.** **711/167**; 395/878; 365/185.09; 365/230.01

[58] **Field of Search** 711/167, 102, 711/104; 395/878; 365/185.09, 230.01

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Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

A semiconductor memory device comprises a memory cell group comprising a plurality of memory cells arranged in matrix; a specification circuit for specifying sequentially memory cells addressed by consecutive addresses in the memory cells, and for enterring them in an active state; a data input/output (I/O) circuit for performing a data read-out/write-in operation (data I/O operation) for the consecutive memory cells specified by the specification circuit under a control based on a read-out/write-in signal provided from an external section; a counter circuit for counting the number of cycles of a basic clock signal provided from an external section; and a controller for receiving at least one or more specification signals provided from an external section, for outputting a control signal per specification signal for specifying a particular cycle as a starting cycle to count the number of the cycles of the basic clock signal, and for instructing the counter circuit to count the number of counts of the basic clock signal based on the control signal, and for controlling a specification operation executed by the specification circuit and the data I/O operation of the data I/O circuit, so that the memory access operations for the memory cell group are controlled.

22 Claims, 18 Drawing Sheets

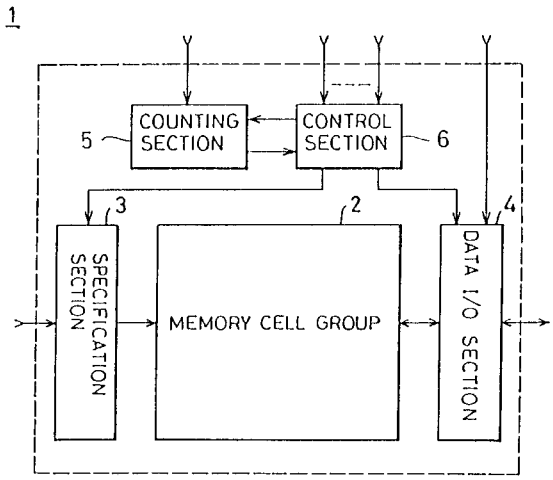

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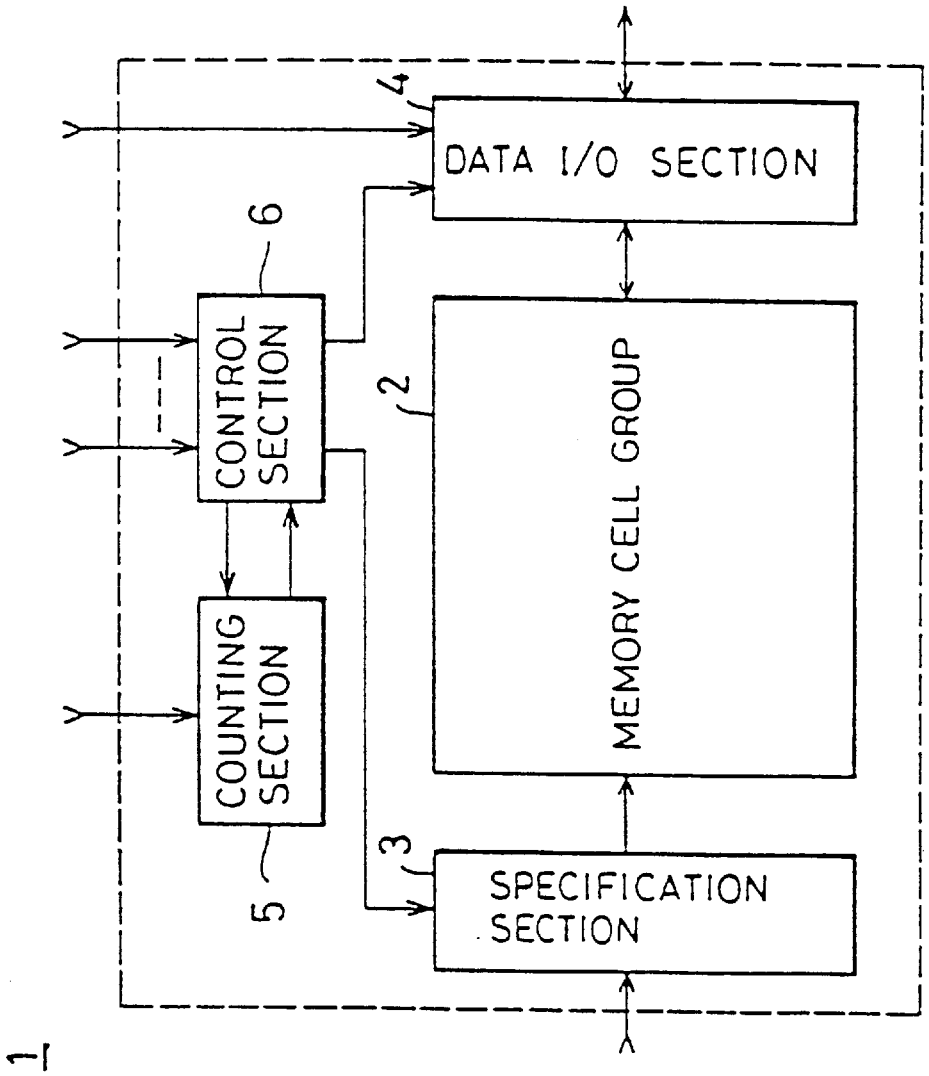
FIG. 1



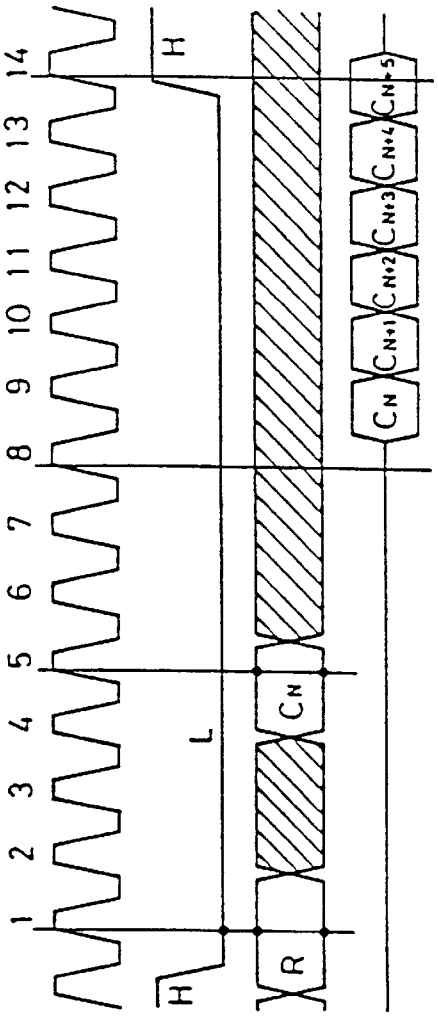


FIG. 2A BASIC CLOCK SIGNAL CLK

FIG. 2B CHIP ENABLE SIGNAL $\overline{CE}$

FIG. 2C Add

FIG. 2D DOUT/IN

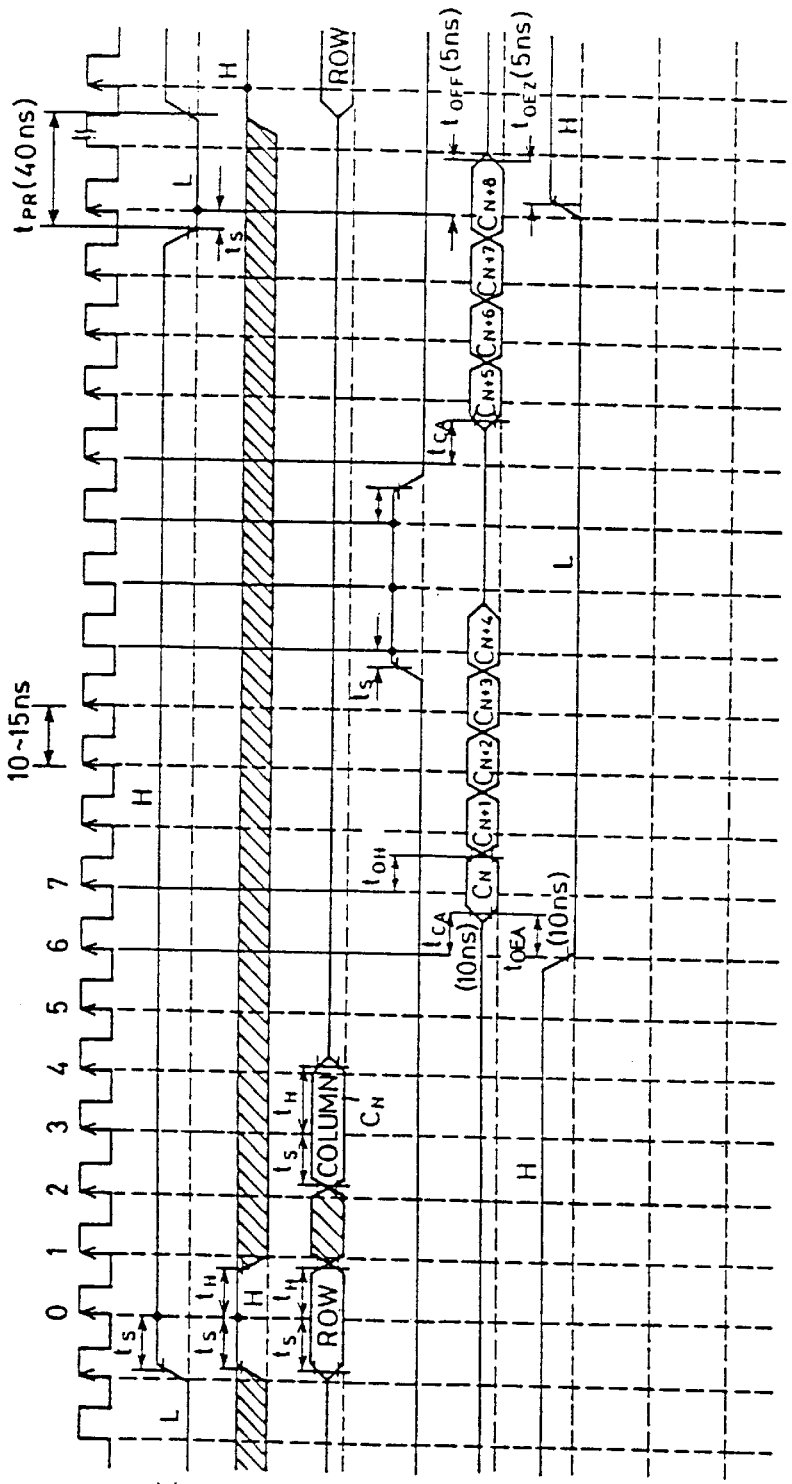


FIG. 3A FIG. 3B FIG. 3C FIG. 3D FIG. 3E FIG. 3F FIG. 3G

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