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SAMSUNG ELECTRONICS CO., LTD. Petitioner

v.

ELBRUS INTERNATIONAL LIMITED Patent Owner

Case: IPR2015-01524 U.S. Patent No. 6,366,130

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE



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LIST OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 6,366,130 ("the '130 Patent") to Podlesny et al.
1002	Declaration of Dr. R. Jacob Baker
1003	File History of the '130 Patent
1004	Excerpts from File History of the <i>Inter Partes</i> Reexamination of the '130 Patent
1005	U.S. Patent No. 5,828,241 to Sukegawa
1006	U.S. Patent No. 6,108,254 to Watanabe et al.
1007	U.S. Patent No. 6,249,469 to Hardee
1008	"Half-V _{DD} Bit-Line Sensing Scheme in CMOS DRAM's," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4, August 1984 by Lu et al.
1009	Excerpts from the Modern Dictionary of Electronics (7th ed. 1999)
1010	Excerpts from the IEEE Standard Glossary of Computer Hardware Terminology, IEEE Standard 610.10-1994 (1995)
1011	Deposition of William R. Huber, D.Sc.
1012	Fairchild Semiconductor, Application Note AN-600 Understanding Latch-Up in Advanced CMOS Logic, March 1998
1013- 1019	Reserved
1020	United States Patent 6,366,130, Samsung Exhibit 1001, with drawings by Dr. Huber
1021	U.S. Patent 5,828,241, Samsung Exhibit 1005, with drawings by Dr. Huber



1022	Declaration of William R. Huber, D.Sc., P.E. in Support of Patent Owner's Response to Petition
1023	United States Patent 6,366,130, Samsung Exhibit 1001, with drawings by Dr. Huber
1024	Handwritten drawing by Dr. Huber



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