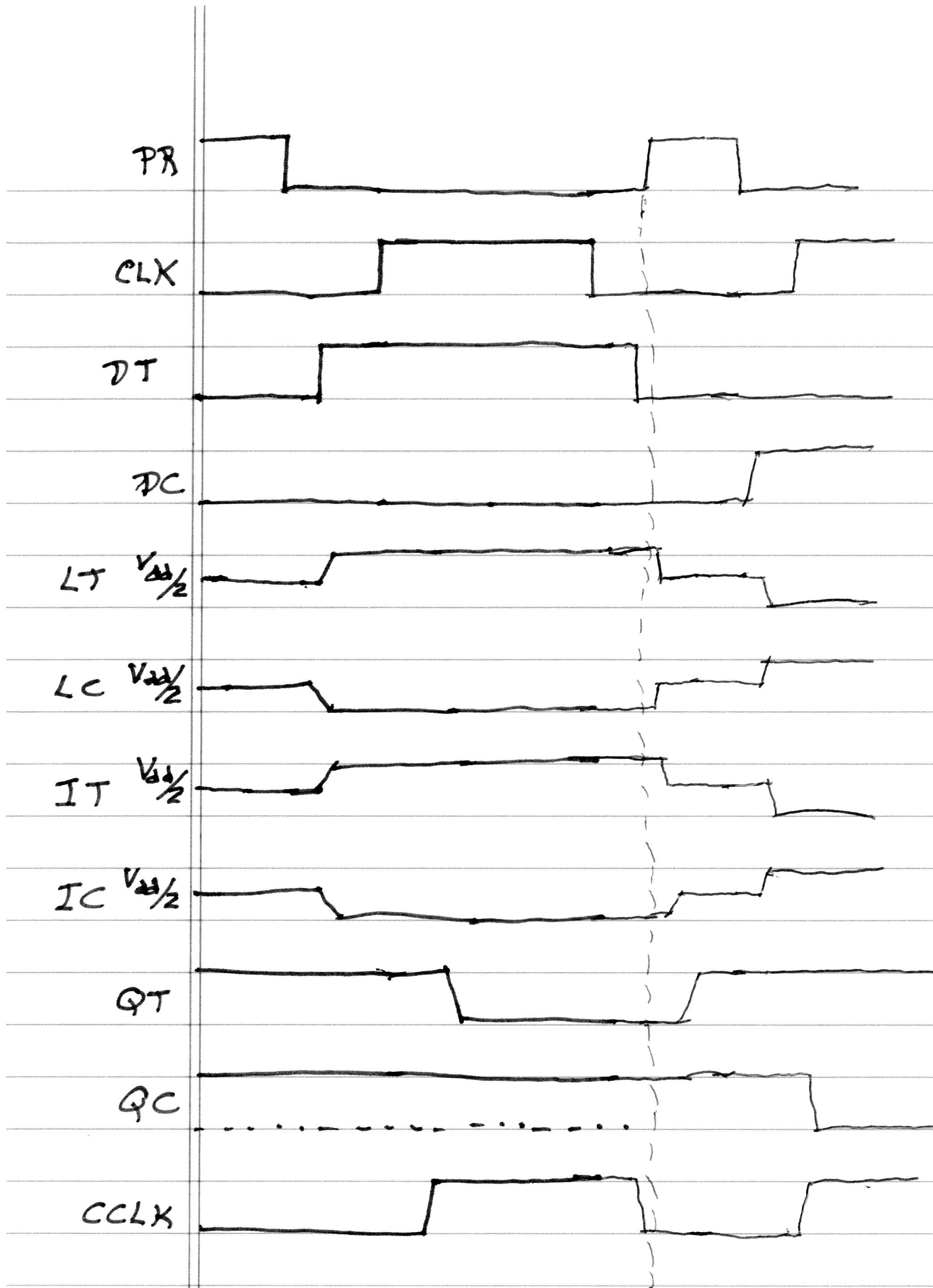

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Papers

Half-V_{DD} Bit-Line Sensing Scheme in CMOS DRAM's

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Abstract —A sensing scheme in which the bit line is precharged to half V_{DD} is introduced for CMOS DRAM's. The study shows that the half-V_{DD} bit-line sensing scheme has several unique advantages, especially for high-performance high-density CMOS DRAM's, when compared to the full-V_{DD} bit-line sensing scheme used for NMOS memory arrays or the grounded bit-line sensing scheme for PMOS arrays in CMOS DRAM's.

I. Introduction

In this paper a sensing scheme for CMOS DRAM's in which the bit line is precharged to half V_{DD} is introduced. The study shows that half-V_{DD} bit-line sensing has several unique advantages, especially for high-performance high-density CMOS DRAM's, when compared to the full-V_{DD} bit-line sensing scheme used for NMOS memory arrays or the grounded bit-line sensing scheme for PMOS arrays in CMOS DRAM's (n-well CMOS technology is assumed in this paper).

The half-V_{DD} bit-line sensing was used in early NMOS DRAM chips with 4 kbits [1]–[3]. One of the most widely used variants is shown in Fig. 1 [3]. The bit lines are precharged to a reference voltage approximately equal to $V_{DD}/2$, which can be obtained from a voltage regulator as suggested by Foss and Harland [3], or by shorting two bit-line halves after restoring the signal [1], [2]. After the sense latching clock Φ_S is activated, the load clock Φ_L is turned on, pulling up the high bit line to fully overdrive the cross-coupled latch and also to restore a full signal. After the 4 kbit NMOS DRAM generation, a 5 V-only V_{DD} power supply was widely adopted. Sensing was converted to full-V_{DD} bit-line precharge, sometimes with an active restore circuit, such as shown in Fig. 2 [4] or in Fig. 5 of [5], to obtain sufficient overdrive on the NMOS latch for higher speed and to restore the full signal. Half-V_{DD} bit-line sensing lost its importance in NMOS DRAM's because of the following disadvantages:

1) there is less overdrive on the NMOS latch, thus degrading the latching speed; and

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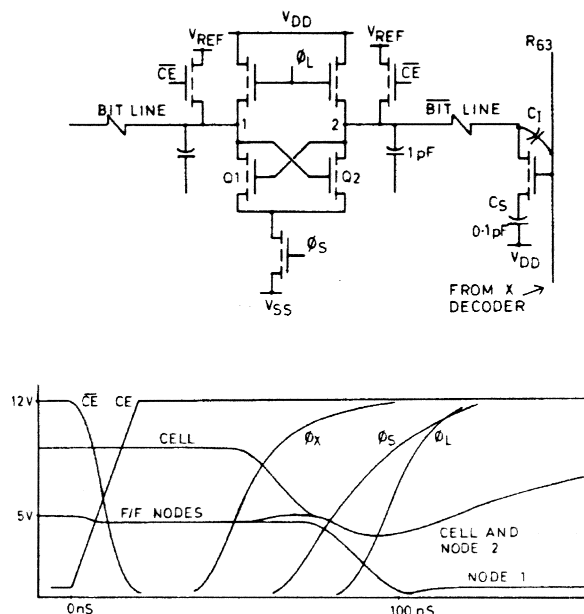

Fig. 1. Schematic of the NMOS half-V_{DD} bit-line sensing circuitry with associated timing signals [3].

2) for static pull-up loads [4], dc power is consumed on the low bit-line side. For an active restore circuit [5], the timing control is sensitive. Without pull-up circuits, only partial signal is restored and both sensing speed and sensitivity are degraded because of voltage droop at two sensing nodes, due to latch-device gate-capacitance coupling as latching speed is fast (Fig. 3).

Recently, CMOS is beginning to be used in DRAM designs. Advantages include decreasing the radiation-induced soft errors and isolating cells from substrate noise by putting the array in a well, reducing the number of clock generators in peripheral circuits, and obtaining lower standby power [6], [7]. For grounded-substrate n-well CMOS technology, an NMOS array may be difficult to use because minority carrier injection due to localized forward-biasing of junctions will cause destruction of stored

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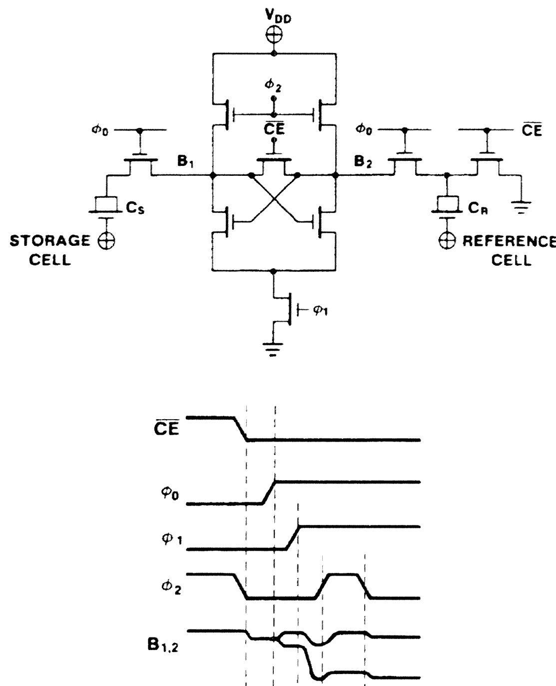

Fig. 2. Schematic of the NMOS V_{DD} bit-line sensing circuitry with associated timing signals [4].

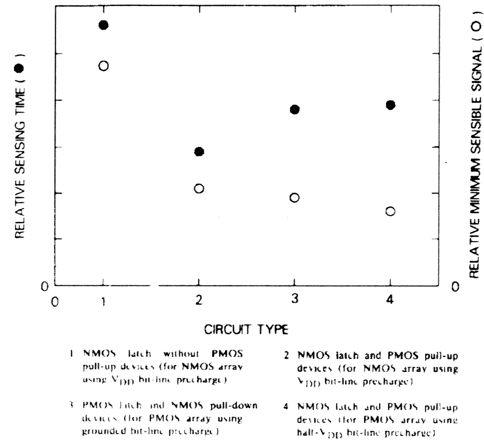

Fig. 3. Sensing speed[1] and minimum sensible signal[2] (both in normalized linear scale) for different cross-coupled sense amplifiers with device mismatches. Depletion NMOS decoupling transistors are used.

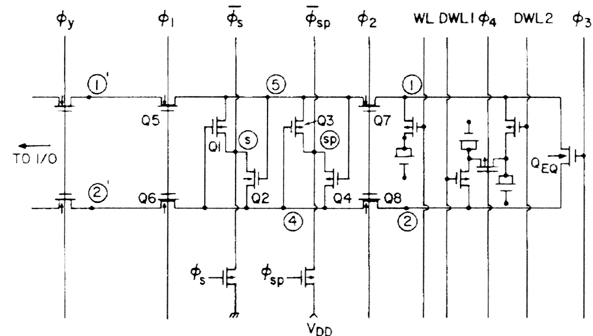

Fig. 4. Schematic of the CMOS half-V_{DD} bit-line sensing circuitry. Φ_1 and Φ_2 clocks are used for multiplexing bit lines. Φ_3 clock controls the equalization device and Φ_4 clock is used to establish the reference voltage. Φ_s and Φ_{sp} are complementary clocks to control the sense-amplifier latching. Φ_y is the column-selection clock.

information in the array [8].[1] If a PMOS array in the well is used, full-V_{DD} bit-line precharge is not desirable because it gives large junction capacitance and high sensitivity of the junction capacitance to voltage variation, which can increase sense-amplifier mismatch and any word-line noise can easily cause stored charge leakage. For grounded bit-line precharge, a PMOS cross-coupled latch must be used, which has slower sensing speed even when used with an NMOS restore circuit (Fig. 3). This is because the PMOS device has lower mobility and higher threshold voltage, since it is also used as cell transfer device.[2] In comparison, half-V_{DD} bit-line sensing gives almost the same speed for the latching operation, as shown in Fig. 3. Although the NMOS cross-coupled latch with PMOS restore circuit using V_{DD} precharge is fastest, the NMOS array may be difficult to use for grounded-substrate n-well CMOS technology.

II. CMOS Half-V_{DD} Bit-Line Sensing Circuitry

The proposed CMOS sense-amplifier circuitry for the half-V_{DD} sensing scheme using a PMOS memory array is shown in Fig. 4. It incorporates the following features: 1) a complementary sense amplifier consisting of NMOS and PMOS cross-coupled pairs, 2) clocked pulldown of the latching node, 3) complementary clocking of the PMOS pullup, 4) full-sized dummy cell generation of reference potential for sensing, 5) shorting transistor to equalize precharge potential of bit lines, and 6) depletion NMOS decoupling transistors for multiplexing bit lines (4 and 6 are not mandatory).

The operation of the circuit is described by the simulated waveforms in Fig. 5. At the end of the previous active cycle, one bit-line half is at V_{DD} and the other is at 0 V. A precharge of the bit line before sensing is initiated by switching on Φ_3 to turn on the equalization device Q_{EQ}, which shorts two bit-line halves together. The charge sharing between two bit-line halves results in a precharge level at nearly half V_{DD}. The reference voltage established on a full-size dummy cell is obtained by activating Φ_4 to turn on Q_{DS} for charge sharing between two dummy cells (Q_{D1}

[1]Applying a substrate bias in n-well CMOS has the advantages of relaxing the constraints of junction forward-biasing and latchup, decreasing the junction capacitances, and reducing the substrate sensitivity of the threshold voltage, thus allowing high-performance peripheral circuits. If the system solution to the soft error problem is acceptable to the memory applications [9], use of an NMOS array may be considered due to some superior device characteristics.

[2]Unless an extra mask plus ion-implantation is used to generate a second PMOS threshold voltage.

[1]Time for a differential signal of 0.3 V to be amplified to 2.5 V across two bit-line halves.

[2]High-performance design.

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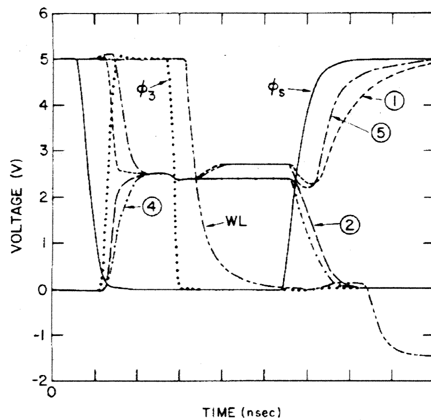

Fig. 5. Simulated waveforms for the CMOS half-V_{DD} sensing circuitry. Refer to Fig. 4 for node numbers.

and Q_{D2}), one having a stored high and the other a stored low level. READ can be performed by selecting a word line and the corresponding dummy word line (DWL1), which establishes a differential signal on the two sensing nodes (4 and 5) of the flip-flop pair. The worst-case charge transfer is to read the stored low level or 0 V, which starts after the word line is pulled down to $(V_{DD}/2)-|V_{TP}|$, where V_{TP} is the PMOS threshold voltage. The stored charge is fully transferred to the bit line without threshold loss even if the word line is not boosted. The word-line boosting can be used subsequently for restoring the full signal (0 V) into the cell and does not delay the read access time.

To amplify the signal, the NMOS cross-coupled pair (Q_1 and Q_2) and the PMOS cross-coupled pair (Q_3 and Q_4) are switched on by Φ_s and its complementary signal Φ_{sp}, respectively. The NMOS latch gives fast initial sensing. The PMOS cross-coupled pair pulls up the high bit-line-half to give full overdrive on the latch and full signal for restoring. The PMOS cross-coupled pair also pulls up the voltage droop at the high sensing node (5 in Fig. 5) due to the gate capacitance of the NMOS cross-coupled transistors, which can seriously degrade the sensitivity of the sense amplifier, especially for high performance. To activate a PMOS cross-coupled latch in the grounded bit-line sensing scheme, the latching node charges from 0 to 5 V; however, the half-V_{DD} sensing is activated by discharging the latching node only from $V_{DD}/2$ to 0 V, thus reducing the voltage droop at the two sensing nodes. Since half-V_{DD} is close to the switching point of both the NMOS and PMOS cross-coupled pairs, the active pullup of the drooping voltages at two sensing nodes by the PMOS cross-coupled pair is more effective. As a result, the sensitivity of the sense amplifier is also improved (Fig. 3).

III. FEATURES OF HALF-V_{DD} BIT-LINE SENSING

As mentioned earlier, the half-V_{DD} bit-line sensing gives almost the same latching speed as grounded bit-line sensing, as shown in Fig. 3, because NMOS devices are used in the sensing latch and the PMOS cross-coupled pair can effectively avoid the voltage droop on the two sensing nodes and also supplies sufficient overdrive. Also, for half-V_{DD} bit-line sensing, the stored charge can be fully transferred onto the bit lines during the read cycle without boosting the word line. If a boosted word line is used to store a full-level charge into the cell, the boosted level is needed only during the restore period, thus causing no extra delay during read access due to boosting. This makes the word line boosting attractive using the half-V_{DD} sensing scheme. By comparing the speed of a complete charge transfer from the memory cell to the bit lines, the half-V_{DD} sensing scheme has a much faster rate than the grounded bit-line sensing scheme because the complete transfer can start when the word line is pulled down to one $|V_{TP}|$ below $V_{DD}/2$ rather than being boosted down below 0 V in the grounded bit-line sensing scheme. As a result, the elapsed time from word-line activation to turning on the bit switch is faster in the half-V_{DD} bit-line sensing scheme.

In addition, the NMOS cross-coupled pair and the PMOS cross-coupled pair form a complementary pair, which does not have dc power dissipation and can be clocked simply.

In CMOS DRAM's, therefore, half-V_{DD} bit-line sensing has none of the disadvantages which it has when used in NMOS DRAM's and also shows advantages in comparison to the grounded bit-line sensing scheme. It has other additional advantages, which are very important for high-density high-performance DRAM design:

1) Reduces the peak currents at both sensing and bit-line precharge by almost a factor of two due to the half-V_{DD} swing, which reduces the electromigration problem and the IR drop. The chip reliability can be increased and the resulting narrower metal lines decrease the parasitic wiring capacitances thus giving better speed.

2) Reduces the dI/dt by a factor of two during bit-line precharge and discharge if the time is fixed, which decreases the voltage bouncing noise due to wiring inductance. If the voltage bouncing is not the limit, the precharge and discharge time can be shortened by a factor of two.

3) Reduces the ac power for charging and discharging the bit lines because the precharge voltage is obtained by charge sharing between the two bit-line halves instead of charging bit lines to V_{DD}.

4) At sensing and bit-line precharge in half-V_{DD} sensing, the pullup and pulldown of bit lines are balanced and have only half-V_{DD} swing. By using folded bit lines, coupled noises due to bit-line swing to the memory cell plate, the array substrate, and word lines can be largely reduced due to local cancellation. This also relaxes the requirement of using a low-impedance cell plate. Even if the plate has voltage bumping (for example, write at high plate voltage and read at low plate voltage), there will be no significant signal loss because the cell transfer device is operated in the linear region in half-V_{DD} sensing. In contrast, in grounded bit-line sensing, only one of the two segments of bit lines is pulled up (at sensing) or down (at precharge) by full-V_{DD}, which gives much larger coupling noises. The signal loss due to plate voltage bumping is also larger because the cell transfer device is operated in the saturation region.

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The only drawback may be a longer period of bit-line floating such that the bit-line precharge levels can be perturbed to cause mismatch due to radiation noise, substrate noise, and leakage effects. However, studies show that this is tolerable by using the following design approach, some of which is unique to CMOS technology:

1) Use folded metal bit lines to minimize the noise mismatch between two halves and also to minimize the junction area which reduces the leakage, substrate noise, and radiation noise.

2) Use a PMOS array in an n-well such that the p^+–n junctions are protected by the n-well. This reduces the leakage current, the substrate noise, and radiation-induced soft error rates.

3) Keep the bit-line equalization device on until just before the word-line activation. Differential noises occurring on a bit-line half during precharge will be distributed over the two halves in a common mode to minimize mismatch. The noise distribution is fast because the metal bit line gives very small resistance. For example, if a PMOS equalization device has $W/L = 4\ \mu m/1.2\ \mu m$ and each bit-line half has 200 fF, a 500 nA 10 ns square-pulse noise gives less than 3 mV mismatch noise which decays with a time constant of 2 ns.

4) Use a dummy cell to generate the reference potential so that the absolute bit-line precharge level and the word-line to bit-line coupling noise causing sensing signal mismatch are not crucial at least to first-order.

5) Use distributed refresh to shorten the time of bit-line floating at chip standby.

VI. Conclusion

The use of a half-V_{DD} bit-line sensing scheme in CMOS DRAM's has been described. It shows several advantages over the grounded bit-line sensing schemes used in existing CMOS DRAM's. The half-V_{DD} sensing has not been employed in NMOS DRAM's with chip density larger than 16 kbits; however, in CMOS DRAM's, the following advantages have been demonstrated:

1) Comparable sensing speed with better sensitivity of sense amplifier.

2) Complete charge transfer can be read from the cell without word-line boosting provided that $|V_{TP}|$ is less than $V_{DD}/2$ minus the sensing signal which depends on the charge transfer ratio.

3) Faster when compared to the word-line boosting scheme to read full signal.

4) Delayed word-line boost for full-signal restoring gives no penalty on read speed.

5) Smaller peak currents at both sensing and bit-line precharge.

6) Smaller ac power consumption for bit-line charge and discharge.

7) Smaller dI/dt, thus smaller bouncing noise due to wiring inductance.

8) Smaller coupling noises to the cell plate, the array substrate, and word lines because of balanced bit-line swing.

9) Less signal loss due to cell-plate voltage bumping.

Acknowledgment

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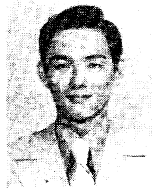

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