UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

ELBRUS INTERNATIONAL LIMITED
Patent Owner

Case: IPR2015-01524
U.S. Patent No. 6,366,130

DECLARATION OF WILLIAM R. HUBER, D.Sc., P.E. IN SUPPORT OF PATENT OWNER'S RESPONSE TO PETITION

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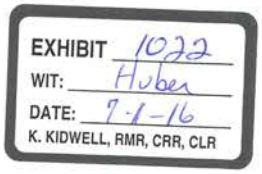

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I. Executive Summary

1. This Declaration is in support of patent owners in *inter partes* review before the Patent Trial and Appeal Board of U.S. Patent 6,366,130 to Podlesny et al.

2. The Board has decided to institute review with respect to the following grounds:

A. Whether independent claim 1 and dependent claims 2, 5, 6, and 9 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of U. S. Patent 5,828,241 to Sukegawa and Lu JSSC;

B. Whether dependent claim 3 is unpatentable under 35 U.S.C. § 103 as obvious over the combination of Sukegawa, Lu, and U. S. Patent 6,108,254 to Watanabe; and

C. Whether dependent claim 7 is unpatentable under 35 U.S.C. § 103 as obvious over the combination of Sukegawa, Lu, and U. S. Patent 6,249,469 to Hardee;

3. Evidence detailed in this Declaration demonstrates that

A. Regarding Issue A above:

1) The combination of Sukegawa and Lu fails to disclose or suggest the differential data bus required by claim 1.

2) The combination of Sukegawa and Lu fails to disclose or suggest precharging the nodes identified as the differential data bus to a voltage Vpr between Vdd and ground, as required by claim 1.

3) Modifications to Sukegawa and Lu necessary to provide precharging of the nodes identified as the differential data bus to the required voltage would not have been obvious to one of ordinary skill in the art at the time of the invention of the '130 patent.

4) The combination of Sukegawa and Lu fails to disclose or suggest the following elements required by claim 5: "logic high voltage" and "logic low voltage."

B. Regarding Issue B above:

1) The combination of Sukegawa, Lu and Watanabe fails to disclose or suggest the following requirement stated in claim 3: "…wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass transistors is coupled to an input…".

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