(12) **United States Patent**

Hardee

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(54) **SENSE AMPLIFIER WITH LOCAL SENSE DRIVERS AND LOCAL READ AMPLIFIERS**

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(22) Filed: **Jul. 1, 1996**

Related U.S. Application Data

(63) Continuation of application No. 07/976,312, filed on Nov. 12, 1992, now abandoned.

(51) Int. Cl.^{7} **G11C 7/00**

(52) U.S. Cl. **365/205**; 365/208; 365/189.05

(58) Field of Search 365/205, 207, 365/208, 189.05, 189.01

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(57) **ABSTRACT**

A sense amplifier for a very high density integrated circuit memory using CMOS technology is described. Each sense amplifier includes first and second local sense amplifier drive transistors, one connecting the P channel transistors to VCC; the other connecting the N channel transistors to VSS. A read amplifier circuit is provided within each sense amplifier and is operated by read control signals. Internal nodes of the latch of the sense amplifier are coupled by pass transistors that are responsive to column write control signals. Local data write driver transistors are also provided to selectively couple the pass transistors to VCC-Vt or VSS in response to further data write control signals. A relatively wider power line is coupled to the drive transistors to provide VCC thereto, and a narrower line is used to control those first sense amplifier drive transistors. Corresponding wide and narrow lines are used for the second local sense amplifier drive transistors which couple the N channel transistors to ground. Each sense amplifier may be shared between first and second pairs of bit lines through the use of isolation transistors and a corresponding isolation signal.

22 Claims, 7 Drawing Sheets
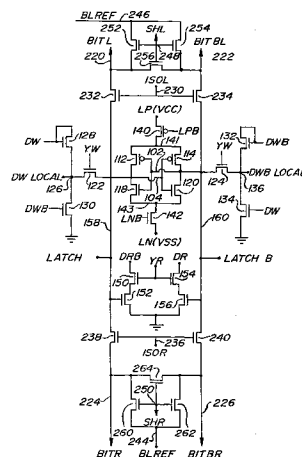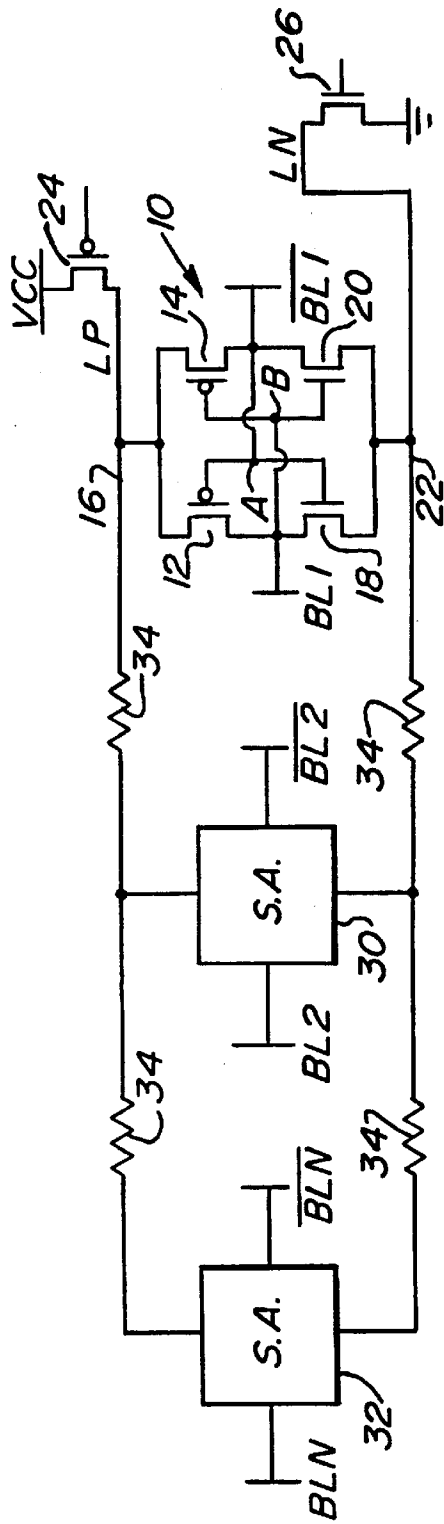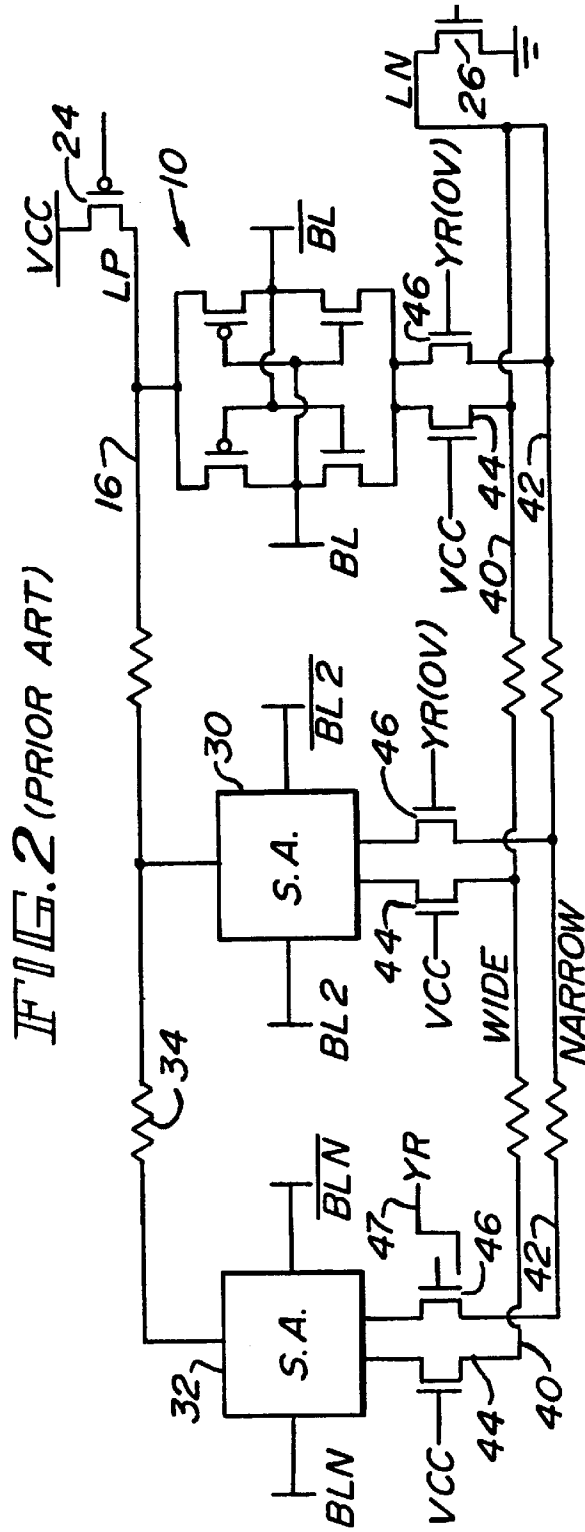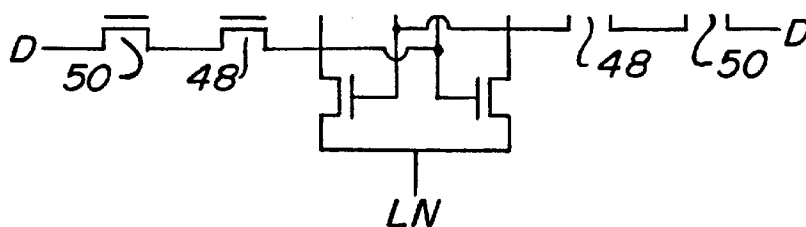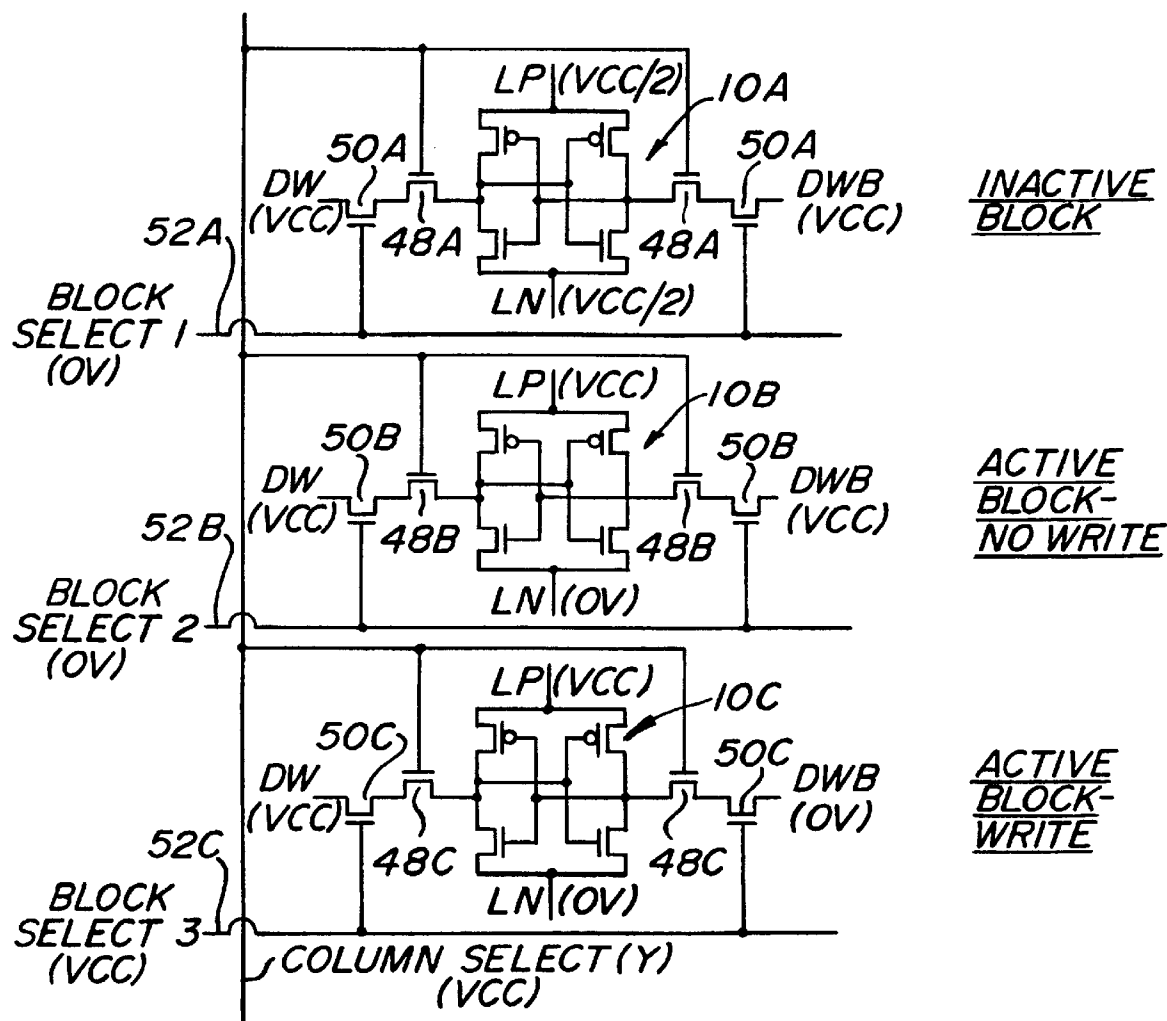
FIG.1 (PRIOR ART)

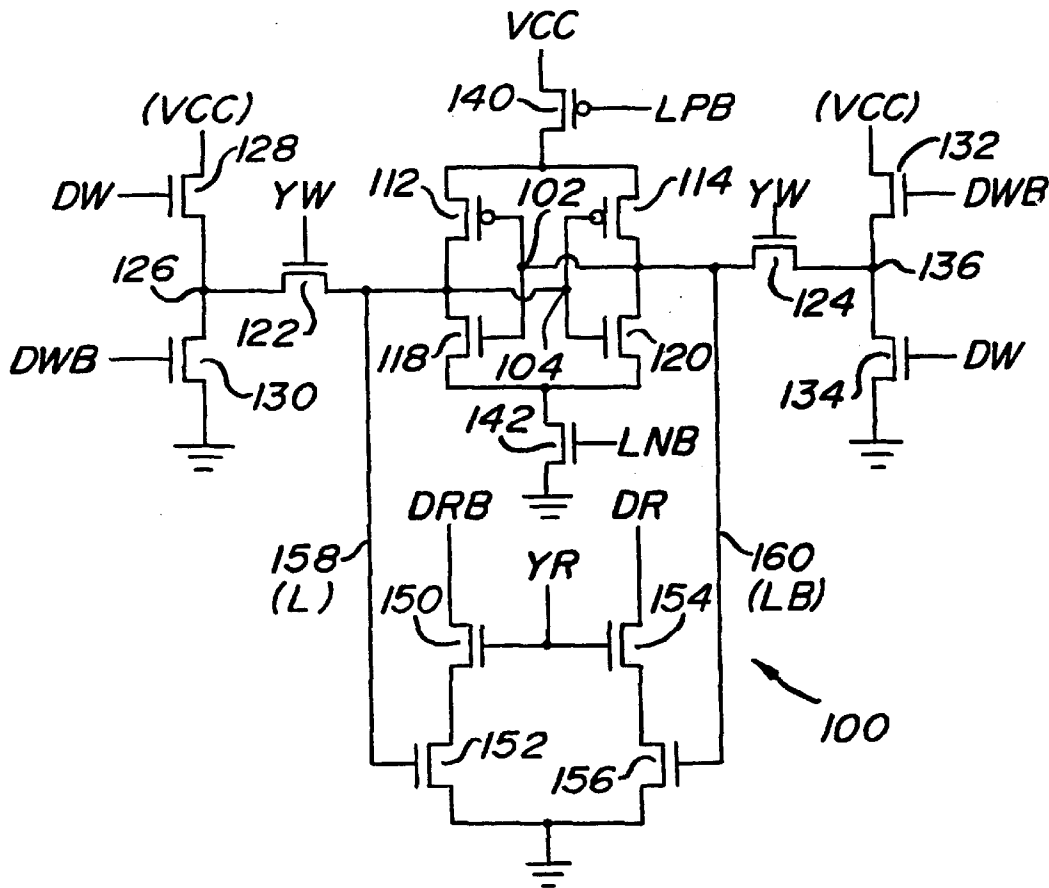FIG.2 (PRIOR ART)

FIG. 3 (PRIOR ART)

FIG. 4 (PRIOR ART)

FIG.5

FIG.6

FIG.7

INACTIVE BLOCK

ACTIVE BLOCK— NO WRITE

ACTIVE BLOCK— WRITE

COLUMN SELECT YW (VCC)

DOCKET ALARM
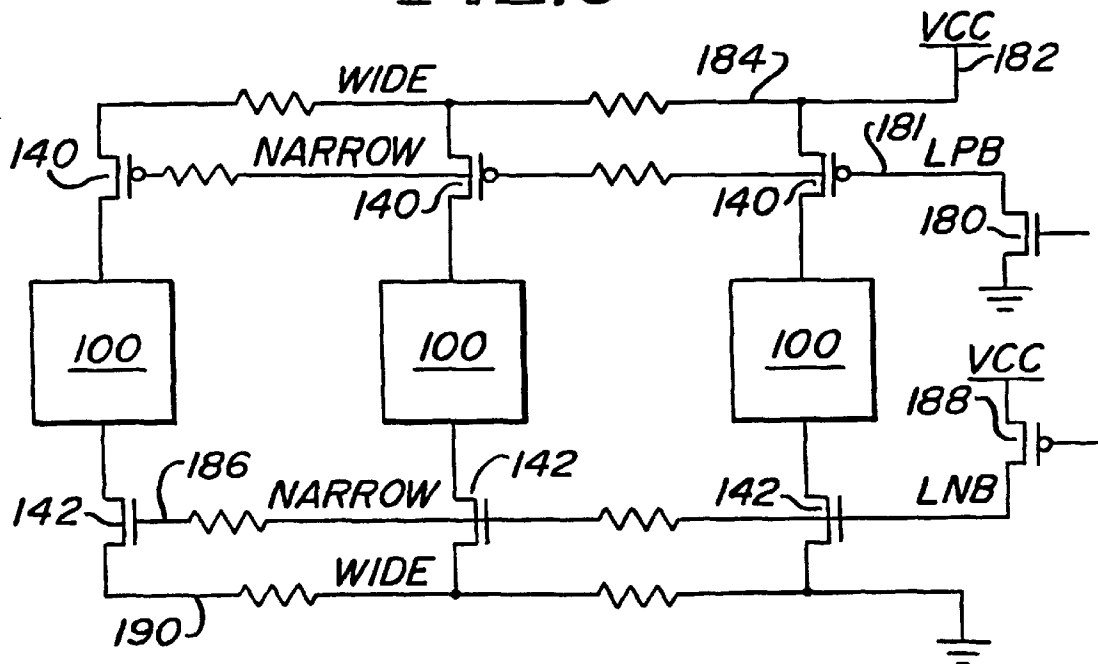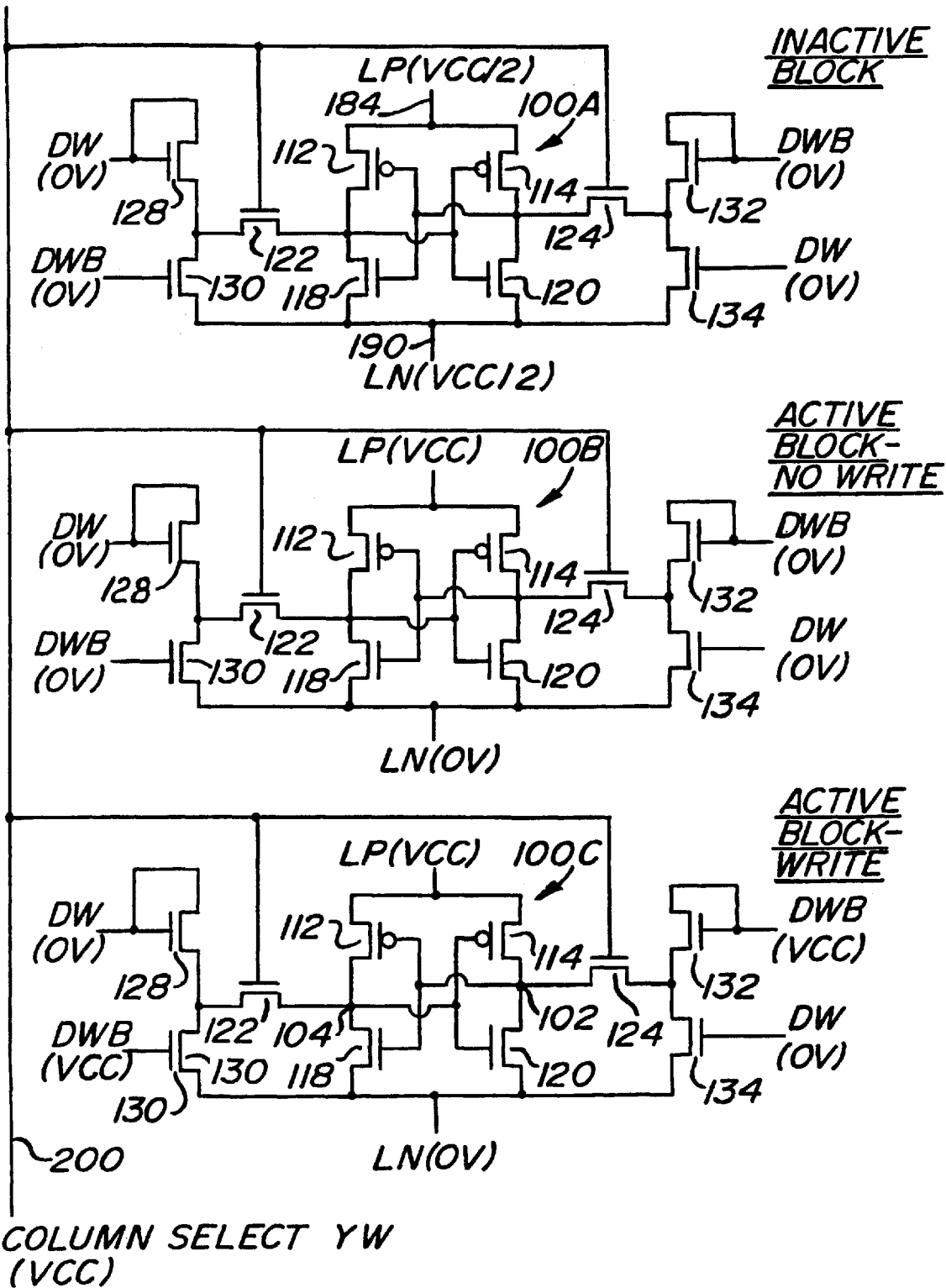
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