



[54] DYNAMIC RANDOM ACCESS MEMORY HAVING CONTINUOUS DATA LINE EQUALIZATION EXCEPT AT ADDRESS TRANSITION DURING DATA READING

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[75] Inventors: Yohji Watanabe; Kenji Tsuchida, both of Kawasaki, Japan

[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

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[21] Appl. No.: 08/150,782

[22] Filed: Nov. 12, 1993

Related U.S. Application Data

[63] Continuation of application No. 07/709,873, Jun. 4, 1991, abandoned.

[30] Foreign Application Priority Data

Jun. 4, 1990 [JP] Japan 2-144442

[51] Int. Cl.⁷ G11C 7/06; G11C 11/407

[52] U.S. Cl. 365/202; 365/203; 365/205; 365/207; 365/233.5

[58] Field of Search 365/154, 156, 365/189.05, 190, 202, 203, 205, 207, 233.5, 230.08; 307/494, 530, 355, 269

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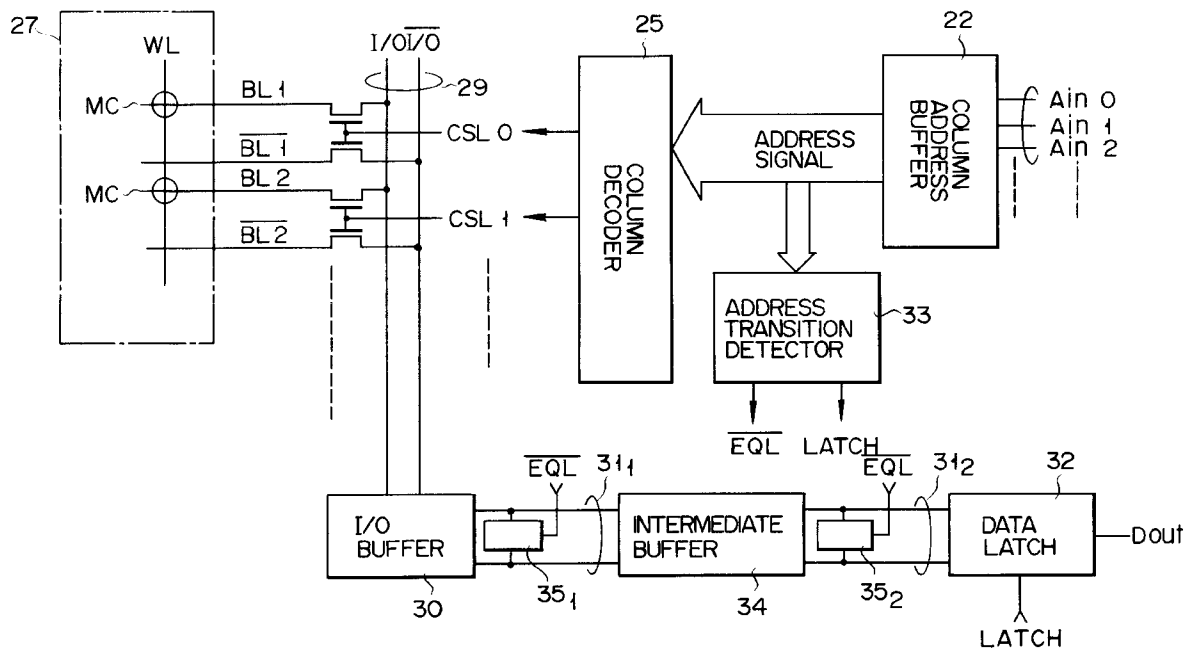
ISSCC 84/Thursday, Feb. 23, 1984/Continental Ballrooms 5-9/3:45 P.M.; Session XV: Static RAMs; Osamu Minato et al; 1984 IEEE International Solid-State Circuits Conference; pp. 222-223.

Primary Examiner—Jack A. Lane
Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

[57] ABSTRACT

A Dynamic Random Access Memory (DRAM) in which a data input/output buffer is connected between first data lines and second data lines. An equalizing circuit and a data latch circuit are connected to the second data lines. The equalizing circuit maintains the second data lines in reset condition, during normal operation. It temporarily releases the second data lines from the reset condition, in response to an output from an address-transition detecting circuit, thereby to transfer the data from the data input/output buffer. The data latch circuit latches the data transferred to the second data lines, in response to the output from the address-transition detecting circuit.

13 Claims, 9 Drawing Sheets



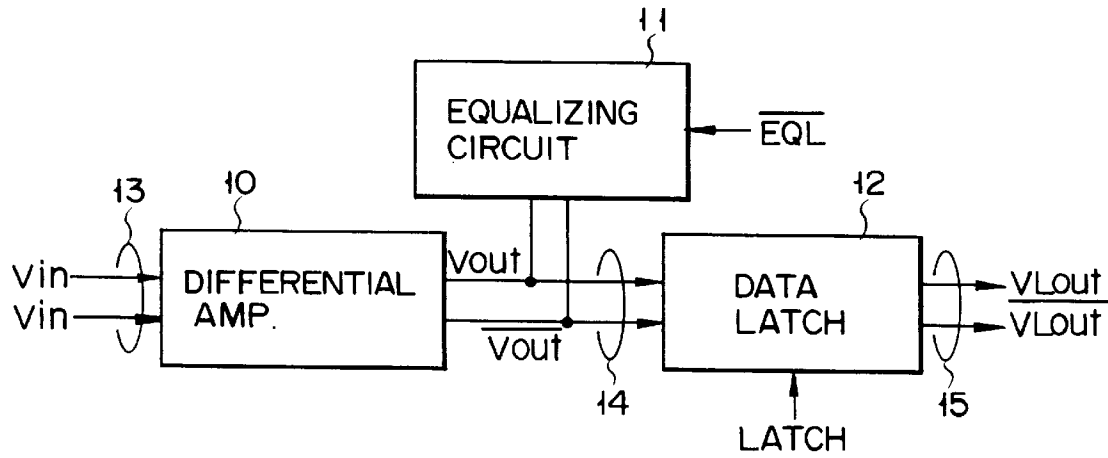


FIG. 1

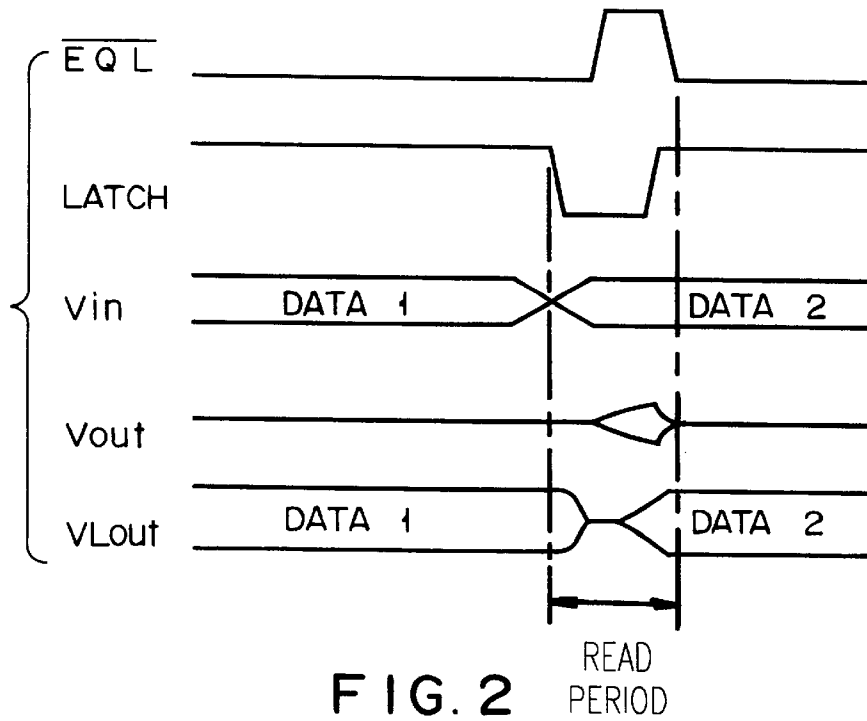


FIG. 2

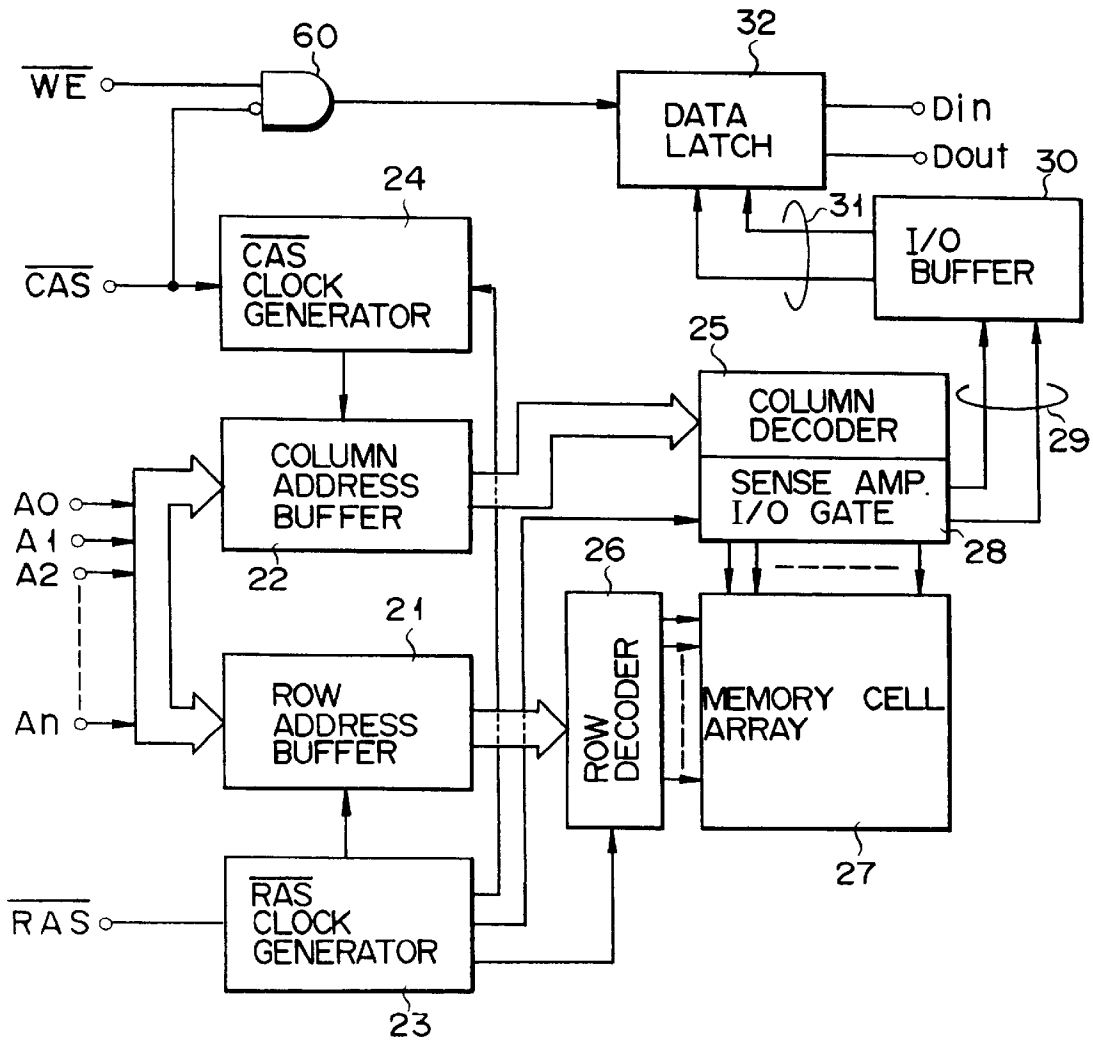
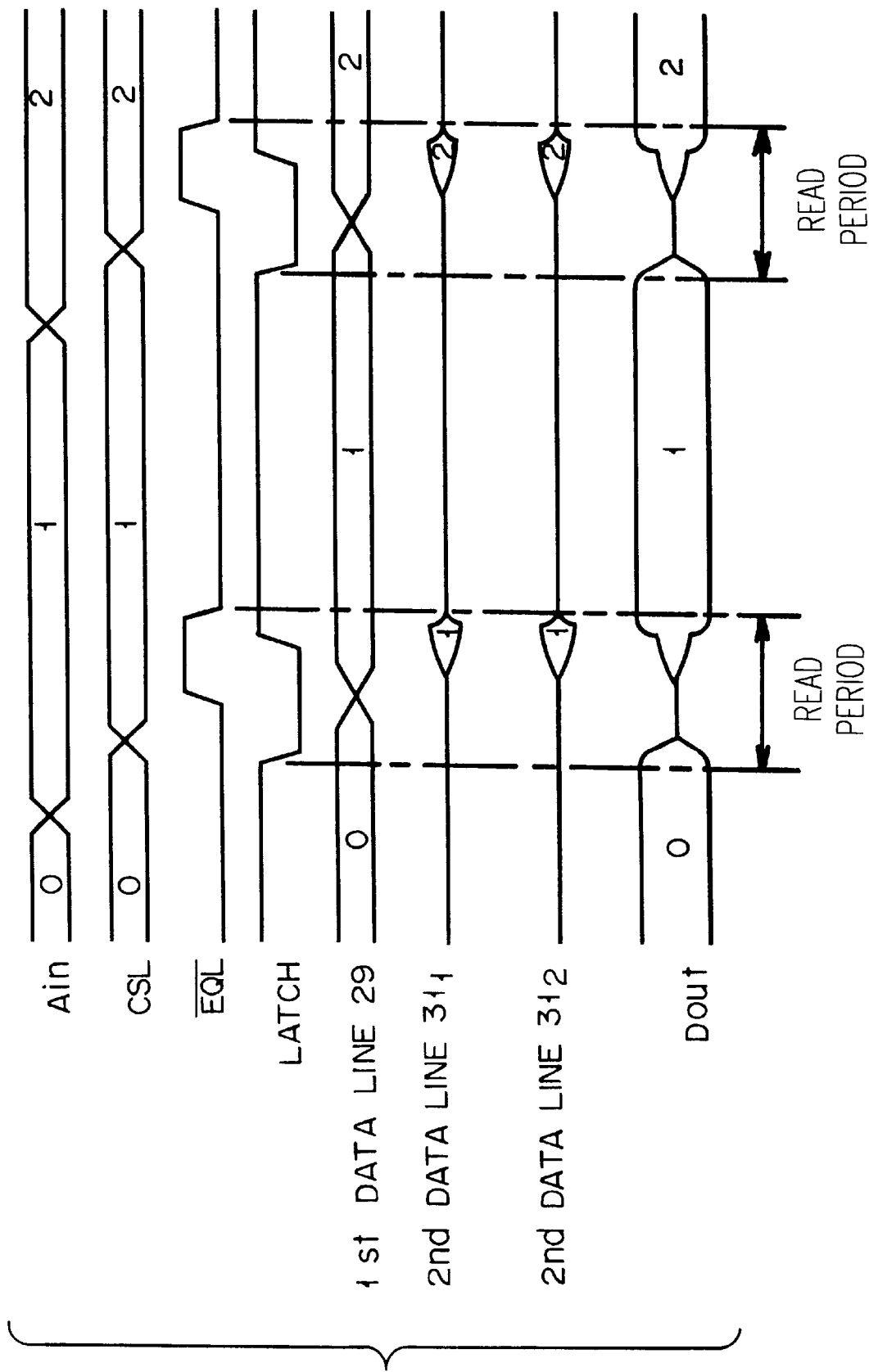


FIG. 3

FIG. 5



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