Re-Exam

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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Also referred to as FORM PTO-1465)

REQUEST FOR *INTER PARTES* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Inter Partes* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 19968-0006RX1

Date: January 19, 2012

1. ☒ This is a request for *inter partes* reexamination pursuant to 37 CFR 1.913 of patent number 6,366,130 issued April 2, 2002. The request is made by a third party requester, identified herein below.

2. ☒ a. The name and address of the person requesting reexamination is:
W. Karl Renner
Fish & Richardson P.C.
1425 K St, NW #1100, Washington, DC 20005

b. The real party in interest (37 CFR 1.915(b)(8)) is: Hynix Semiconductor Inc.

3. ☐ a. A check in the amount of $_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(2);

☒ b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(2) to Deposit Account No. 06-1050 ; **or**

☐ c. Payment by credit card. Form PTO-2038 is attached.

4. ☒ Any refund should be made by ☐ check or ☒ credit to Deposit Account No. 06-1050 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. ☒ A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.915(b)(5)

6. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
☐ Landscape Table on CD

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
If applicable, items a. – c. are required.

a. ☐ Computer Readable Form (CRF)
b. Specification Sequence Listing on:
i. ☐ CD-ROM (2 copies) or CD-R (2 copies); **or**
ii. ☐ paper
c. ☐ Statements verifying identity of above copies

8. ☐ A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. ☒ Reexamination of claim(s) 1-3 and 5-7 is requested.

10. ☒ A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. ☐ An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.915(b)(3)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.915(b)(1) & (3).

13. [X] It is certified that the estoppel provisions of 37 CFR 1.907 do not prohibit this reexamination. 37 CFR 1.915(b)(7)

14. [X] a. It is certified that a copy of this request has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:
KILPATRICK TOWNSEND & STOCKTON LLP
TWO EMBARCADERO CENTER, 8TH FLOOR
SAN FRANCISCO, CA 94111
Date of Service: January 19, 2012 ; **or**

[ ] b. A duplicate copy is enclosed because service on patent owner was not possible. An explanation of the efforts made to serve patent owner **is attached**. See MPEP 2620.

15. Third Party Requester Correspondence Address: Direct all communications about the reexamination to:

[X] The address associated with Customer Number: 26171

OR

[ ] Firm or Individual Name

Address

City	State	Zip
Country		
Telephone	Email	

16. [ ] The patent is currently the subject of the following concurrent proceeding(s):

[ ] a. Copending reissue Application No.
[ ] b. Copending reexamination Control No.
[ ] c. Copending Interference No.
[X] d. Copending litigation styled:
Cascades Computer Innovation, LLC v. Hynix Semiconductor Inc. in U.S. Dist Court Northern Dist of IL Case# 1:11-cv-04356

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Authorized Signature	Date: 01/19/2012
Typed/Printed Name: W. Karl Renner	Registration No., if applicable: 41265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent to Podlesny, et al.	)
	)
U.S. Patent No.: 6,366,130	)
Issued: April 2, 2002	)
	)
Serial No.: 09/505,656	)
Filed: February 17, 2000	)
	)
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	)

Mail Stop Inter Partes Reexam
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REQUEST FOR *INTER PARTES* REEXAMINATION UNDER 35 U.S.C. §§ 302 and 311 AND 37 C.F.R. § 1.902 *et seq.*

*****REEXAMINATION REQUEST FOR PATENT ASSERTED IN LITIGATION*****

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Appendix B2: Select Excerpts from Prosecution History of U.S. Patent No. 6,366,130

Appendix C: European Patent No. 0 597 231 to Hardee (hereinafter "Hardee")

Appendix D: U.S. Patent No. 5,274,598 to Fujii (hereinafter "Fujii")

Appendix E: U.S. Patent No. 5,659,512 to Koyanagi (hereinafter "Koyanagi")

Appendix F: IDS Form PTO/SB/08

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 302 and 311 and 37 C.F.R. § 1.902 *et seq.*, *inter partes* reexamination is requested for U.S. Patent No. 6,366,130 ("the '130 patent"). A copy of the '130 patent is attached in Appendix A.

Requestor is aware of one presently-pending proceeding in the United States District Court for the Northern District of Illinois, in which the '130 patent has been asserted. Section III of this request provides further detail on the pending litigation involving the '130 patent. In view of the current litigation, special dispatch pursuant to 35 U.S.C. §§ 314 is respectfully requested to expedite the handling of this request and for any subsequent reexamination proceedings.

Requestor is not aware of any reexamination certificates that have issued for the '130 patent. The '130 patent is not subject to a terminal disclaimer.

In accordance with 37 C.F.R. § 1.915, as modified by The Leahy-Smith America Invents Act (HR 1249, pp.16-20; Federal Register, Vol. 76, No. 185, pp.59055-58), this Request includes the following:

1. an identification of the patent by patent number and every claim for which reexamination is requested (Section II);

2. a citation of the patents and printed publications which are presented to provide a showing that there is a reasonable likelihood that the requester will prevail with respect to at least one of the claims challenged in the request (Section IV);

3. a statement pointing out, based on the cited patents and printed publications, each showing of a reasonable likelihood that the requester will prevail with respect to at least one of the claims challenged in the request, and a detailed explanation of the pertinence and manner of applying the patents and printed publications to every claim for which reexamination is requested (Sections VI and VII);

4. a copy of every patent or printed publication relied upon or referred to in paragraphs (1) through (3) above, accompanied by an English language translation of all the

necessary and pertinent parts of any non-English language document (Appendices C-E);

5. a copy of the entire patent including the front face, drawings, and specification/claims (in double column format) for which reexamination is requested, and a copy of any disclaimer, certificate of correction, or reexamination certificate issued in the patent (Appendix A);

6. a certification by the third party requester that a copy of the request has been served in its entirety on the patent owner at the address provided for in § 1.33(c) (Certification Following Signature Page);

7. a certification by the third party requester that the estoppel provisions of § 1.907 do not prohibit the *inter partes* reexamination (Section II); and

8. a statement identifying the real party in interest to the extent necessary for a subsequent person filing an *inter partes* reexamination request to determine whether that person is a privy (Section II).

The Director is hereby authorized to charge payment in the amount of $8,800 for the *inter partes* reexamination fee specified by 37 C.F.R. § 1.20(c)(2) to Deposit Account 06-1050.

II. IDENTIFICATION OF PATENT AND CLAIMS, AND REAL PARTY IN INTEREST

In accordance with 37 C.F.R. § 1.915(b)(1), (b)(7), and (b)(8), requester Hynix Semiconductor Inc. ("Hynix" or "Requester") requests *inter partes* reexamination of claims 1-3 and 5-7 of the '130 patent, assigned to Elbrus International Limited, Cayman Islands ("Elbrus")[1]. Requester certifies that the estoppel provisions of 37 C.F.R. § 1.907 do not prohibit this inter partes reexamination.

As explained below, claims 1-3 and 5-7 are unpatentable over the prior art patents and publications identified and applied in this Request. The patents and printed publications relied upon in this request, and the manner in which they are applied to the claims, present substantial new questions of patentability and show a reasonable likelihood that the Requester will prevail with respect to the claims challenged in the Request.

III. LITIGATION INVOLVING THE '130 PATENT

The '130 patent is the subject of pending litigation. In particular, Cascades Computer Innovation, LLC ("Cascades") has asserted the '130 patent against Hynix Semiconductor Inc. in the United States District Court for the Northern District of Illinois, Case No. 1:11-cv-04356. No other parties were named as co-defendants. Hynix has waived service of the complaint and its answer is due on January 19, 2012. A copy of the complaint is included in Appendix B1.

IV. CLAIMS FOR WHICH REEXAMINATION IS REQUESTED AND PRIOR ART REFERENCES APPLIED

Reexamination is requested for claims 1-3 and 5-7 of the '130 patent in view of the following art:

1. European Patent Publication No. 0 597 231 to Hardee (copy provided in Appendix C) (hereinafter "Hardee");

[1] Assignee listed on the US 6,366,130 patent: Elbrus International Limited, George Town Grand Cayman (KY). Appendix A at page 1. Assignee listed on the USPTO Assignment Database: Elbrus International Limited, P.O. BOX 265, George Town Grand Cayman, Cayman Island. In the Complaint for Patent Infringement, the plaintiff, Cascades Computer Innovation LLC stated that "Cascades owns the exclusive license and right to sue for past, present and future infringement of the '130 patent." Appendix B1 at page 2.

2. U.S. Patent No. 5,274,598 to Fujii (copy provided in Appendix D) (hereinafter "Fujii"); and

3. U.S. Patent No. 5,659,512 to Koyanagi (copy provided in Appendix E) (hereinafter "Koyanagi").

Each of the above references is listed on IDS Form PTO/SB/08 provided in Appendix F.

These references independently qualify as prior art under 35 U.S.C. § 102. Specifically, Hardee qualifies as prior art under 35 U.S.C. § 102(b) because Hardee issued was published on May 18, 1994, which is more than one year prior to the earliest possible effective February 17, 1999 filing date of the '130 patent.

Fujii qualifies as prior art under 35 U.S.C. § 102(b) because Fujii issued as a patent on December 28, 1993, which is more than one year prior to the earliest possible effective February 17, 1999 filing date of the '130 patent.

Koyanagi qualifies as prior art under 35 U.S.C. § 102(b) because Koyanagi issued as a patent on August 19, 1997, which is more than one year prior to the earliest possible effective February 17, 1999 filing date of the '130 patent.

None of the references were considered during prosecution of the '130 patent.

V. OVERVIEW OF THE GROUNDS OF UNPATENTABILITY

The '130 patent is directed to an electronic circuit configured to enable data transfer with relatively high speed and low power consumption. '130 patent at 2:34-38. The '130 patent attributes its improved speed and power characteristics to pre-charging of a differential bus and a differential data bus. Specifically, data buses are pre-charged to voltage levels prior to data transfer operations. Then, when data transfer is desired, the pre-charged voltage levels on opposing differential buses are each changed in the opposite manner, yielding a differential voltage level that represents data to be transferred. In this process, relatively modest voltage level changes are quickly and efficiently imparted on each data bus, with the resulting opposite but marginal changes reflecting a differential of sufficient magnitude to yield perceptible and transferable data.

Against this backdrop, the basic concept of pre-charging bus lines was itself recited by claims of the '130 patent. This feature was highlighted by applicants during original prosecution when seeking to distinguish prior art, and indeed, it was relied upon by that original Examiner as

the sole basis for allowing the claims of the '130 patent. Appendix B2 at page 24, Notice of Allowance mailed in Application No. 09/505,656 on February 22, 2001.

Below, additional details are provided regarding structure and function disclosed by the '130 patent, with reference to its specification and figures, despite the fact that claims of the patent were allowed based on pre-charging of the data buses alone.

Structurally, the '130 patent uses just two figures to illustrate an electronic circuit responsible for the pre-charging and claimed functionality. FIG. 1 provides an overview of the complete electronic circuit, and FIG. 2 shows details relating to a particular aspect of FIG. 1, namely its sensing amplifier element 16. Below, FIG. 1 is reproduced for convenient visual reference.

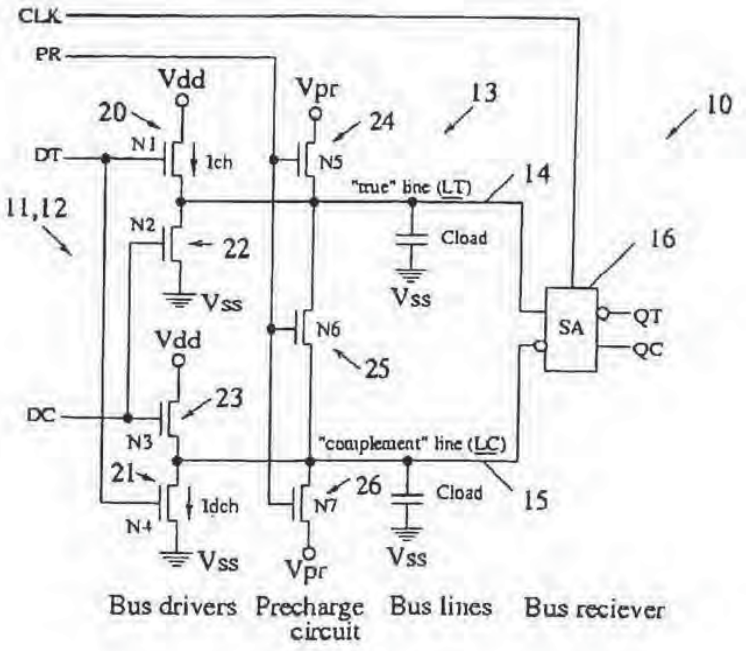


FIG.1.

As indicated by labels applied on the bottom of the drawing itself, FIG. 1 shows bus drivers, a precharge circuit/source, and bus lines (i.e., a differential bus) coupled to the bus drivers and to the voltage precharge circuit/source. Also coupled to the bus lines is a latching

sense amplifier 16, the contemplated details of which are illustrated by FIG. 2, reproduced below.

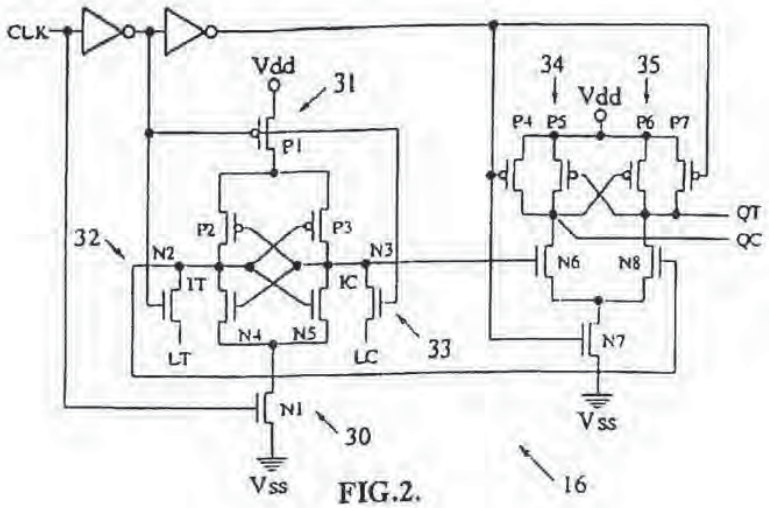


FIG.2.

In particular, in FIG. 2, latching sense amplifier 16 is shown to include a cross-coupled latch having internal nodes IT and IC coupled to differential data buses, and complementary outputs QT and QC.

Functionally, two phases of operation are describe for the bus driver circuit of FIG. 1, and two analogous but opposite phases of operation for the sense amplifier shown by FIG. 2. With respect to each, the two phases is identified as (1) a bus precharge phase and (2) a data transfer phase, but as indicated, they are opposite/offset to promote data propagation through the circuit. Below, the phases are described, first with respect to components of the bus driver circuit shown in FIG. 1 and then with respect to components of the sense amplifier shown by FIG. 2.

During the precharge phase of the bus driver circuit shown by FIG. 1:

> [t]he true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23 are in high impedance state and both bus lines are equalized and precharged to a potential Vpr (buses precharging voltage level) through the turned on transistors 24, 25 and 26. '130 patent at 2:18-22.

Thereafter, during the data transfer phase of the bus driver circuit shown by FIG. 1:

> [o]ne of the drivers is pulled up and charges the appropriate bus line from the precharged level Vpr toward a more positive Vdd – Vt (where Vt is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged

> level Vpr towards a more negative level Vss (ground). This provides a differential voltage: +dV and -dV from the precharging level Vpr between true and complement bus lines. Id. at 2:25-33.

During the precharge phase of the sense amplifier circuit shown by FIG. 2 (which occurs when the bus driver circuit is operating in its data transfer phase), the control input CLK is low, such that the differential voltage on bus lines 14 and 15:

> passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal 55 point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to Vdd and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high. Id. at 2:52-59.

And, during the data transfer phase of the sense amplifier circuit shown by FIG. 2 (which occurs when the bus driver circuit is operating in its precharge phase), the control input CLK is high, such that the differential voltage passed to the internal nodes IT and IC is received and passed by the cross-coupled amplifier

> to power buses (transistors 30 and 31 are turned on) and [the cross-coupled amplifier] begins to amplify the low voltage swings of the internal nodes IT and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low. Id. at 2:64-3:3.

During original prosecution, the handling Examiner rejected the original claims based on U.S. Patent No. 5,598,371 ("Lee") in view of U.S. Patent No. 6,184,722 ("Hayakawa"). Indeed, allowance was not secured until applicants amended the claims to recite pre-charging of bus lines, nor until they presented arguments suggesting that this general concept was missing from within the prior art. The Examiner's reasons for allowance, reproduced below, make clear that allowance was secured on this basis alone:

> applicants' arguments have been fully considered and deemed to be persuasive. The present invention teaches precharging the buses to a specific level between ground and Vdd, which results in equal, low differential Voltage swings, providing increased speed of data transfer. The prior art of Lee et al. does not teach such precharging buses as described above. Appendix B2 at page 24, Notice of Allowance mailed in Application No. 09/505,656 on February 22, 2001.

Despite the Examiner's determination that these features are absent from the prior art, a close inspection reveals that these features relate to very basic differential voltage amplification techniques that have been well-known among engineers designing sensing amplifier circuits for memory systems.

Because these features were well-known prior to the '130 patent, as demonstrated by the references applied in this Request, which show the features of claims 1-3 and 5-7 of the '130 patent, Requester requests reexamination of the '130 patent and cancellation of the challenged claims.

VI. THERE IS A REASONABLE LIKELIHOOD THAT THE REQUESTER WILL PREVAIL WITH RESPECT TO THE CLAIMS CHALLENGED

The legal standard for ordering *inter partes* reexamination was recently modified by The Leahy-Smith America Invents Act. See HR 1249, pp.16-20; Federal Register, Vol. 76, No. 185, pp.59055-58). An *inter partes* reexamination should be granted when there is a showing that there is a reasonable likelihood that the requester will prevail with respect to at least one of the claims challenged in the request (the "reasonable likelihood" standard). This standard replaced the previously applicable "substantial new question of patentability" standard. Regardless of how this new controlling standard is interpreted and applied in the courts and the Office, the instant Request is sufficient to justify reexamination. Indeed, the grounds of rejection proposed by this Request are based on patents and printed publications and they raise substantial new questions of patentability that are reasonably likely to be upheld against the claims being challenged.

Below, Requester sets forth proposed grounds for rejection of claims 1-3 and 5-7 of the '130 patent, demonstrating why the prior art applied in the proposed grounds are reasonably likely to be adopted and sustained against these claims. Because none of the references applied in this request were considered during prosecution of the '130 patent, they also raise substantial new questions of patentability with respect to claims 1-3 and 5-7 of the '130 patent.

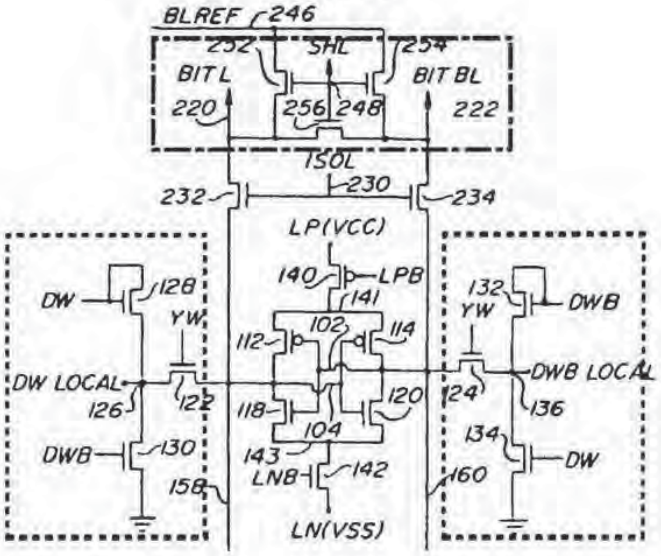
A. HARDEE

Hardee describes a memory circuit that amplifies a voltage difference between two precharged data buses during a write operation. In this manner, Hardee contemplates the concept of precharging differential buses that was deemed sufficient to justify allowance of the '130 patent claims.

Structurally, the Hardee memory circuit as shown in FIG. 8 represents one of many columns in a memory system, where the YW signal selects the column of memory circuit to be written. The true and complement data input signals are DW and DWB, respectively, and the

true and complement data output signals are BIT L and BIT BL, respectively, which lead to a memory cell. As shown in representative FIG. 8 reproduced below, the Hardee memory circuit includes a precharge source BLREF, a precharge circuit as enclosed in the dashed-dotted box, two bus drivers as enclosed in the dashed boxes, a cross-latched sense amplifier, and isolation transistors 232 and 234.

FIG. 8



Functionally, prior to writing the memory cell on a column, both DW and DWB are disabled. The YW signal is enabled, resulting in the DW Local and DWB Local bit lines being coupled to the data lines 158 and 160, respectively. Upon activating precharge circuit and the isolation transistors 232 and 234, the DW Local and DWB Local bit lines and the data lines 158 and 160 are precharged to a voltage BLREF, which is illustratively a constant voltage of ½ VCC. Hardee at 13:17-19. The precharged lines are then isolated by turning off the isolation transistors.

To write the memory cell on the column, DW or DWB is enabled while YW remains high, and a pair of transistor gates 128/134 or 130/132 turn on. The DW Local and the DWB Local bit lines experience a change in voltage, one bit line going high while the other bit line goes low. The differential voltage then enables the cross-latched sense amplifier and drives one of the data lines 158 or 160 to VCC and the other line to ground. Hardee at 13:43-53. The isolation transistors 232 and 234 are coupled to the output of the data lines 158 and 160, and

controlled to pass the voltage on the data lines 158 and 160 to the BIT L and BIT BL outputs after the voltages have reached a steady state.

As described, Hardee discloses a scheme for precharging differential data line pairs to a voltage of ½ VCC, and amplifying a differential voltage across a differential data line pair when writing data to a memory cell. In doing so, Hardee discloses the features identified by the Examiner as justifying allowance of independent claim 1. This and other teachings of Hardee establish a substantial (and new) question of patentability, and they also establish a reasonable likelihood that the requester will prevail with respect to at least independent claim 1.

B. FUJII

Fujii describes a circuit configured to enable access to a memory circuit/cell. In doing so, Fujii describes applying a charge to main and sub-bit data bus lines (i.e., precharging those bus lines) before using those bus lines to read data from the memory circuit/cell. In this manner, Fujii also contemplates the concept of precharging differential buses, which was deemed sufficient to justify allowance of the '130 patent claims.

Structurally, with reference to FIG. 3 of Fujii, reproduced below, there exist several selectable memory circuits (MCs) in a memory array. Each memory circuit (MC) includes a true and complement sub-bit line (SB and $\overline{SB}$) used to read data from within the memory cell (MC). When selected, the sub-bit lines SBi/$\overline{SBi}$ for a particular memory circuit (i) may be used to communicate data from within that memory cell to main data lines (MB and $\overline{MB}$), which yield memory contents through their connection at output buses I/O and $\overline{I/O}$. Importantly, a precharge source HVC and a precharge circuit 5 are configured to work together to precharge main data line pair MB and $\overline{MB}$ and sub-bit lines SBi/$\overline{SBi}$. Also bus drivers (enclosed in the dashed-dotted boxes), a main cross-latched sense amplifier 1, and isolation transistors Q_Y and Q_T are configured to facilitate flow of precharge voltage and data to/from sub-bit data lines (SB and $\overline{SB}$).

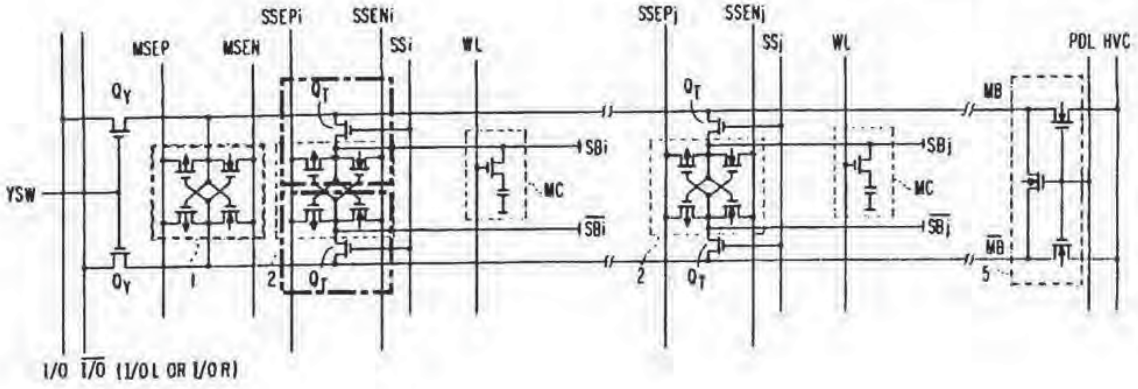


FIG. 3
PRIOR ART

Functionally, the sub-bit line selection signal SSi is enabled when access is desired to data within a corresponding a memory cell MC. Responsively, the main data line pair MB and $\overline{MB}$ are coupled to the sub-bit line pair SBi and $\overline{SBi}$, where the index "i" corresponds to one of the several sub-bit line pairs able to be connected to the main data line pair, namely, the sub-bit line pair corresponding to the sub-bit line selection signal SSi.

To enable ready access to data from within the memory cell MC, the sub-bit lines (SBi and $\overline{SBi}$) and the data lines (MB and $\overline{MB}$) are each precharged[2], by disabling the word select signal WL while enabling the precharge control signal PDL and the sub-bit line selection signal SSi. The precharged main and sub-bit lines are thereafter isolated from the precharge source by disabling the precharge control signal PDL, and they are isolated from each other by disabling the sub-bit line selection signal SSi. Fujii at 2:53-56.

The precharged sub-bit line SBi then accesses the data from the memory cell MC by enabling the word select signal WL, enabling the precharged sub-bit line SBi to experience a change in voltage reflective of the memory cell MC data contents/charge. Moreover, this change in voltage is experienced in the opposite direction on the complement sub-bit line $\overline{SBi}$ by controlling the driver control signals SSEPi and SSENi. Fujii at 2:56-64.

Ultimately, the sub-bit line selection signal SSi is again enabled to connect the main data line pair MB and $\overline{MB}$ to the sub-bit line pair SBi and $\overline{SBi}$, and using the main sense amplifier

[2] Fujii discloses "[t]he main bit lines and the sub-bit lines are set at the ½ Vcc level of the pre-charge level." Fujii at 2:48-49.

activation signals MSEP and MSEN, the differential voltage at the sub-bit line pair SBi and $\overline{SBi}$ is passed to the main data line pair MB and $\overline{MB}$. Fujii 2:60-3:3.

The two isolation transistors, both identified as Q_Y, are coupled to the output of the main data lines MB or $\overline{MB}$, and used to control passage of the voltages on the main data lines MB and $\overline{MB}$ to the output buses I/O and $\overline{I/O}$ after those voltages have reached a steady state.

As described, Fujii discloses a sensing amplifier circuit that precharges the main and sub-bit (differential) data lines to a voltage of ½ VCC. In doing so, Fujii discloses the features identified by the Examiner as justifying allowance of independent claim 1, establishing a substantial (and new) question of patentability, and also establishing a reasonable likelihood that the requester will prevail with respect to at least independent claim 1.

C. KOYANAGI

Koyanagi describes a circuit configured to enable data to be read from a memory circuit/cell. Koyanagi, like other prior art described above, discloses precharging of differential buses used to communicate the data from the memory cell to an output. In particular, in the following paragraphs, data line pairs DQ/*DQ and D/*D are each precharged. In this manner, Koyanagi contemplates the concept of precharging differential buses that was deemed sufficient to justify allowance of the '130 patent claims.

Structurally, and in accord with the FIG. 1 illustration of two memory circuits/cells in a memory system/array, reproduced below, Koyanagi describes a data read circuit which includes paired bit lines BL1/*BL1 and BL2/*BL2 that may be selected to enable a read of a corresponding memory circuit/cell, where an example is enclosed in a solid-lined box. Indeed, each exemplary bit line pair (e.g., BL1/*BL1 and BL2/*BL2) of the data read circuit described by Koyanagi couple both to a corresponding memory cell, and to the differential data line pair (DQ and DQ*). The data read circuit includes a precharge source and circuits 304 and 308 for precharging the differential data line pairs DQ/*DQ and D/*D, respectively, to a high-impedance value (e.g. Vcc). Koyanagi also describes two bus drivers (within the dashed boxes), a latching sense amplifier (within the dashed-dotted box), and isolation circuits 310/311.

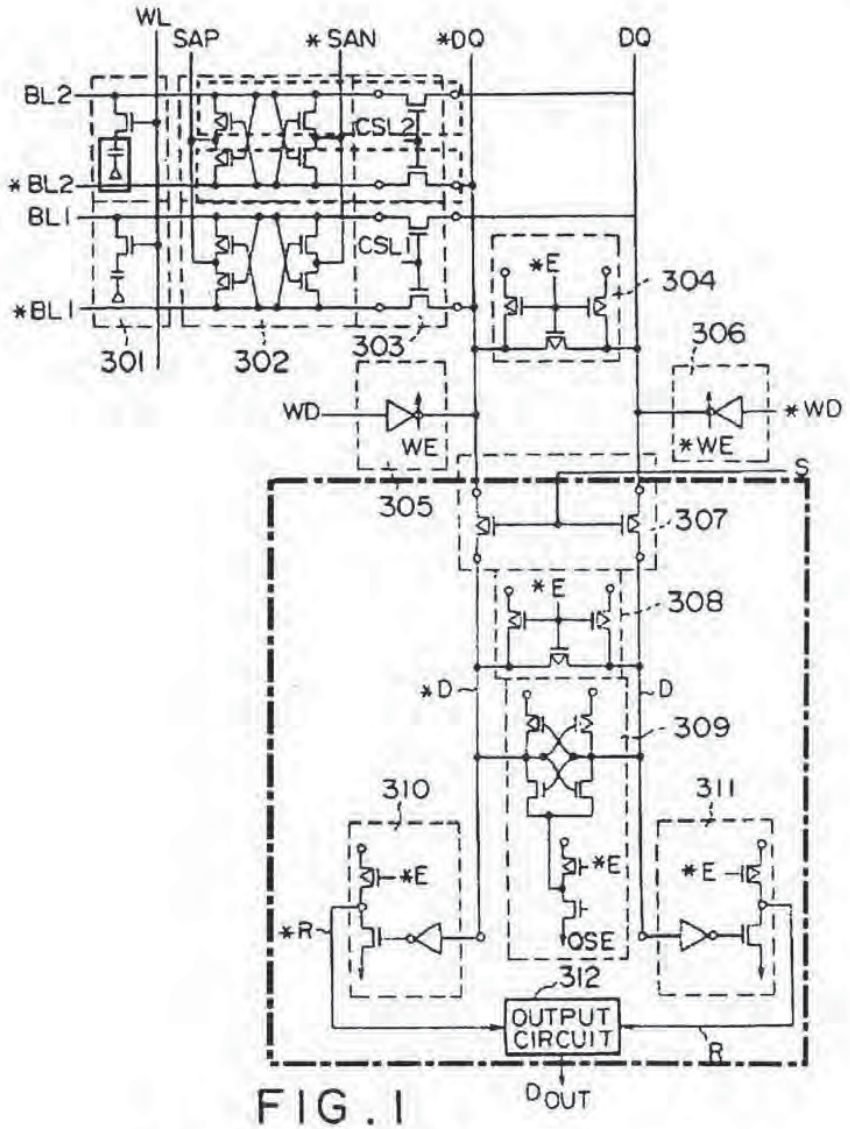


FIG. 1
PRIOR ART

Functionally, prior to reading the data from a memory cell, both CSL1 and CSL2 are disabled to isolate the bit line pairs BL1/*BL1 and BL2/*BL2 from data line pair DQ/*DQ. The *E signal is then enabled, such that the voltage sources coupled to circuits 304 and 308 are

respectively applied as precharging voltages to the separated[3] data line pairs DQ/*DQ and D/*D. The precharging voltage is illustratively a constant voltage of VCC. Koyanagi at 1:54-58.

When the Koyanagi circuit reads data from an exemplary bit line pair BL2/*BL2 in FIG. 1, the word select signal WL is enabled, and data from the memory cell is coupled to the true bit line BL2. The control signals SAP and *SAN are then controlled to logic high and low, respectively, which enables the bus driver 302 to raise the voltage on one bit line of the bit line pair BL2 or *BL2 and to lower the voltage on the other bit line. Koyanagi at 1:40-45. CSL2 is then enabled to connect the bit line pair BL2/*BL2 to the precharged data line pair DQ/*DQ, which induces a voltage difference between the data line pair DQ/*DQ. Koyanagi at 1:60:64. Control signal S is then enabled to connect the data line pair DQ/*DQ to the precharged data line pair D/*D, which induces a voltage difference between the data line pair D/*D.

The differential voltage then enables the cross-latched sense amplifier 309 and connects one of the data lines D or *D to ground and the other line to VCC. Consequently, the voltage on one of the data lines D or *D lowers from VCC to ground, while the voltage on the other data line stays constant at VCC. Koyanagi at 2:15-17. The isolation circuits 310/311 are coupled to the output of the data lines D and *D, and controlled to pass the voltage on the data lines D and *D to the R and *R outputs after the voltages have reached a steady state. Koyanagi at 2:18-20.

As described, Koyanagi discloses precharging the data pairs DQ/*DQ and D/*D to a high-impedance state voltage, and thereafter adjusting the voltage on those lines to reflect differentials that correspond to data read from memory cell. Because Koyanagi discloses the features identified by the Examiner as justifying allowance of independent claim 1, Koyanagi establishes a substantial (and new) question of patentability, and it also establishes a reasonable likelihood that the requester will prevail with respect to at least independent claim 1.

VII. MANNER OF APPLYING CITED PRIOR ART TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

In this Section, Requester proposes various grounds of rejection for claims 1-3 and 5-7, justifying reexamination. Requester presents claim charts that compare the claim language, under its broadest reasonable construction, with the disclosure of the prior art, as understood by one of ordinary skill in the art. The proposed rejections include anticipation rejections. Requester

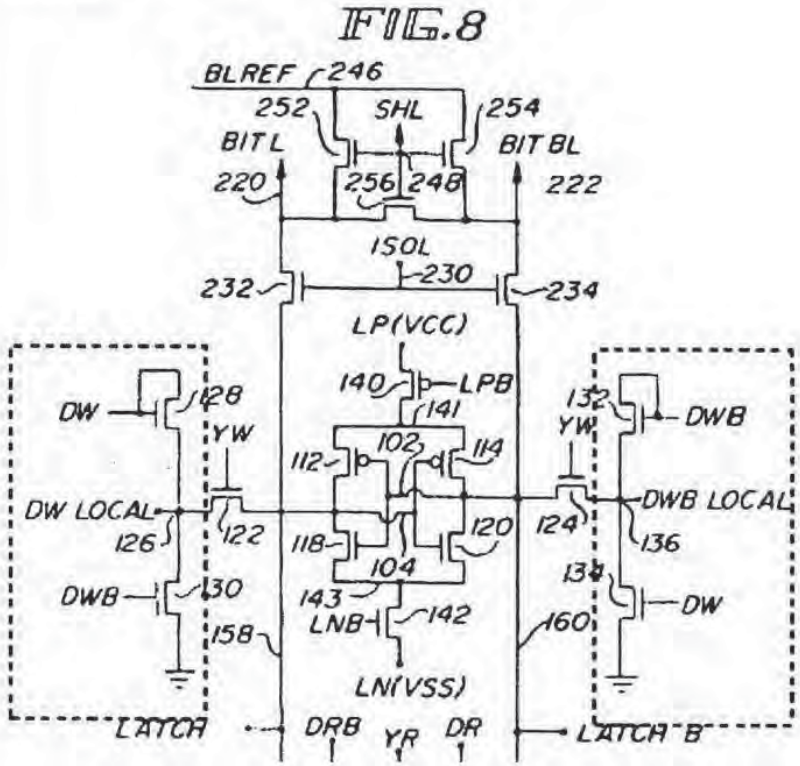
[3] The two data line pairs DQ/*DQ and D/*D are separated by isolation circuit 307 as shown in FIG. 1 of Koyanagi.

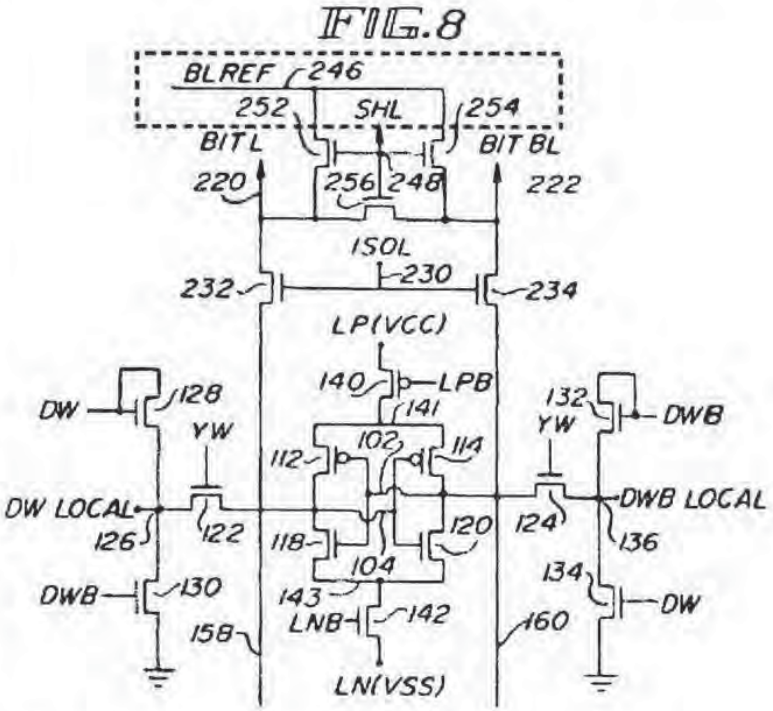
further notes that under the M.P.E.P., the closeness of the prior art with the claimed invention at times merits alternative rejections over a single reference, namely an anticipation or an obviousness rejection. *See* M.P.E.P. § 2112. ("There is nothing inconsistent in concurrent rejections for obviousness under 35 U.S.C. 103 and for anticipation under 35 U.S.C. 102." In re Best, 562 F.2d 1252, 1255 n.4, 195 U.S.P.Q. 430, 433 n.4 (CCPA 1977)). For several of the claims, Requester has proposed alternative anticipation/obviousness rejections to advise the Examiner of the various options for rejecting the challenged claims.

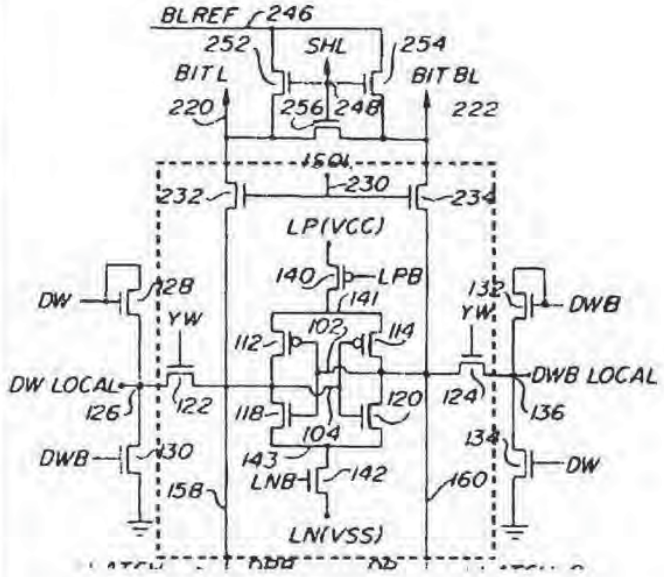
A. HARDEE

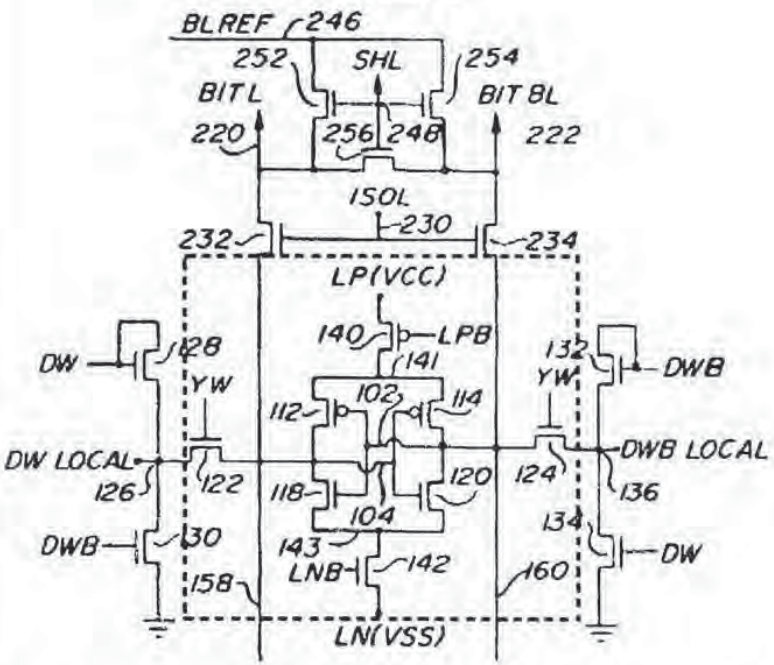
As shown in the Claim Chart below, each and every limitation of claims 1-3 and 5-7 of the '130 patent are anticipated by Hardee. Specifically, the following grounds of rejection are presented in the claim chart below:

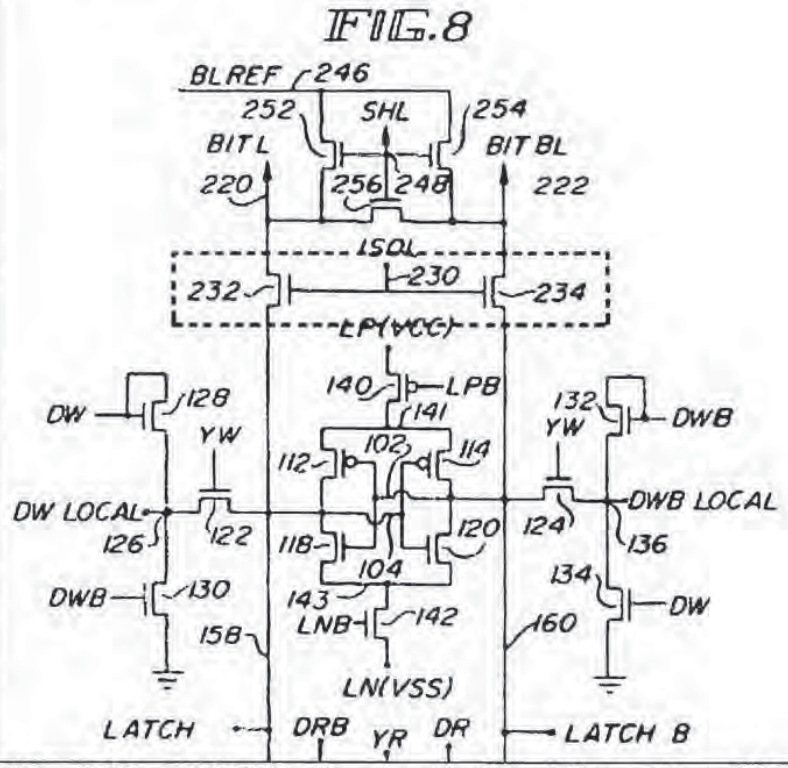
(1) Claims 1-3, and 5-7 of the '130 patent are anticipated by Hardee.

Claim Language	Application of Hardee
Claim 1	
1. A data transfer arrangement comprising:	Hardee describes a memory circuit that transfers data from and to a memory cell using differential data lines.
two bus drivers;	FIG. 8 of Hardee shows two bus drivers, with DW and DWB, located at dashed boxes overlaying FIG. 8, reproduced below:  Specifically, the voltage at data lines 126 and 136 are driven based on the voltage levels

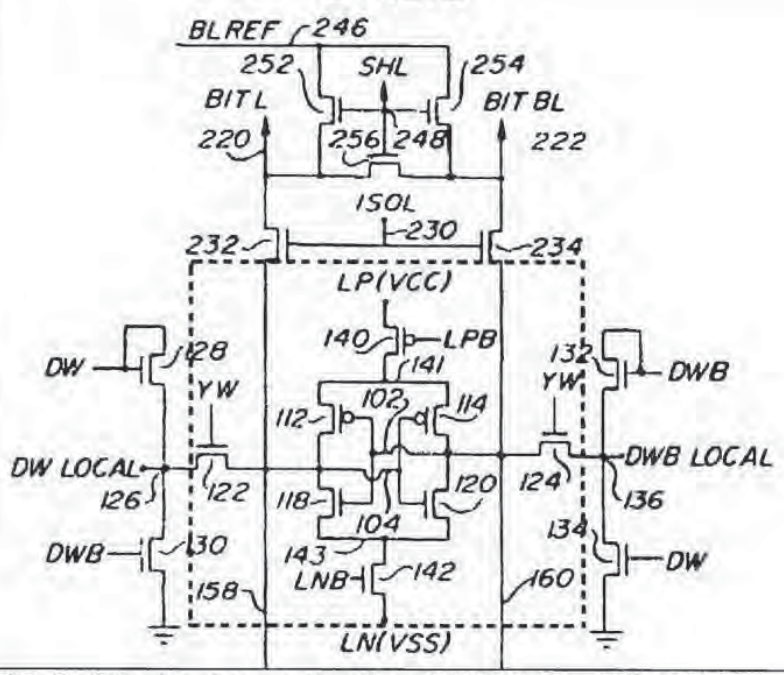
	established for DW and DWB. When DW is set to a logic high and DWB is consequentially set to a logic low, the voltage levels at 126 and 136 rise and fall, respectively. Whereas, when DW is set to a logic low and DWB is consequentially set to a logic high, the voltage levels at 126 and 136 fall and rise, respectively. Hardee at 14:43-53.
a voltage precharge source;	FIG. 8 of Hardee shows a voltage precharge source, as indicated by the dashed box below:  Hardee discloses the BLREF reference, which is configured to provide a precharge source for data line pairs 158/160 and 126/136, where the BLREF value is illustratively a constant voltage of ½ VCC. Hardee at 13:17-19.

a differential bus coupled to the bus drivers and to the voltage precharge source;	Hardee discloses a differential bus 126 and its complement 136, each being coupled to the above-identified bus drivers (DW and DWB) and to the above-identified voltage precharge source BLREF. In greater detail, when control signals YW, SHL, and ISOL are high, the differential bus pair 126 and 136 are connected to BLREF and precharged to ½ Vcc. Conversely, when control signals ISOL and SHL are low, the differential bus pair 126 and 136 are connected to the bus drivers. Hardee at 14:43-53.
and a latching sense amplifier coupled to the differential bus;	Hardee discloses a latching sense amplifier, as indicated by the dashed box overlaying the version of FIG. 8 reproduced below, coupled to the differential bus pair 126 and 136. FIG. 8 

wherein the latching sense amplifier comprises: a first stage including a cross-coupled latch coupled to a differential data bus;	Hardee discloses a cross-latched circuit as the first stage of the latching sense amplifier, as indicated by the dashed box overlaying the version of FIG. 8 reproduced below. The first stage is coupled to a differential data bus 158, where the complement differential data bus is 160. FIG. 8  To write the memory cell on the column, DW or DWB is enabled while YW remains high, and a pair of transistor gates 128/134 or 130/132 turn on. The DW Local and the DWB Local bit lines experience a change in voltage, one bit line going high while the other bit line goes low. The differential voltage enables the cross-latched sense amplifier and drives one of the data lines 158 or 160 to VCC and the other line to ground. Hardee at 13:43-53.

and an output stage coupled to an output of said first stage; wherein the output of the first stage is coupled to an input of the output stage;	Hardee discloses an output stage, as indicated by the dashed box overlaying the version of FIG. 8 provided below, coupled to an output of the cross-latched circuit. Specifically, the output stage includes two isolation transistors 232 and 234 controlled by the ISOL signal. The differential voltage pair 158 and 160, at the output of the first stage, serve as the input of this output stage. Hardee at 14:19-23. 
wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where	When ISOL and YW signals are enabled, the differential bus 158 and the differential data bus 126 are precharged to ½ Vcc. Specifically, in Hardee, "[t]ransistors 252 and 254 have their source-drain paths connected between the bit line reference BLREF at node 246 and the bit lines 220, 222, respectively, and will therefore, when turned on, couple the bit line reference

Vpr=K*Vdd, and K is a precharging voltage factor.	voltage to the bit lines themselves. . . The bit line reference is illustratively a constant voltage approximately equal to ½ VCC in one preferred embodiment." Hardee at 13:5-19.
Claim 2	
2. The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers.	The two bus drivers DW and DWB are pull-up and pull-down bus drivers. Specifically, the voltage at data lines 126 and 136 are driven based on the voltage levels established for DW and DWB. When DW is set to a logic high and DWB is consequentially set to a logic low, the voltage levels at 126 and 136 rise and fall, respectively. Whereas, when DW is set to a logic low and DWB is consequentially set to a logic high, the voltage levels at 126 and 136 fall and rise, respectively. Hardee at 14:43-53.
Claim 3	
3. The data transfer arrangement in accordance with claim 1, wherein the first stage of the latching sense amplifier comprises: a plurality of input pass transistors each having a gate, a source terminal, and a drain;	Hardee, as shown using the dashed box overlying the following reproduction of FIG. 8 shows aspects of the first stage of its latching sense amplifier, including input pass transistors (e.g., NMOS 122 and 124), each having a gate, a source terminal, and a drain.

	FIG. 8 
and a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain;	FIG. 8 of Hardee shows a plurality of NMOS (e.g., 142, 118, 120) and PMOS transistors (e.g., 140, 112, 114), each having a gate, a source terminal, and a drain.
wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass transistors is coupled to an input,	FIG. 8 of Hardee shows the drains of the input pass transistors coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, and also shows each source terminal of the input pass transistors coupled to an input. The drain of an input pass transistor 122 is coupled to a drain of the cross-coupled latch amplifier NMOS 118 and PMOS 112 transistors, and the source terminal of the input pass transistor 122 is coupled to an input data bus 126.

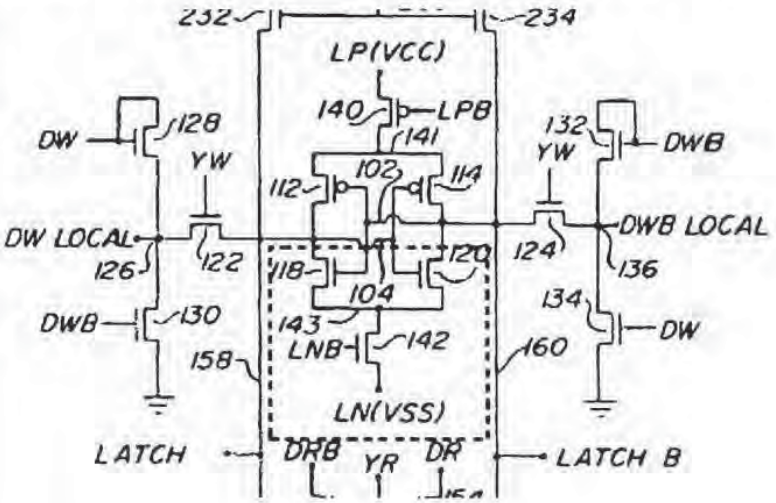
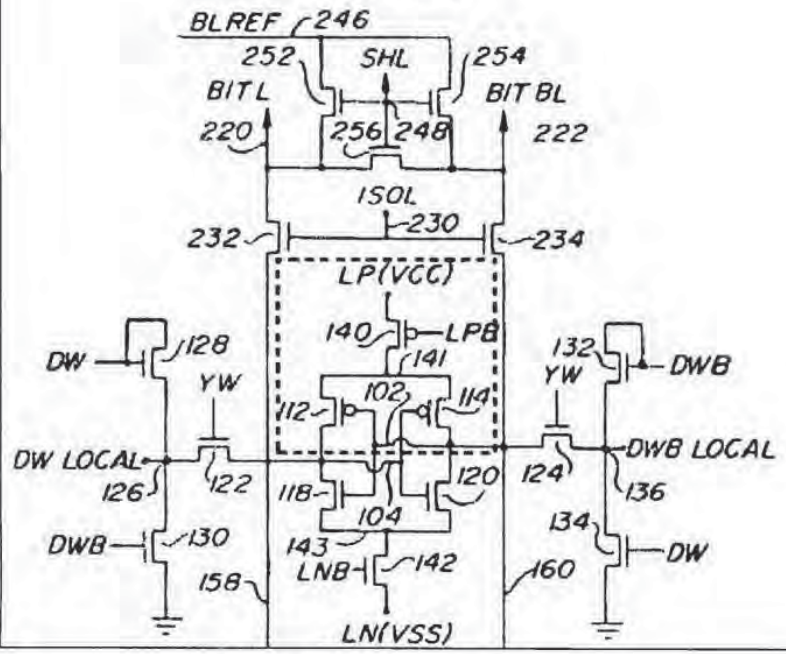
	Similarly, the drain of an input pass transistor 124 is coupled to a drain of the cross-coupled latch amplifier NMOS 120 and PMOS 114 transistors, and the source terminal of the input pass transistor 124 is coupled to an input data bus 136.
the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input,	Within the box overlaying the version of FIG. 8 reproduced below, Hardee discloses coupling between the sources of the cross-coupled latch amplifier NMOS transistors 118 and 120 and the drain of the NMOS transistor 142 coupled to a LNB input. 
and the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input.	FIG 8 of Hardee shows that the sources of the PMOS transistors 112 and 114 are coupled to the drain of the PMOS transistor 140 having a gate coupled to the LPB signal.

FIG.8


BLREF
246
252
SHL
254
BIT L
BIT BL
220
256
248
222
ISOL
230
232
234
LP(VCC)
140
LPB
141
128
DW
YW
102
112
114
132
YW
DWB
DW LOCAL
126
122
118
120
124
136
DWB LOCAL
104
DWB
130
143
LNB
142
134
DW
158
160
LN(VSS)

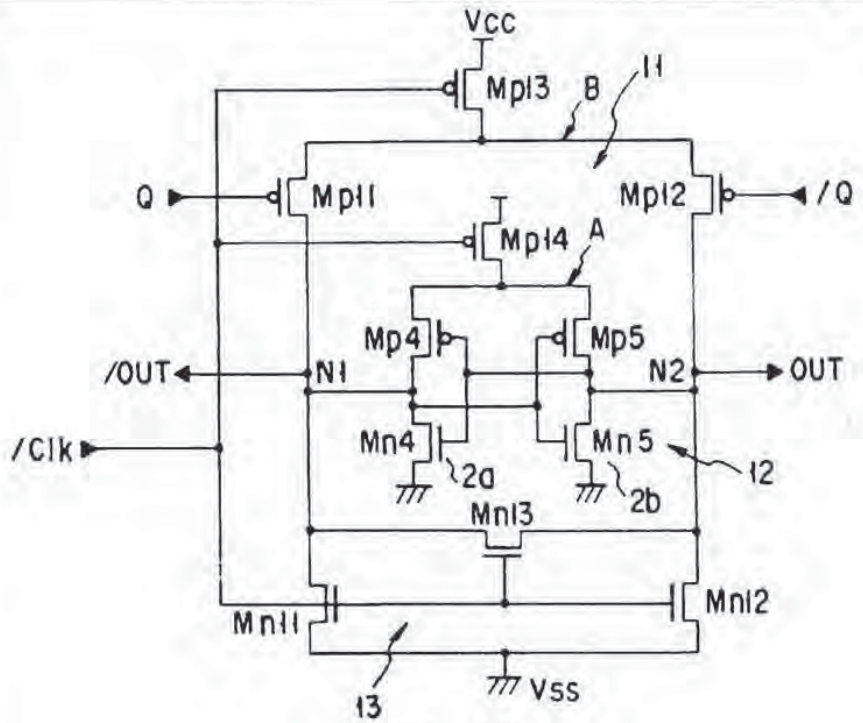
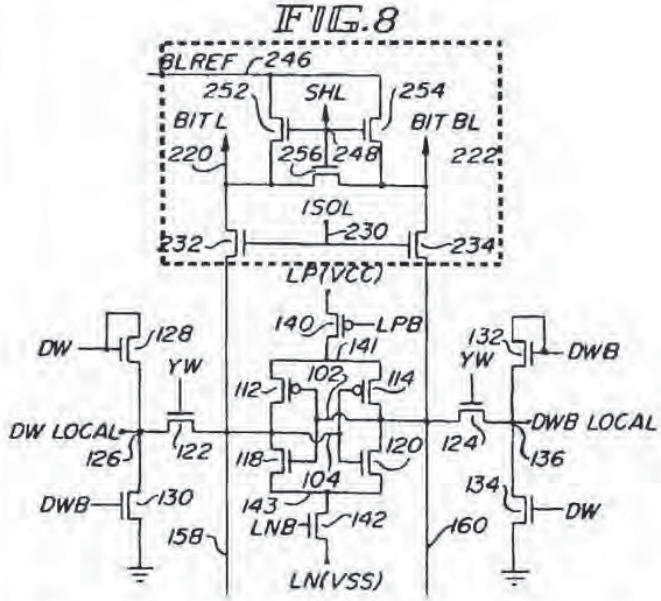
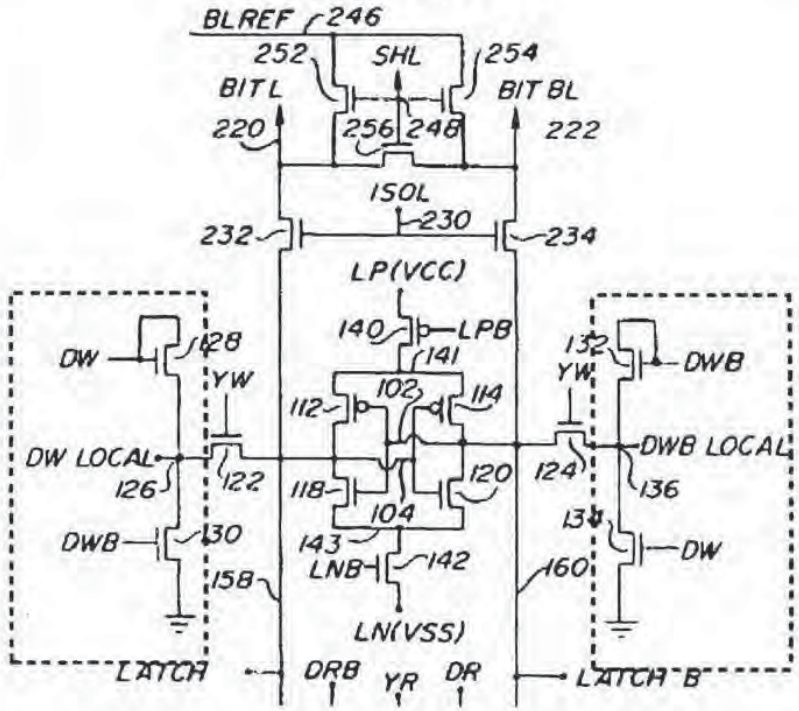


FIG. 18

Claim 5	
5. The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic	Hardee discloses the use of ½ VCC as its precharging voltage, dictating that the precharge voltage is both less than a logic high voltage (VCC) and greater than a logic low voltage (GND). Specifically, Hardee states that "[t]ransistors 252 and 254 have their source-drain paths connected between the bit line reference BLREF at node 246 and the bit lines 220, 222 respectively, and will therefore, when turned on, couple the bit line reference voltage to the bit lines themselves. . . The bit line reference is illustratively a constant voltage approximately

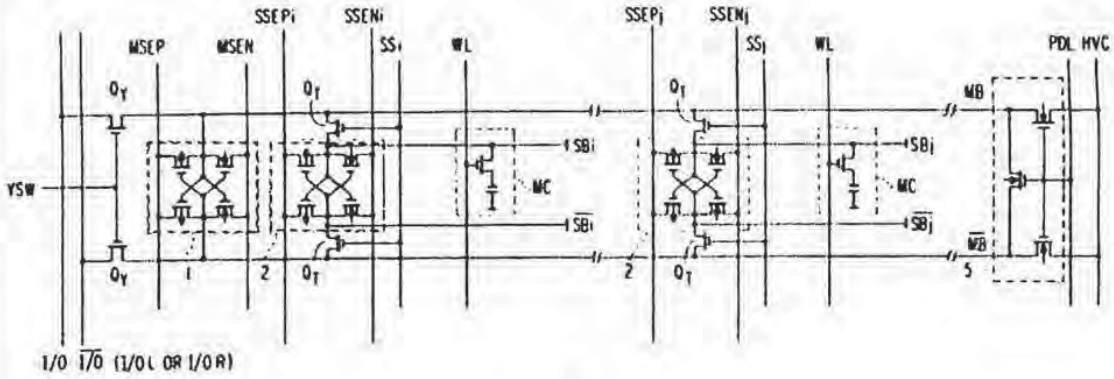
high voltage and greater than a logic low voltage.	equal to ½ VCC in one preferred embodiment." Hardee at 13:5-19.
Claim 6	
6. The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.	FIG. 8 of Hardee shows a precharge circuit, as enclosed in the dashed box, coupled between the precharge source and the differential bus.  Specifically, in Hardee, the precharge circuit as controlled by signals SHL and ISOL. When both signals and the YW signal are enabled, the differential bus 126 is precharged to the same voltage as BLREF.
Claim 7	
7. The data transfer arrangement in	The two bus drivers as shown in FIG. 8 of Hardee are pull-up and pull-down bus drivers:

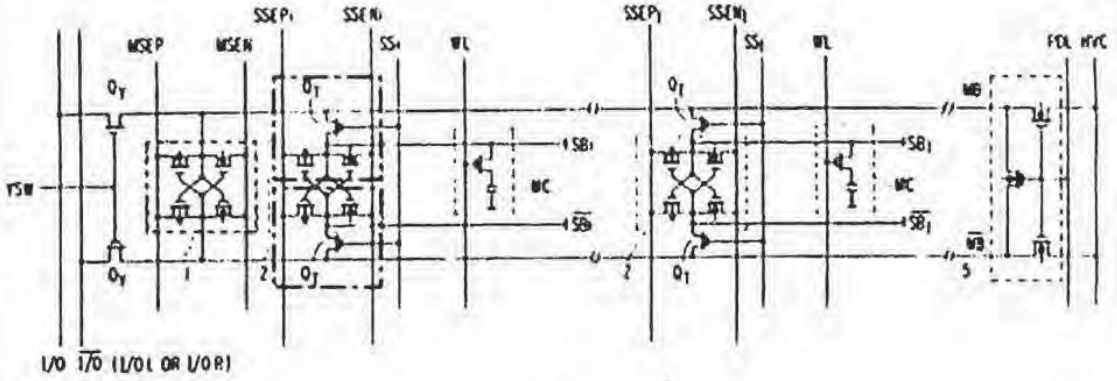
accordance with claim 2 wherein the active pull up and pull down bus drivers are NMOS transistors.	FIG.8  As shown, the active pull-up and active pull-down bus drivers in Hardee are implemented with NMOS transistors.

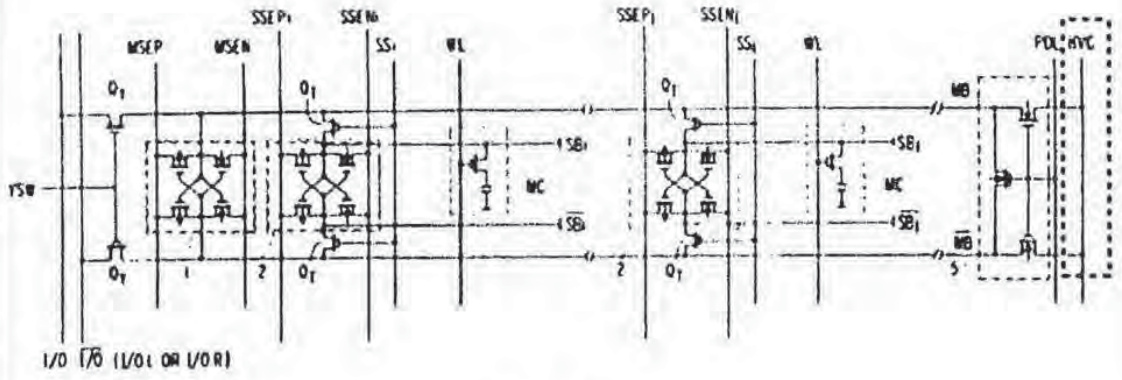
B. FUJII

As shown in the Claim Chart below, each and every limitation of claims 1, 2, and 5-7 are anticipated by Fujii. The following grounds of rejection are presented in the claim chart below:

(1) Claims 1, 2, and 5-7 of the '130 patent are anticipated by Fujii.

Claim Language	Application of Fujii
Claim 1	
1. A data transfer arrangement comprising:	Fujii describes a circuit configured to enable access to a memory circuit/cell. In doing so, Fujii describes applying a charge to main and sub-bit data bus lines (i.e., precharging those bus lines) before using those bus lines to read data from the memory circuit/cell. In this manner, Fujii also contemplates the concept of precharging differential buses, which was deemed sufficient to justify allowance of the '130 patent claims. FIG. 3 of Fujii shows an exemplary data read circuit configuration, showing one memory circuit/cell within many columns in a memory system/array. Using this circuit configuration, the data read from a memory cell MC is transferred from one of the sub-bit line pairs SB and $\overline{SB}$ to the main data line pair MB and $\overline{MB}$.  FIG. 3 PRIOR ART
two bus drivers;	Fujii discloses two bus drivers, examples of which are shown by the circuits within the dashed-dotted boxes overlying the version of FIG. 3 reproduced below. These drivers, in combination with control signals SSEPi and SSENi, drive bus lines SBi and $\overline{SBi}$. Specifically, the bus lines SBi and $\overline{SBi}$ are precharged to an equal "precharged" voltage prior to reading. Then, during a read operation, WL is enabled to allow the data in the memory cell MC to be transferred to the true bus line SBi. The voltage difference between the bus lines SBi and $\overline{SBi}$ is amplified by the

	two bus drivers, while configuring SSEPi to logic high and SSENi to logic low. Fujii at 2:60-64.  FIG. 3 PRIOR ART
a voltage precharge source;	Fujii discloses a voltage precharge source, an example of which is shown by the circuit within the dashed box overlying the version of FIG. 3 reproduced below. To enable ready access to data from within the memory cell MC, the sub-bit lines (SBi and $\overline{SBi}$) and the data lines (MB and $\overline{MB}$) of Fujii are each precharged by HVC to ½ Vcc, by disabling the word select signal WL while enabling the precharge control signal PDL and the sub-bit line selection signal SSi. Fujii at 48-49 ("The main bit lines and the sub-bit lines are set at the ½ Vcc level of the pre-charge level."). A box overlaying the version of FIG. 3 reproduced below shows the precharging source of Fujii.

	 FIG. 3 PRIOR ART
a differential bus coupled to the bus drivers and to the voltage precharge source;	Fujii discloses a differential bus coupled to the bus drivers and to the voltage precharge source, examples of which are shown by the data lines within the dashed-dotted boxes overlying the version of FIG. 3 reproduced below. Sub-bit line pair SBi and $\overline{SBi}$ are differential buses coupled to the bus drivers (identified above) and to the voltage precharge source HVC.

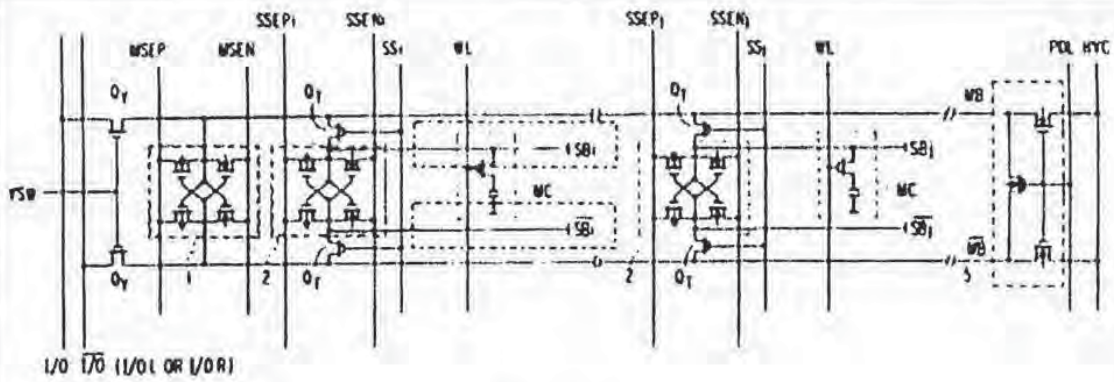
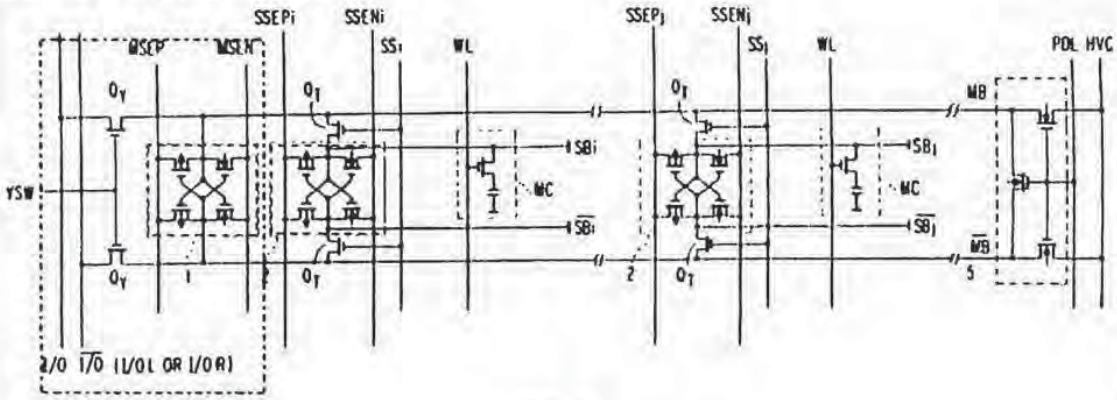


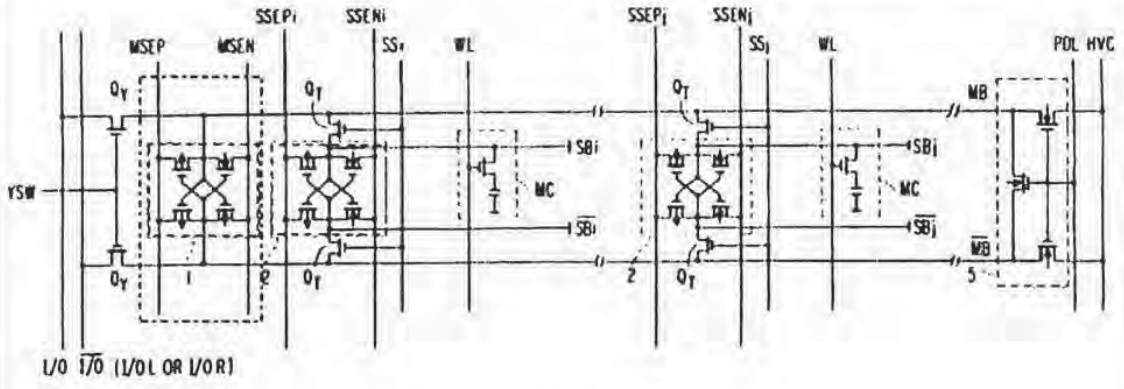
FIG. 3
PRIOR ART

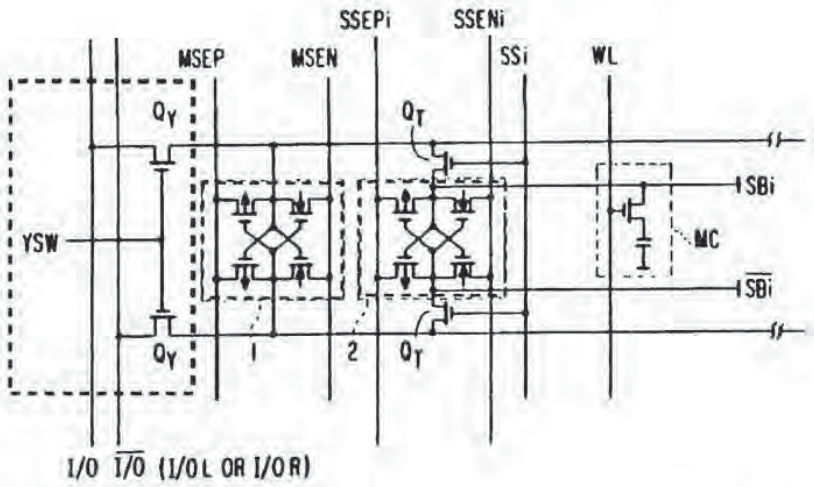
More specifically, when the word select signal WL and the sub-bit sense amplifier activation signals SSEPi and SSENi are disabled, and the precharge control signal PDL and the sub-bit select signal SSi are enabled, the differential bus SBi is precharged to the ½ Vcc level as the precharge source HVC. Fujii at 2:45-52.

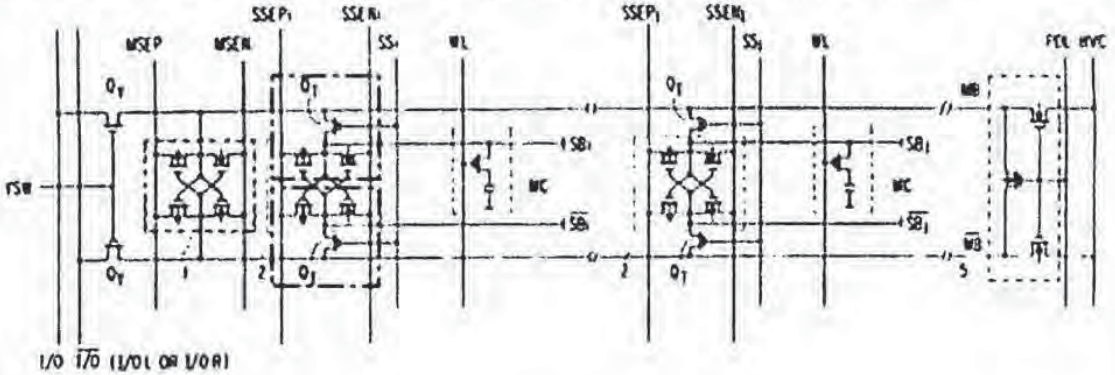
Subsequently, to read the data in the memory cell MC, the precharge control signal PDL is disabled and the word select signal WL and the sub-bit sense amplifier activation signals SSEPi and SSENi are enabled. The data in the memory cell MC is then read to the differential bus SBi, and the differential voltage between the differential bus SBi and its complement bus $\overline{SBi}$ is amplified by the bus drivers including the cross-latched sub-sense amplifier circuit 2. Fujii 2:53-64.

and a latching sense amplifier coupled to the differential bus;	Fujii discloses a latching sense amplifier coupled to the differential bus, an example of which is shown by the circuit within the dashed-dotted boxes overlying the version of FIG. 3 reproduced below. The modified version of FIG. 3 includes a dashed-dotted box to highlight the main sense amplifier, which is a latching sense amplifier, and which is coupled to the differential bus pair SBi and $\overline{SBi}$. The main differential data line pair MB and $\overline{MB}$, which is a part of the

	latching sense amplifier, read data from the differential bus pair SBi and $\overline{SBi}$. The latching sense amplifier then amplifies the differential voltage on the main differential data line pair MB and $\overline{MB}$ to logic high and logic low.  FIG. 3 PRIOR ART
wherein the latching sense amplifier comprises: a first stage including a cross-coupled latch coupled to a differential data bus;	Fujii discloses a first stage of the latching sense amplifier, an example of which is shown by the circuit within the dashed-dotted boxes overlying the version of FIG. 3 reproduced below. As shown in the following version of FIG. 3, modified to highlight a sub-portion of the latching sense amplifier, the first stage of the latching sense amplifier is a cross-coupled latch coupled to a differential data bus MB. The differential data bus pair MB and $\overline{MB}$ are coupled to the differential bus pair SBi and $\overline{SBi}$ through isolation transistors Q_T. When the sub-bit select signal SSi is enabled, the voltages on the differential bus pair SBi and $\overline{SBi}$ are passed to differential data bus pair MB and $\overline{MB}$, and the differential voltage is amplified by the cross-coupled latch. Fujii at 2:64-3:3.

	 FIG. 3 PRIOR ART
and an output stage coupled to an output of said first stage; wherein the output of the first stage is coupled to an input of the output stage;	Fujii discloses an output stage of the latching sense amplifier, an example of which is shown by the circuit within the dashed-dotted boxes overlying the version of FIG. 3 reproduced below. The following version of FIG. 3 is an exploded version of a portion of that FIG., using an overlaying box to highlight an output stage coupled to the first stage. Specifically, as shown, the output of the first stage (MB and $\overline{MB}$) is coupled to the input of the output stage (QY controlled by column selection signal YSW).

	 FIG. 3 PRIOR ART
wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.	Fujii discloses precharging each of the differential bus SBi and the differential data bus MB to a voltage of the precharge source HVC, namely ½ Vcc. Specifically, when the word select signal WL and the sub-bit sense amplifier activation signals SSEPi and SSENi are disabled, and the precharge control signal PDL and the sub-bit select signal SSi are enabled, the differential bus SBi and the differential data bus MB are precharged to the ½ Vcc level of the precharge source HVC. Fujii at 2:45-52. Fujii discloses a precharging voltage factor of ½. When the voltage on the differential bus and the differential data bus deviate from the ½ Vcc level, the sub-bit or the main sense amplification circuit can be enabled to amplify the differential voltage.
Claim 2	
2. The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active	Fujii discloses two bus drivers, as shown in dashed-dotted boxes in FIG. 3 below. One of the two bus drivers functions as an active pull-up bus driver, and the other functions as an active pull-down driver.

pull-up and active pull-down bus drivers.	Specifically, the sub-bit differential bus pair SBi and $\overline{SBi}$ are precharged to ½ Vcc. During data read, the true sub-bit bus SBi is connected to the memory cell MC, and it creates a differential voltage between SBi and $\overline{SBi}$. The control signal SSi, SSEPi, and SSENi are then enabled, such that the two bus drivers drive one of the sub-bit differential bus lines SBi or $\overline{SBi}$ up towards logic high and the other sub-bit line down towards logic low. Fujii at 2:60-64.  FIG. 3 PRIOR ART
Claim 5	
5. The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.	The Fujii memory circuit includes a precharge source HVC and a differential bus SBi, as shown in FIG. 3.

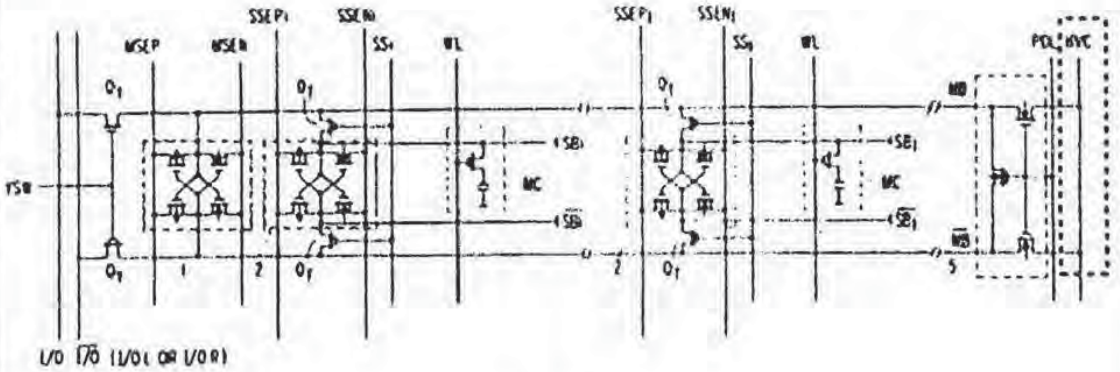
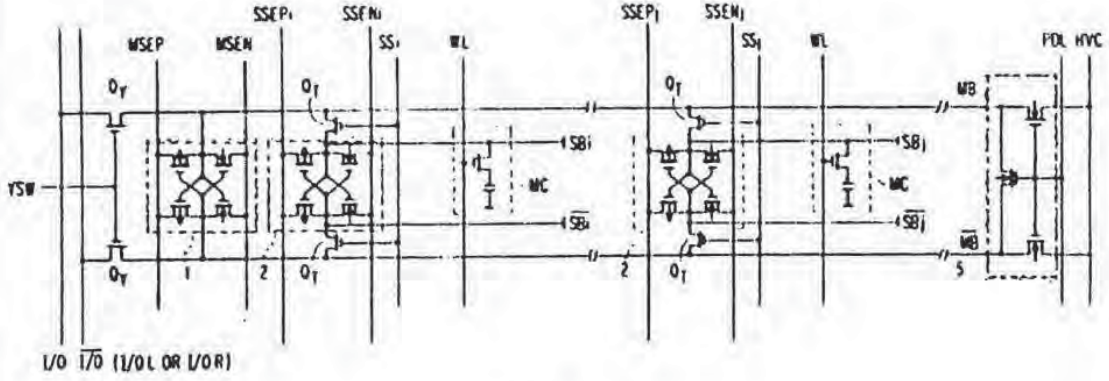


FIG. 3
PRIOR ART

Specifically, prior to accessing the data from the memory cell MC to the sub-bit line SBi, the word select signal WL is disabled, while the precharge control signal PDL is enabled. The main data line pair MB and $\overline{MB}$ as well as the sub-bit line pair SBi and $\overline{SBi}$ are precharged to a voltage HVC, which is illustratively a constant voltage of ½ VCC, that is a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage. Fujii at 2:37-49, with particular reference to lines 48-49 ("The main bit lines and the sub-bit lines are set at the ½ Vcc level of the pre-charge level.").

Claim 6	
6. The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.	Fujii discloses a precharge circuit 5 coupled between the precharge source HVC and the differential bus SBi, as shown in FIG. 3. Prior to accessing the data from the memory cell MC to the differential bus SBi, the word select signal WL is disabled, while the precharge control signal PDL is enabled. The precharge circuit 5 is activated, and the differential bus pair SBi and $\overline{SBi}$ are then precharged to a voltage HVC, which is illustratively a constant voltage of ½ VCC. Fujii at 2:37-41. The precharged differential bus pair are then isolated from the precharge source by disabling the precharge

	control signal PDL.  FIG. 3 PRIOR ART
Claim 7	
7. The data transfer arrangement in accordance with claim 2 wherein the active pull up and pull down bus drivers are NMOS transistors.	The active pull up and pull down bus drivers as shown in FIG. 3 of Fujii are implemented using a combination of NMOS and PMOS transistors.

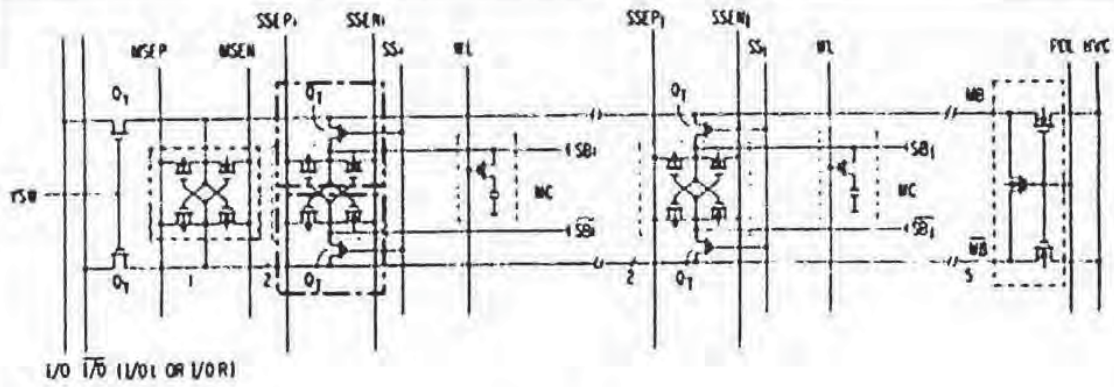


FIG. 3
PRIOR ART

However, FIG. 5 of Fujii shows another implementation of pull up and pull down bus drivers that are implemented using NMOS transistors, as identified in dotted boxes below. Therefore it would have been obvious to modify the bus drivers in FIG. 3 to provide active pull up and pull down bus drivers using NMOS transistors only.

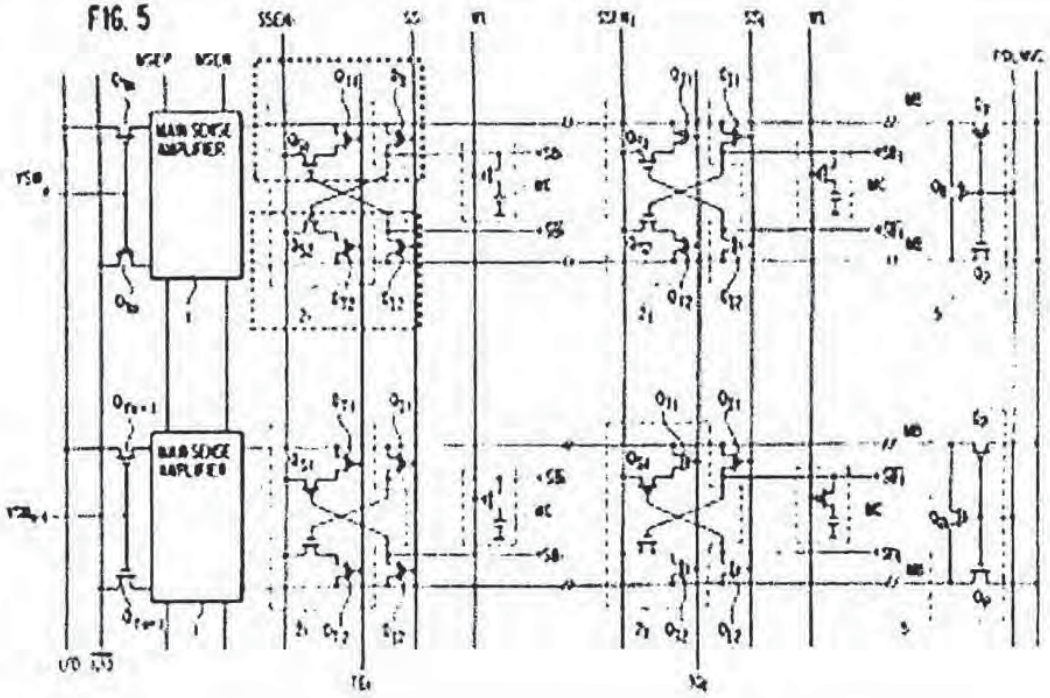


FIG. 5
MAIN SENSE AMPLIFIER
MAIN SENSE AMPLIFIER

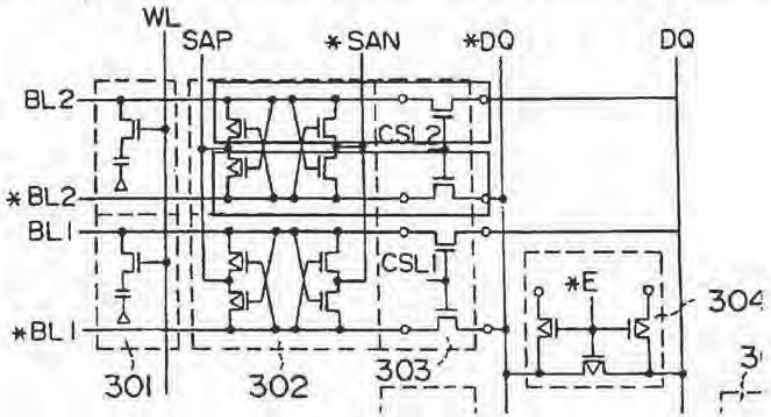
C. KOYANAGI

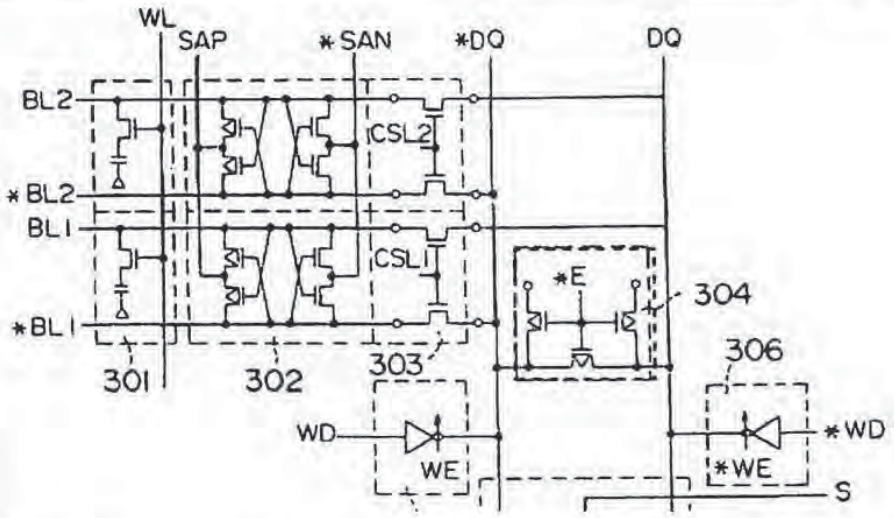
As shown in the Claim Chart below, each and every limitation of claims 1, 2, and 6 are anticipated by Koyanagi, and the features of claims 5 and 7 are rendered obvious in light a combination of Koyanagi and Fujii. The following grounds of rejection are presented in the claim chart below:

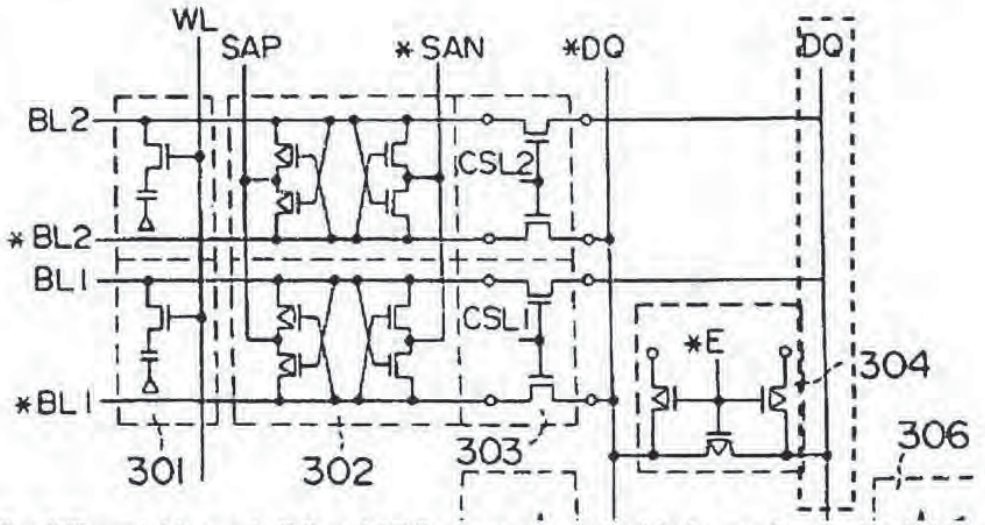
(1) Claims 1, 2, and 6 of the '130 patent are anticipated by Koyanagi.

(2) Claim 5 of the '130 patent is obvious over Koyanagi in view of Hardee.

(3) Claim 7 of the '130 patent is obvious over Koyanagi in view of Fujii.

Claim Language	Application of Koyanagi
Claim 1	
1. A data transfer arrangement comprising:	Koyanagi describes a circuit configured to enable data to be read from a memory circuit/cell. Koyanagi, like other prior art described above, discloses precharging of differential buses used to communicate the data from the memory cell to an output. In particular, data line pairs DQ/*DQ and D/*D are each precharged. In this manner, Koyanagi contemplates the concept of precharging differential buses that was deemed sufficient to justify allowance of the '130 patent claims.
two bus drivers;	FIG. 1 of Koyanagi shows two bus drivers, as enclosed in dashed boxes below:  These elements in combinations with control signals SAP and *SAN drive bus lines BL2 and *BL2. During a read operation, WL is enabled and the data in the memory cell is transferred to the true bus line BL2. The voltage difference between the bus lines BL2 and *BL2 is amplified by the two bus drivers. Koyanagi at 2:41-50.
a voltage precharge source;	FIG. 1 of Koyanagi shows a voltage precharge source coupled a precharge circuit 304.

	 The precharge circuit 304 is controlled by signal *E, and the load of the precharge circuit 304 is disclosed by Koyanagi as a high impedance condition source (i.e. Vcc). Koyanagi at 1:54-58. prior to reading the data from a memory cell, both CSL1 and CSL2 are disabled to isolate the bit line pairs BL1/*BL1 and BL2/*BL2 from data line pair DQ/*DQ. The *E signal is then enabled, such that the voltage sources coupled to circuit 304 is applied as a precharging voltage to the separated data line pair DQ/*DQ (upon enablement of *E, circuit 308 similarly precharges bus lines D/*D). The precharging voltage is illustratively a constant voltage of VCC. Koyanagi at 1:54-58.
a differential bus coupled to the bus drivers and to the voltage precharge source;	FIG. 1 of Koyanagi shows a differential bus DQ coupled to the two bus drivers and to the voltage precharge source.

	 The differential bus pair DQ and *DQ are precharged with the precharge circuit 304, and the voltage on the input line BL2 and *BL2 drive the differential bus pair DQ and *DQ with control signals CSL2, SAP, *SAN, and WL.
and a latching sense amplifier coupled to the differential bus;	FIG. 1 of Koyanagi shows a latching sense amplifier, as enclosed by the dashed box in the version of FIG. 1 copied below, coupled to the differential bus DQ.

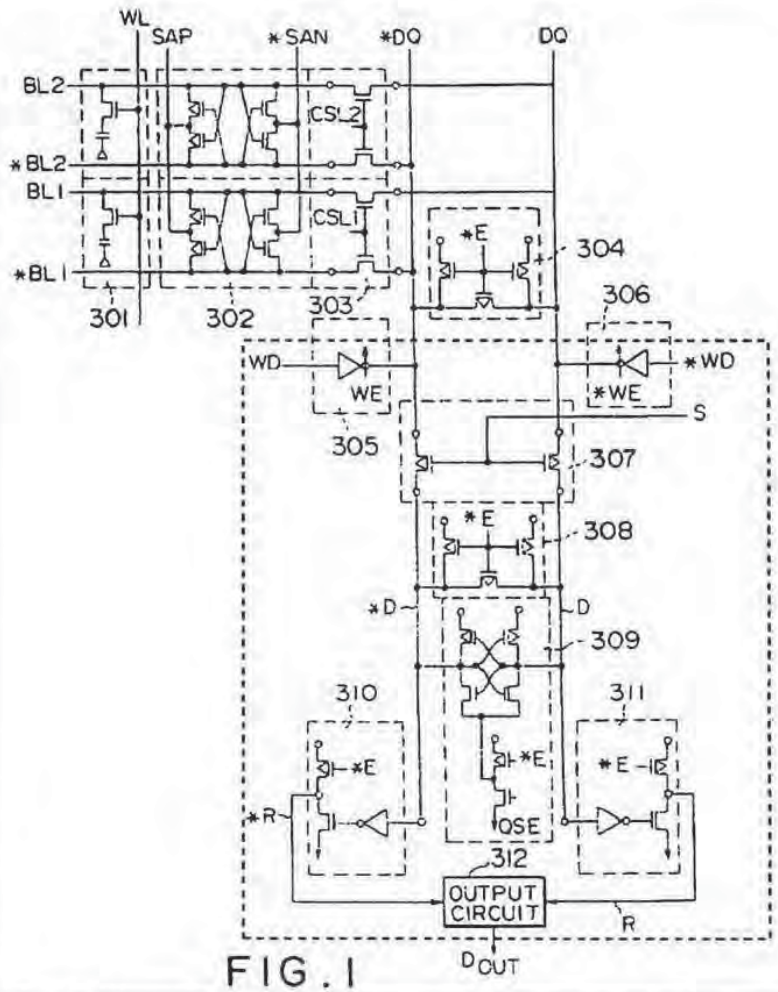
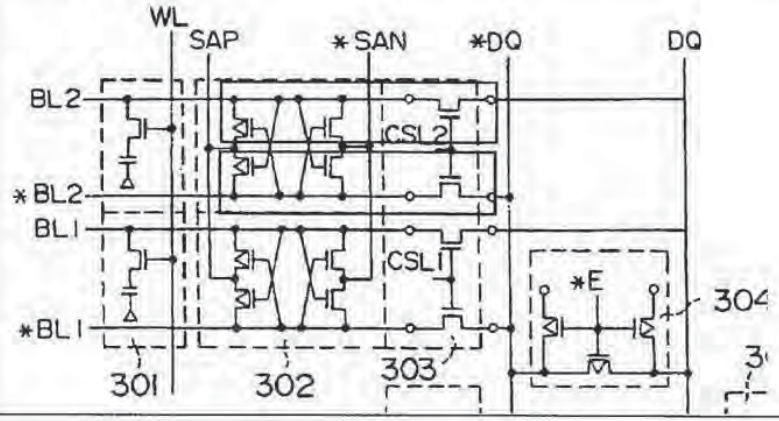


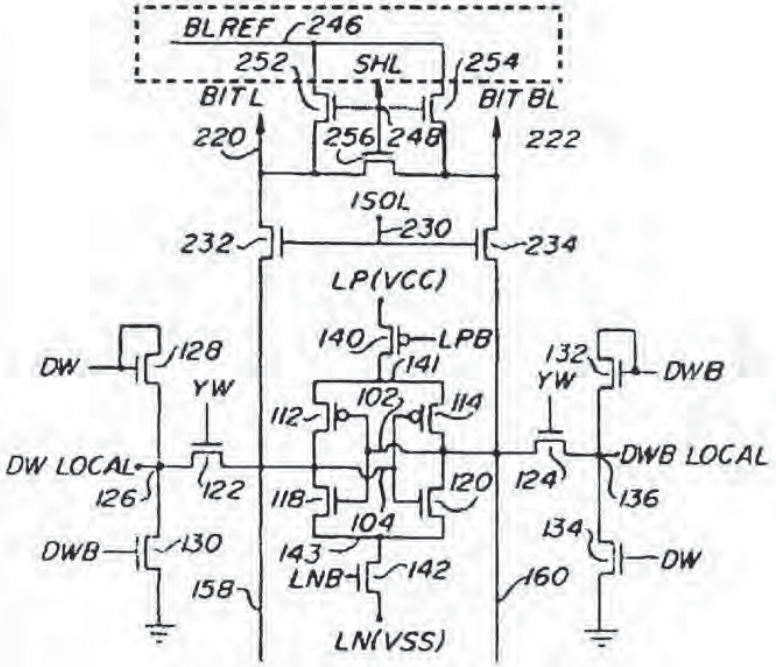
FIG. 1

wherein the latching sense amplifier comprises:	FIG. 1 of Koyanagi shows a cross-coupled latch circuit 309 coupled to a differential data bus D, which is coupled to the differential bus DQ by a switch circuit 307. The cross-coupled latch circuit 309 amplifies the differential voltage on the differential data bus pair D and *D when the

a first stage including a cross-coupled latch coupled to a differential data bus;	control signals *E and QSE are enabled. Koyanagi at 2:14-17.
and an output stage coupled to an output of said first stage; wherein the output of the first stage is coupled to an input of the output stage;	Element 311 in the Koyanagi latching sense amplifier is an output stage coupled to an output of the first stage 309. The differential data bus D is the output of the first stage 309, and is the input of the output stage 311. The conductive or non-conductive condition of the voltage transmission between D and R is controlled by *E. Koyanagi at 2:21-23.
wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.	As described above, Koyanagi discloses precharging of differential buses DQ/*DQ and D/*D to enable communication of data from the memory cell to an output. Notably, its precharge voltage is characterized as a high impedance condition, greater than zero and less than Vcc/Vdd. Koyanagi at 1:54-59.
Claim 2	
2. The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers.	FIG. 1 of Koyanagi shows two active pull-up and active pull-down bus drivers, as enclosed in dashed boxes below: 

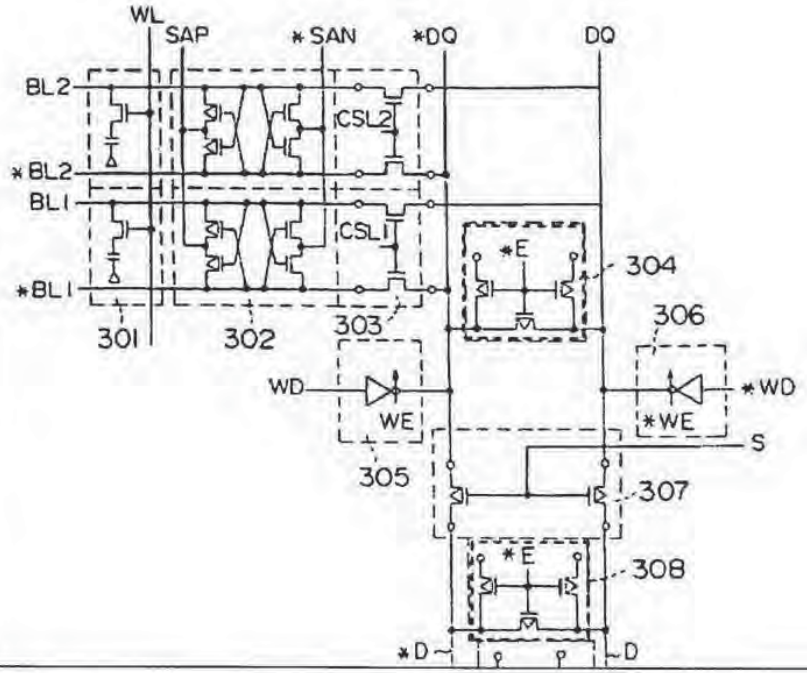
	These elements in combinations with control signals SAP and *SAN drive bus lines BL2 and *BL2. During a read operation, WL is enabled and the data in the memory cell is transferred to the true bus line BL2. The voltage difference between the bus lines BL2 and *BL2 is amplified by the two bus drivers. The voltage on one of the bus line BL2 or *BL2 is pulled up by the bus driver and the other bus line is pulled down accordingly. Koyanagi at 2:41-50.
Claim 5	
5. The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.	Koyanagi discloses the precharge voltage as a high impedance condition. Koyanagi at 1:54-59. **Hardee** FIG. 8 of Hardee shows two bus drivers, as indicated by dashed boxes below:

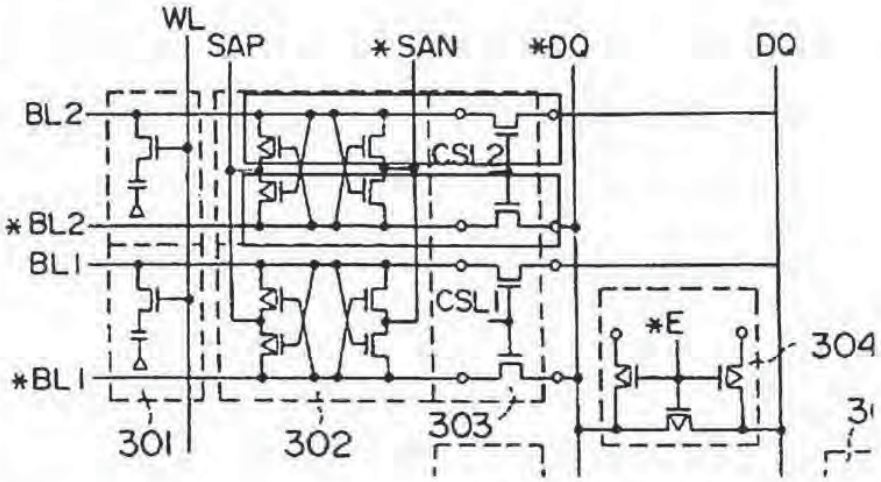
FIG. 8



Hardee discloses the BLREF reference input as a precharge source for the data lines 158, 160, 126, and 136, where the BLREF value is illustratively a constant voltage of ½ VCC. Hardee at 13:17-19. The transistors 252, 254, and 256 in Hardee are similar to the transistors in circuit 304 in Koyanagi.

It would have been obvious to modify Koyanagi's precharge source to a source with a constant voltage of ½ VCC. By connecting the precharge circuits 304 and 308 to ½ VCC, the differential voltage from the BL2 and *BL2 line pair is transferred to the differential bus pair DQ and *DQ with smaller voltage change on the differential bus pair DQ and *DQ, achieving the same benefit as disclosed in Hardee.

Claim 6	
6. The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.	FIG. 1 of Koyanagi shows a precharge circuit 304. The precharge circuit 304 is controlled by *E, and is connected to a high-impedance source. The output of the precharge circuit 304 is connected to the differential bus pair DQ and *DQ. When *E is enabled, the high impedance voltage is transferred to the differential bus pair DQ and *DQ to equalize the voltage between the two lines. The precharge circuit 308 is similar to 304 for precharging the differential data bus pair D and *D. 
Claim 7	
7. The data transfer arrangement in	The transistors of the pull up and pull down drivers as shown in FIG. 1 of Koyanagi include

accordance with claim 2 wherein the active pull up and pull down bus drivers are NMOS transistors.	both NMOS and PMOS transistors.  **Fujii** FIG. 5 of Fujii shows two bus drivers implemented with NMOS transistors. It would have been obvious to modify Koyanagi's bus drivers to include NMOS transistors because when there is a differential voltage on the sub-bit bus line pair, the bus drivers as disclosed by Fujii also raise the voltage on one of the sub-bit bus line pairs and lowers the voltage on the other sub-bit bus line.

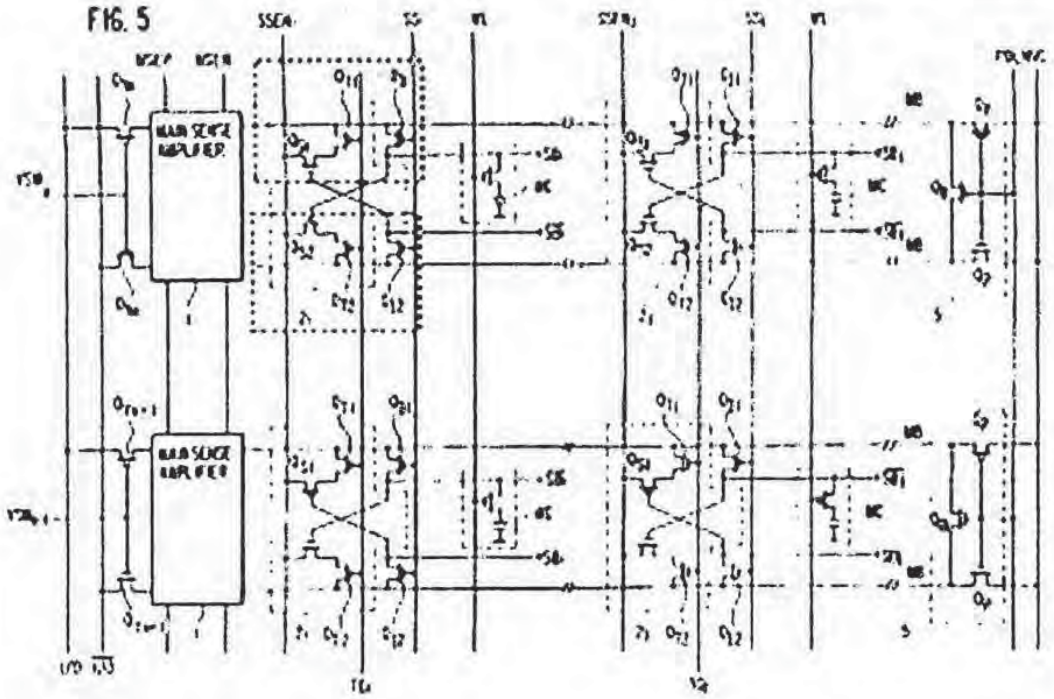


FIG. 5

VIII. SUMMARY OF GROUNDS FOR UNPATENTABILITY

For the forgoing reasons, the references listed in Section IV raise substantial and new questions of patentability with respect to claims of the '130 patent and show a reasonable likelihood that the Requester will prevail with respect to the claims challenged in the Request. These references each constitute prior art to the '130 patent and substantively render claims of the '130 patent unpatentable for the reasons discussed above. Moreover, the requested reexamination on these prior art references is both proper and necessary.

Respectfully submitted,

Dated: 1/19/2012

W. Karl Renner
Reg. No. 41,265

CERTIFICATE OF SERVICE

I hereby certify that on January 19, 2012, I caused a true and correct copy of the foregoing REQUEST FOR *INTER PARTES* REEXAMINATION UNDER 35 U.S.C. §§ 302 and 311 AND 37 C.F.R. § 1.902 *et seq.* to be served in its entirety via First Class Mail on the following attorney of record for the Third Party Requestor:

KILPATRICK TOWNSEND & STOCKTON LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-383

W. Karl Renner
Reg. No. 41,265

CERTIFICATE OF MAILING

I hereby certify that I mailed a true and correct copy of the foregoing REQUEST FOR *INTER PARTES* REEXAMINATION UNDER 35 U.S.C. §§ 302 and 311 AND 37 C.F.R. § 1.902 *et seq.* to the following attorney of record via First Class Mail:

KILPATRICK TOWNSEND & STOCKTON LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-383

Arlenette M. Footes

OFFICE ACTION IN INTER PARTES REEXAMINATION	Control No.	Patent Under Reexamination
	95/000,657	6366130
	Examiner	Art Unit
	DEANDRA HUGHES	3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:
Patent Owner on _____
Third Party(ies) on _____

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:
2 MONTH(S) from the mailing date of this action. 37 CFR 1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.956.
For Third Party Requester's Comments on the Patent Owner Response:
30 DAYS from the date of service of any patent owner's response. 37 CFR 1.947. NO EXTENSIONS OF TIME ARE PERMITTED. 35 U.S.C. 314(b)(2).

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

This action is not an Action Closing Prosecution under 37 CFR 1.949, nor is it a Right of Appeal Notice under 37 CFR 1.953.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892
2. ☒ Information Disclosure Citation, PTO/SB/08
3. ☐ _____

PART II. SUMMARY OF ACTION:

1a. ☒ Claims 1,2 and 5-7 are subject to reexamination.
1b. ☐ Claims 3,4 and 8 are not subject to reexamination.
2. ☐ Claims _____ have been canceled.
3. ☐ Claims _____ are confirmed. [Unamended patent claims]
4. ☐ Claims _____ are patentable. [Amended or new claims]
5. ☒ Claims 1, 2 and 5-7 are rejected.
6. ☐ Claims _____ are objected to.
7. ☐ The drawings filed on _____ ☐ are acceptable ☐ are not acceptable.
8. ☐ The drawing correction request filed on _____ is: ☐ approved. ☐ disapproved.
9. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has: ☐ been received. ☐ not been received. ☐ been filed in Application/Control No 95000657.
10. ☐ Other _____

INTER PARTES REEXAMINATION NON-FINAL ACTION

1. This is a non-final action in the *inter partes* reexamination of **claims 1-2 and 5-7** of USP 6,366,130. ("**'130 patent**")

2. **Claims 1-2 and 5-7** are rejected under 35 U.S.C. 102(b) as being anticipated by **Hardee** (EP 0597231A2 published May 18, 1994). The explanation of the rejection as set forth in the request for reexamination filed Jan. 19, 2012 on pages 11-13 and 19-30 is incorporated by reference.[1]

Conclusion

3. All correspondence relating to this *inter partes* reexamination proceeding should be directed:

By Mail to: Mail Stop *Inter Partes* Reexam
Attn: Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at:

https://efs.uspto.gov/efile/myportal/efs-registered

[1] The proposed rejection of claim 3 as anticipated by Hardee is excluded because it was determined in the Order that the anticipation rejection of claim 3 over Hardee did not have a reasonable likelihood of prevailing.

EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

/Deandra M. Hughes/
Primary Examiner, AU 3992

Conferees:

/James Menefee/
Primary Examiner, Art Unit 3992

MARK J. REINHART
CRU SPE-AU 3992

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of Podlesny et al.	)	
	)	
INTER PARTES REEXAMINATION	)	Art Unit: 3992
of	)	
U.S. Patent No. 6,366,130	)	Examiner: HUGHES, Deandra M.
	)	
Control No. **95/000,657**	)	
	)	
Reexamination date: Jan. 19, 2012	)	
	)	
Patent Issue Date: April 2, 2002	)	Atty. Dkt. No. Cascade-130
	)	
For: HIGH SPEED LOW POWER	)	
DATA TRANSFER SCHEME	)	
	)	

DECLARATION OF DR. PHILIP KOOPMAN

1. My name is Philip Koopman of 5672 Melvin Street, Pittsburgh PA 15217. I have been retained to offer technical opinions with respect to the prior art references cited in this reexamination. I base these opinions on my education and training in electrical engineering, computer engineering and semiconductor systems described below.

2. I am familiar with the content of United States patent number 6,366,130 ("the Podlesny patent") and the present reexamination (control number 95/000,657). In particular, I am familiar with the art the examiner is citing against the claims, and I have read and studied this art for purposes of this declaration.

3. I hold a Ph.D. degree in Electrical and Computer Engineering from the Carnegie Mellon University (1989), an M.Eng. degree in Computer Engineering from Rensselaer Polytechnic Institute (1982), and a B.S. degree in

Electrical Computer & Systems Engineering from Rensselaer Polytechnic Institute (1982). I am a Senior Member of the IEEE and a Senior Member of the ACM.

4. I currently hold the position of Associate Professor with tenure of Electrical and Computer Engineering at Carnegie Mellon University, Pittsburgh PA. Previous positions include Principal Research Engineer at United Technologies Research Center (East Hartford CT), Senior Scientist at Harris Semiconductor (Melbourne FL), Founder at WISC Technologies (CPU design startup, La Honda CA), and an officer in the US Navy (Newport RI and US Pacific Fleet).

5. I have conducted extensive research in the areas of CPU design, memory system design, embedded computer systems, embedded networking, and dependable embedded computing among others. My relevant experiences include manual layout of VLSI integrated circuits at the transistor level, design of CPUs (discrete logic and VLSI, including memory interface logic), and printed circuit board design for microcontrollers including CPU and memory chips. At the time the '130 patent was filed I had recently taught a graduate course on memory systems that included the topics of memory device implementation, memory interface design, and high speed data bus design.

6. I am a named inventor on 26 issued US patents in a variety of areas of computer design and application. I have also acted as an independent engineering/patent consultant since 1996.

7. My hourly rate in this case is $580 per hour.

8. I am familiar with the Podlesny patent number 6,366,130 and the Hardee Published Patent Application number EP 0597231 A2 ("the Hardee reference") cited by the requester and the examiner in this case. I am also familiar with the status of this reexamination, the arguments made by the third party requester, and the Examiner's rejection contained in the non-final office action issued March 2, 2012.

9. My understanding is that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference or embodied in a single prior art device or practice. Moreover, the reference must describe the applicant's claimed invention sufficiently to have place a person of ordinary skill in the field of the invention in possession of it. With this definition in mind, it is my opinion that the Hardee reference does not anticipate Podlesny.

10. The Podlesny patent issued April 2, 2002, is related to a data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus connected to a pre-charge voltage source, and a two-stage sense amplifying latch.

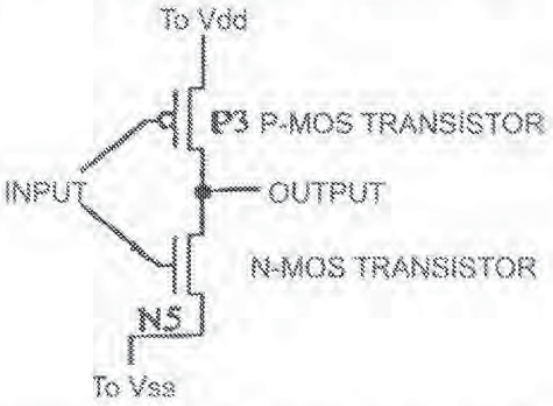
11. The Hardee reference concerns a sense amplifier for a high-density integrated circuit memory using CMOS technology. Hardee differs from Podlesny in many respects. Among the high level differences are: Hardee teaches only a single-stage latch, and Hardee teaches precharging of only one of two differential buses. Additionally, the Hardee reference omits key information as to the operation of the circuit, making it impossible for a practitioner of ordinary skill in the art to use it in a way that meets all of the Podlesny claim limitations.

THE PODLESNY PATENT

12. The Podlesny patent describes a differential data bus driven by DT/DC differential inputs through a pair of CMOS drivers.

13. As a beginning point, it must be understood that the term CMOS stands for Complimentary Metal Oxide Semiconductor, and that CMOS circuits are constructed using two types of transistors: P-MOS transistors and N-MOS transistors. A P-MOS transistor conducts when its input is a logic low (hence the bubble on its gate in the pictorial representation shown in the next paragraph). An N-MOS transistor conducts when its input is logic high (no bubble on its gate).

14. An annotated excerpt of Figure 2 of the Podlesny patent shows an inverter circuit constructed with an example of each type of transistor:



In this figure the top transistor (P3) is a P-MOS transistor that turns "on" when the input is low, and the bottom transistor (N5) is an N-MOS transistor that turns "on" when the input is high. If we assume that the top of the transistor "stack" is connected to the positive power supply (Vdd) and the bottom is connected to ground (Vss), this configuration of transistors forms an inverter gate in which an input that is one (high voltage) is transformed and amplified to create an output

that is zero (low voltage). Similarly, an input that is zero results in an output that is one.

Podlesny Figure 1

15. While it is common to see a inverting "stacks" of P-MOS and N-MOS transistors for most gates, such pairs are not necessary to create functioning chips. N-MOS transistors without corresponding P-MOS transistors can be used as "pass gates" to couple two wires, passing values when turned on, but isolate the transistor source and drain from each other when turned off. Figure 1 of the Podlesny patent, reproduced below, shows this technique of using only N-MOS transistors used as pass transistors:

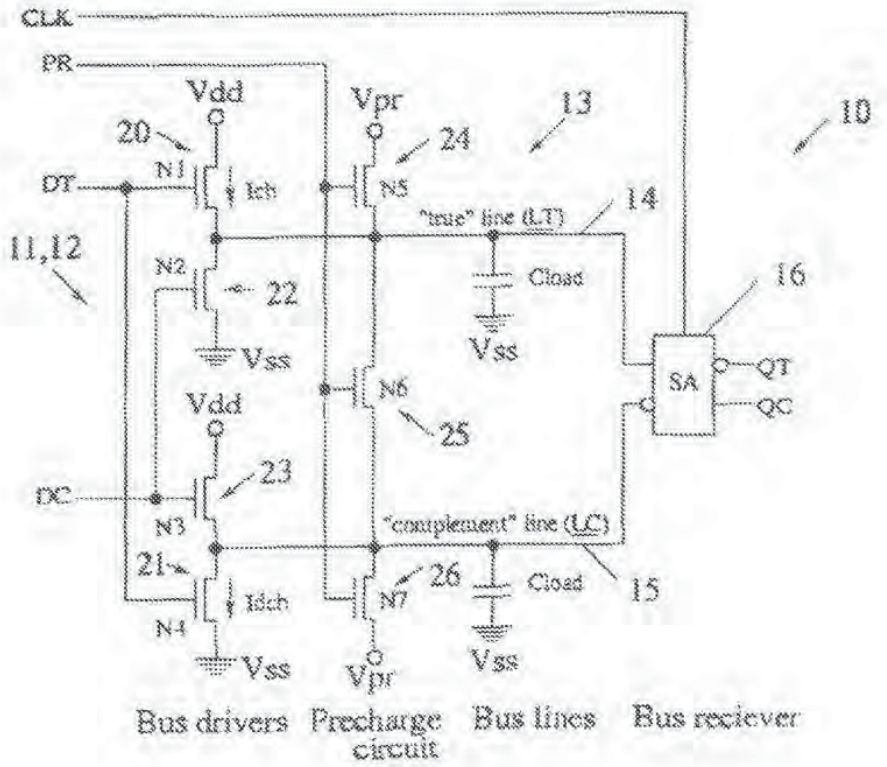


FIG.1.

16. Podlesny Figure 1 has two phases of operation. In the first, precharging, phase inputs DT and DC are both assumed to be low, turning off transistors N1, N2, N3 and N4. During this first phase transistors N5, N6, and N7 are all turned on by the PR signal, precharging the LT line 14 and LC line 15 to a defined intermediate voltage Vpr. (Podlesny 2:1-22) The figure below has been annotated to show this precharge phase:

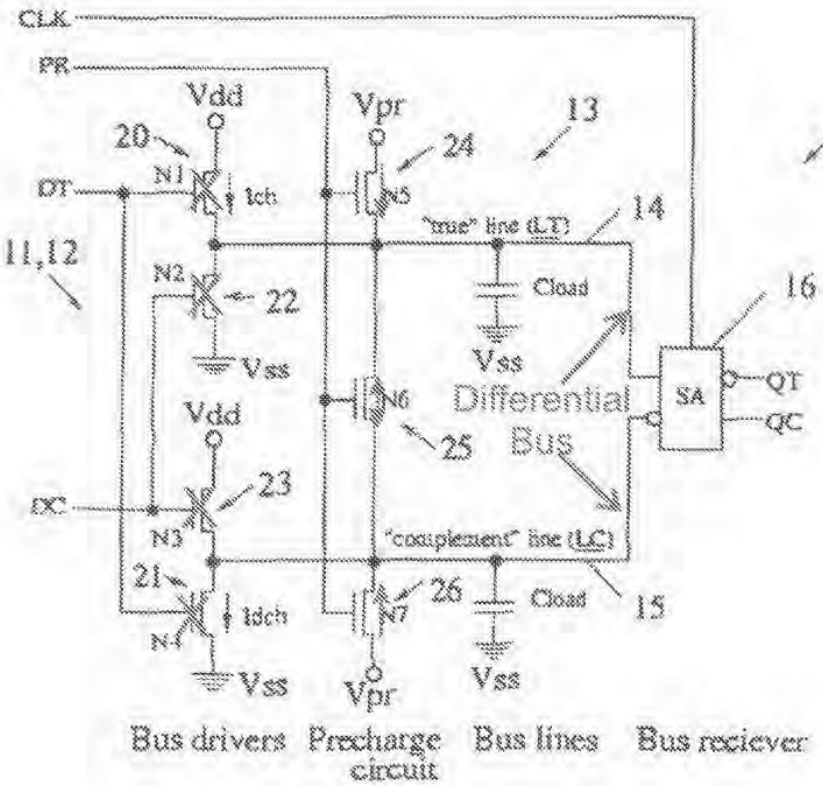


FIG.1.
PRECHARGE PHASE

17. During a second phase of operation DT and DC (11, 12) provide an input voltage difference that is being sensed as an incoming data value. Transistors N5, N6, and N7 are all off during this phase, but the capacitance Cload causes the LT 14 and LC 15 lines to retain their precharge voltages for the

short period it takes for DT and DC transition between both being low (first phase) and providing a voltage difference (this second phase). The DT and DC signals control transistors N1, N2, N3, and N4. Transistors N1 and N4 turn on more strongly if the DT line has a higher voltage than the DC line, driving LT 14 high and LC 15 low. On the other hand, transistors N2 and N3 turn on more strongly if the DC line has a higher voltage than the DT line, driving LT low and LC high. These outputs provide a pre-amplified differential signal into the Sense Amp 16). The result is that the Sense Amp 16 sees an amplified signal with minimized delay (Podlesny 2:23-38). The annotated figure below shows this second phase of operation:

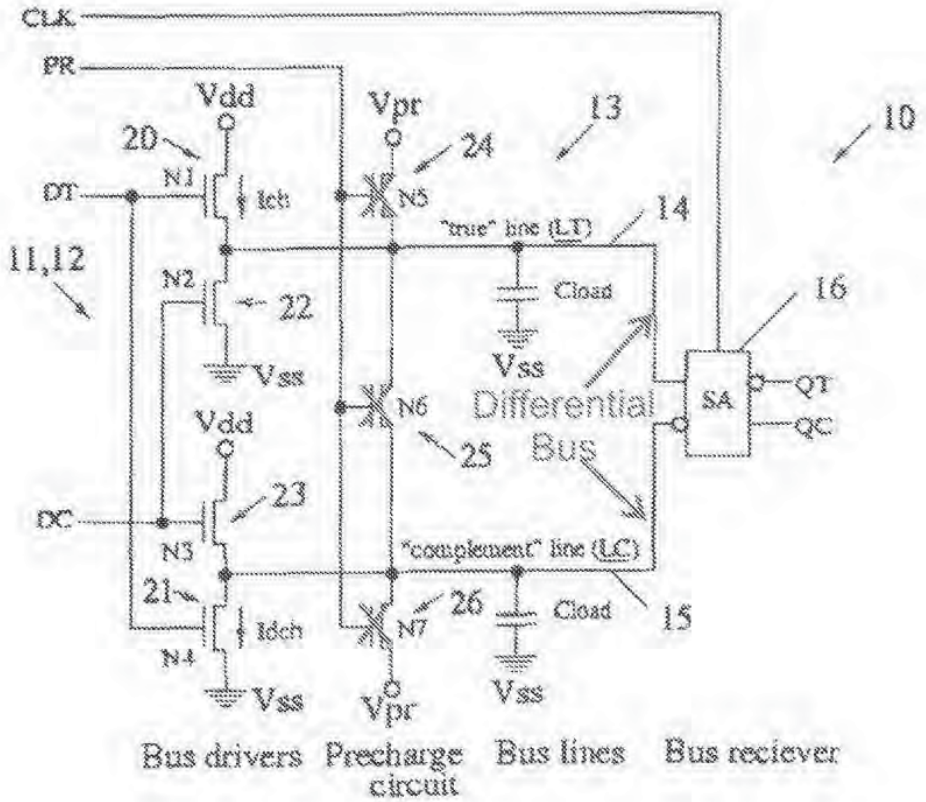
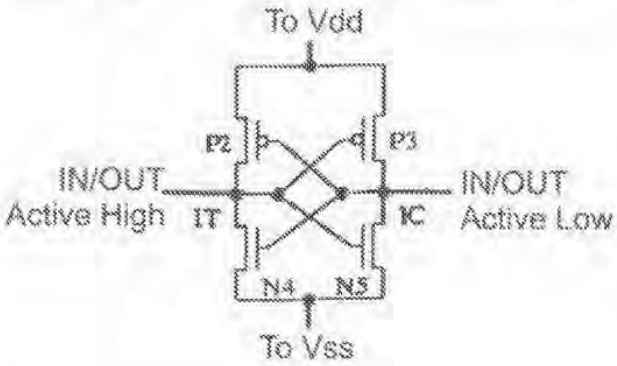


FIG.1.
DATA RECEIVE PHASE

18. In summary, Figure 1 shows a circuit that has a precharge phase and a data receive phase, transforming a differential signal from the pair of inputs DT and DC into a differential output pair LC and LT that are fed into Sense Amp 16. The "differential bus" of '130 patent claim 1 corresponds to the differential pair LT 14 and LC 15.

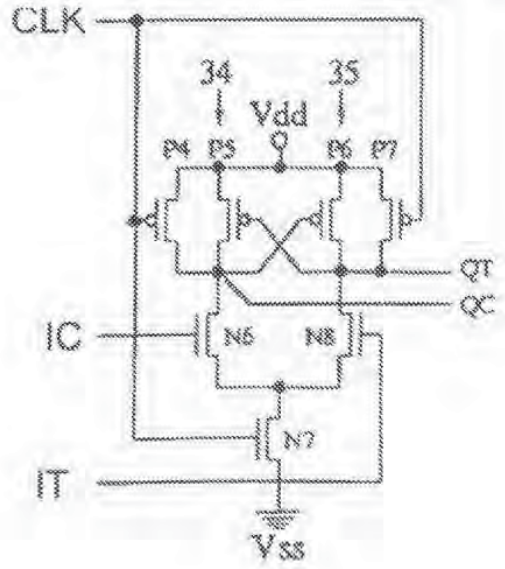
Podlesny Figure 2

19. Fig. 2 of the Podlesny patent illustrates the Sense Amp 16. Within this figure is a static cross-coupled CMOS latch containing two CMOS inverter pairs (four transistors in all), which looks like this (with annotations added):



This circuit is a bistable latch (sometimes known as a flip-flop). Assuming that IT and IC are inverse values (for example, IT is zero and IC is one), feedback within the circuit will retain its value with opposite outputs for IT and IC as long as power is applied. While it is common to change the value in a latch such as this by over-riding the IT and IC values with stronger transistors to force changes, the Podlesny invention instead changes values by isolating the circuit from Vdd and Vss and performing a precharge operation.

20. The bistable latch shown above is part of an input stage to the Sense Amp. Podlesny additionally teaches a second, output stage cross-coupled latch shown below with annotations showing the CLK, IC, and IT inputs:



This is a domino-style clocked latch, which precharges on a first clock phase (CLK low) then discharges only one side of the cross-coupled latch on a second clock phase (CLK high) when N7 turns on, connecting the bottom of the latch to ground. The feedback of QT and QC to the gates of transistors P5 and P6 latches the complementary output values QT and QC given complementary input values IC and IT. (Podlesny 3:4-11 discusses this domino output stage.)

21. The entirety of the Sense Amp circuit shown in Podlesny Figure 2 below:

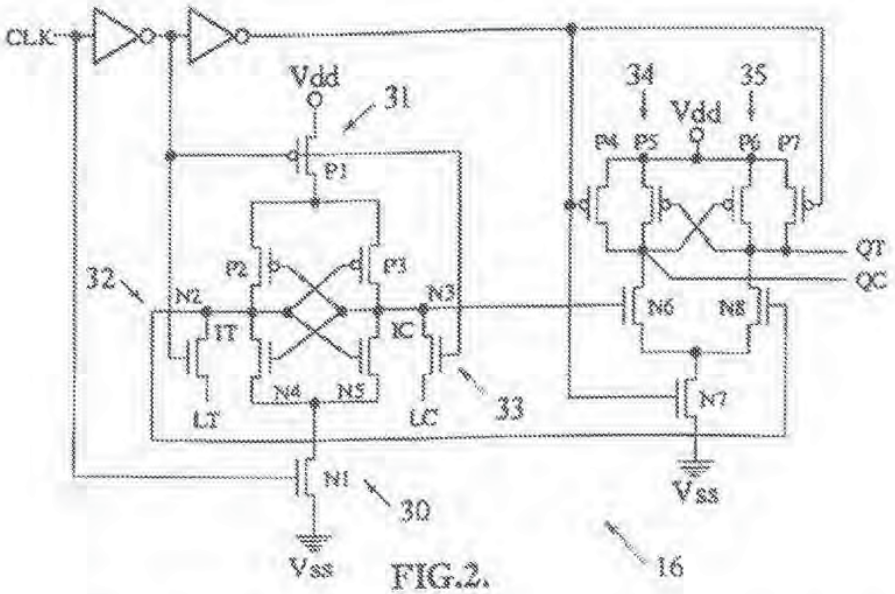


FIG.2.

22. The Podlesny Sense Amp circuit functions in two phases as follows. The figure below is annotated to show the first, precharge phase:

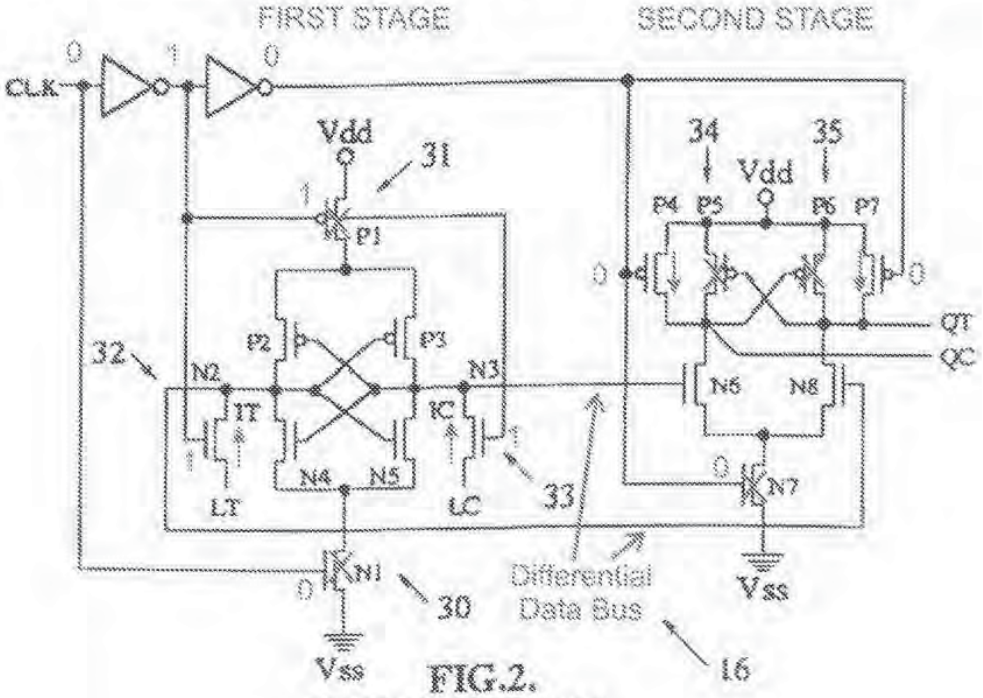


FIG.2.
PRECHARGE PHASE

In the precharge phase, CLK is 0, which turns off N1, P1, P5, P6 and N7, isolating the first stage from power and ground, and also isolating the second stage from Vss (ground). CLK also turns on P4 and P7, which precharges outputs QT and QC to 1 by connecting them to Vdd. CLK also connects the first stage to the LT and LC inputs, which precharges the Differential Data Bus. (Podlesny 2:39-59)

23. The second phase of sense amp operation is the data transfer phase:

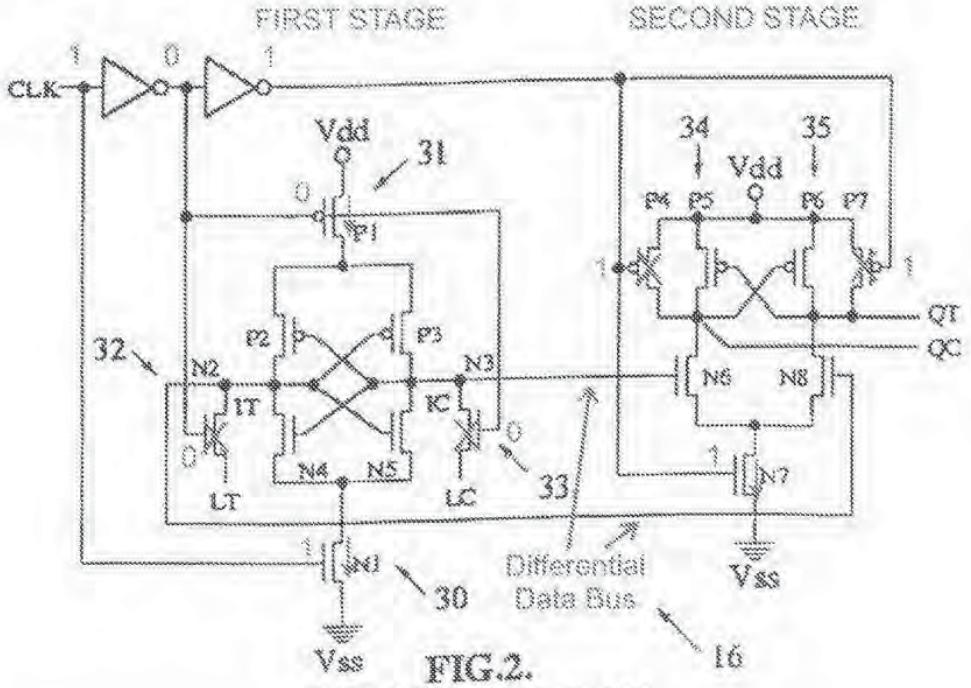


FIG.2.
DATA TRANSFER PHASE

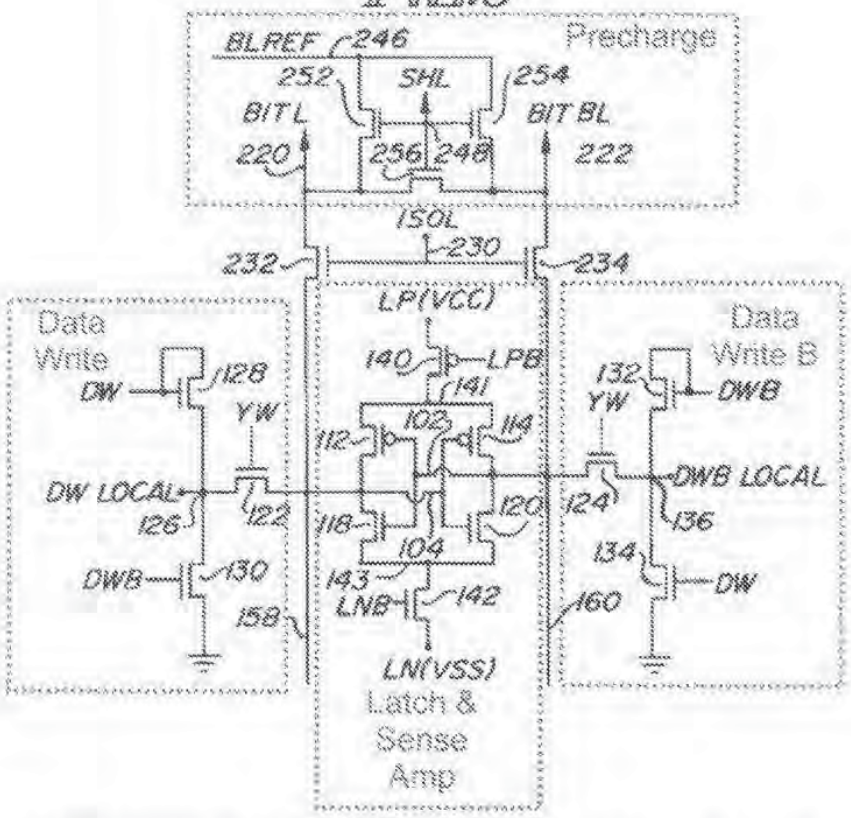
In the data transfer phase, CLK is 1, which turns on N1, P1, and N7 while turning off N2, N3, P4, and P7. This implements a "domino"-style CMOS circuit in which the second stage outputs are both charged to 1 during the precharge phase, and then only one output (QT or QC depending upon the values of LT and LC) is pulled down to a zero during the data transfer phase (Podlesny 2:60-3:11)

24. In summary, the Podlesny invention includes two distinct differential data buses, each of which is precharged and then operated to transfer a data value in alternation. It also includes a two-stage latch, with each stage having cross-coupled feedback.

THE HARDEE REFERENCE

25. The Hardee reference concerns a sense amplifier for a high-density integrated circuit memory using CMOS technology. The relevant portion of Figure 8 of Hardee is shown below for reference. The bottom portion of the figure that depicts a read circuit and a redundant access circuit has been omitted as was done in the Reexamination Request:

FIG. 8



The figure has been annotated with dashed boxes to point out the Precharge

circuitry, the Latch & Sense Amp circuit, and the two complementary Data Write circuits (Data Write and Data Write B). The differential bus is alleged to be the differential pair 126/136 (Reexamination Request page 21). The differential data bus is alleged to be the differential pair 158/160 (Reexamination Request page 22).

26. There are additional reading circuits shown in the original Fig 8 (including transistors 150, 152, 154, 156). The fact that these were intentionally removed from the figures included in the Reexamination Request is tacit admission that they – and reading operations overall – are irrelevant to the arguments presented in that Request. In particular, during read operations the signal YW is low, turning off transistors 122 and 124, decoupling the data write buffers from the bit lines.

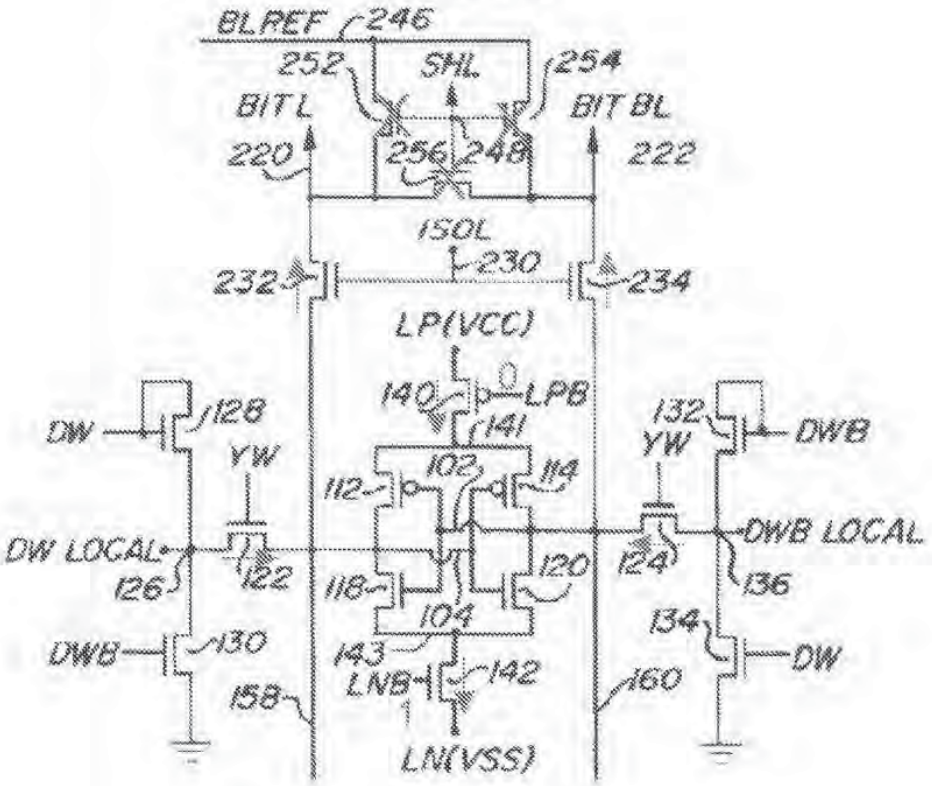
27. The general operation of Hardee Fig 8 writing to a memory cell is as follows (Hardee Fig 8 and 14:38-15:11). YW turns on transistors 122 and 124 (Hardee 14:29). DW and DWB are then activated for a particular sense amp and drive complementary values onto DW LOCAL 126 and DWB LOCAL 136 (Hardee 14:43-50). These data write signals pass through transistors 122 and 124, forcing the latch into a corresponding value (Hardee 14:50-54).

28. The values of SHL and the precharge circuits are not mentioned by Hardee in the context of writes, and a practitioner of ordinary skill in the art would have appreciated that precharging would NOT have been performed for writes for reasons that will be discussed in subsequent paragraphs. Similarly, the value of ISOL is not mentioned in the context of writes, but a practitioner would

probably have assumed that the ISOL transistors were turned on if that is the side of the array that was being written (with ISOL turned off but ISOR turned on if the other side were to be written).

29. The Hardee Fig. 8 copy below has been annotated to show write operations. Note that the values for LPB and LNB are *speculative* as describe below – Hardee does not teach what these values should be for write operations:

FIG. 8



Write Operation

30. Given that understanding of operation, the following errors in the claim chart presented in the Reexamination Request become apparent.

THE HARDEE REFERENCE CANNOT ANTICIPATE CLAIMS 1 OF THE PODLESNY PATENT

HARDEE DOES NOT TEACH PRECHARGE BEFORE WRITE

31. On page 12 of the Reexamination Request it is alleged that a *write* operation involves first enabling YW, turning on transistors 122, 124, then activating the precharge circuit. While references from Hardee are given for many other points of the narrative stated, *no* reference from Hardee is given for the combination of enabling YW and then enabling precharge (which would require enabling SHL). That is because ***there is no such reference in Hardee***! Hardee does not teach precharging while YW is enabled. Hardee only teaches precharging for a read, and the operating being discussed is for a write. During writes, YW is disabled, decoupling nodes 126/136 from the bit lines. Also, in no case does Hardee teach precharging any other bus in any mode, and in particular, Hardee does not teach or suggest ever precharging the DW or DWB lines as is stated on p. 12 of the Reexamination Request.

32. While the differential data bus 158/160 is precharged during read operations, there is no requirement in Hardee that a read be performed before every write, or for that matter that a read ever be performed. Writes must therefore work without precharging. Thus, Hardee does not teach precharging before writes.

DIFFERENTIAL BUS NOT COUPLED TO PRECHARGE SOURCE IN HARDEE

33. On page 21 of the Reexamination Request, it is alleged that "a differential bus coupled to the bus drivers and to the voltage precharge source" is

satisfied by node 126 being coupled to BLREF "when control signals YW, SHL, and ISOL are high." There is no time during a write when this is true, and Hardee contains no suggestion that this would be a desirable mode of operation.

34. Hardee does not teach SHL being high during a write operation. The operation of SHL is only mentioned in the context of a read operation, which has been tacitly admitted by the Reexamination Request to be irrelevant for purposes of this discussion by the omission of read circuitry from the copy of Fig. 8 and the omission of any mention of read operations.

35. A practitioner of ordinary skill in the art would have appreciated that SHL should be low during a write operation for the following reasons. First, precharge is intended to make it easier for a relatively weak voltage source resident in a memory bit to induce a slight voltage imbalance that can be read by a sense amplifier. That is the reason the sense amplifier is in the circuit. During writing there is a direct connection to a strong voltage source (via the Data Write blocks mentioned previously), so precharging is unnecessary and would be avoided to minimize power consumption.

36. Second, Hardee states that the first thing that happens during a write operation is that YW is turned on. If precharging were to be attempted at some point after this, it would lead to a short between BLREF and Ground via transistors 252, 232, 122, and 130, dissipating power and potentially damaging the chip. Analogous reasoning applies to the path through transistors 254, 234, 124, and 134.

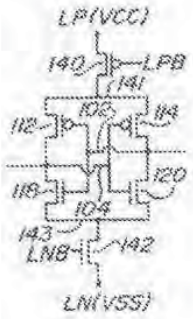
37. In other words there is no reason to perform a separate precharge cycle, and once a write starts, attempting to precharge from BLREF would be a bad idea. For these reasons, SHL has to be zero during writes, which isolates the BIT L and BIT BL bus from the precharge voltage and prevents precharging. There is a separate write-back operation possible during reads (Hardee 14:20-23), but during this operation it is essential that YW be false to prevent DW and DWB from over-writing the value that is being refreshed. Therefore this write-back operation is not relevant to the discussion at hand.

38. Based on the above reasoning and taking Hardee as a whole, it is my opinion that during write cycles the differential bus is not coupled to the voltage precharge source.

LATCHING SENSE AMP NOT COUPLED TO DIFFERENTIAL BUS IN HARDEE

39. On page 21 of the Reexamination Request, it is alleged that "a latching sense amplifier coupled to the differential bus" is satisfied by the Latch & Sense Amp show in the preceding figure. However, during the write cycle Hardee does not teach this circuit operating as a latching sense amp.

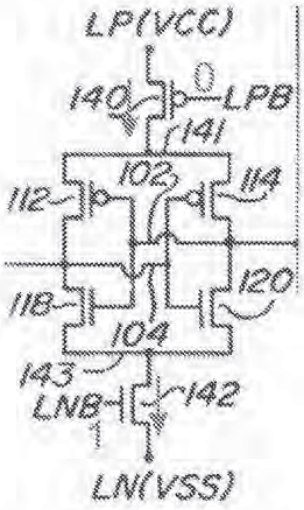
40. The relevant latch and sense amp portion of Hardee Figure 8 is shown below:



CMOS transistor pairs 112,118 and 114,120 are the two inverters that form a latching sense amp, with transistors 140 and 142 controlling the latching function.

41. While operation of the sense amp is described for reads, Hardee does not specify the values of LPB and LNB during a write operation. Thus, a practitioner of ordinary skill in the art would be forced to speculate as to how the latch operates during a write. It is clear that these signals are manipulated during reads (Hardee 13:24-35) and are not statically set values. But there is no mention as to their values during writes. I shall speculate as to an illustrative possibility, but it is impossible to know with certainty what Hardee had in mind for this operation.

42. In my opinion the most likely speculative possibility is that LPB is low and LNB is high during the entire write operation. This connects node 141 to power and node 143 to ground, forming a classical bistable latch:



43. This means that the "sense amp" circuit is not operating as a sense amp at all, but is merely operating as a latch during writes. This possibility seems the most likely one to me because Hardee talks about forcing the bit line

voltages: "This differential voltage that is forced on the DW Local nodes will – since YW is high – actually flip the latch and drive the bit lines, one to VCC and one to ground." (Hardee 14:50-54). One does not "force" a sense amp; indeed the whole point of a sense amp is to be exquisitely sensitive to a voltage difference without having to force the sense amp in any significant regard. Moreover, a sense amp works by being at an indeterminate value and then being amplified into a more distinct value – no "flip" is involved, and the word "flip" would only make sense in this context if it is referring to a bistable latch. It should be noted that this is mere inference and what Hardee really had in mind cannot be determined with certainty, and would not be readily apparent to a practitioner of ordinary skill in the art.

44. Given the strong drive provided by transistors 128, 130, 132 and 134, there is no other mode of operation I can envision that would have the "latching sense amp" operating as an actual sense amp. In my opinion it is acting as a latch in this scenario regardless of whether my conjecture as to operation is correct.

45. Therefore, during a write operation the "sense amp" circuit taught by Hardee is being operated as a latch, not as a "latching sense amp" as required by the Podlesny claims. As a result, it is my opinion that during a write operation there is no latching sense amplifier coupled to the differential bus, but rather the circuit is configured to provide just a latch with no sense amplifier functionality.

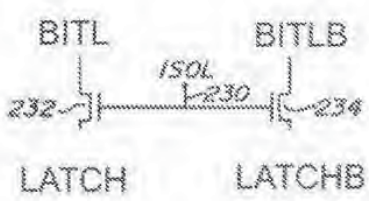
NO LATCH OUTPUT STAGE IN HARDEE

46. On page 23 of the Reexamination Request, it is alleged that the Hardee sense amplifier contains an "output stage coupled to an output of said first stage" as recited in Podlesny Claim 1. The Reexamination Request states: "Specifically, the output stage includes two isolation transistors 232 and 234 controlled by the ISOL signal. The differential voltage pair 158 and 160, at the output of the first stage, serve as the input of this output stage. Hardee at 14:19-23."

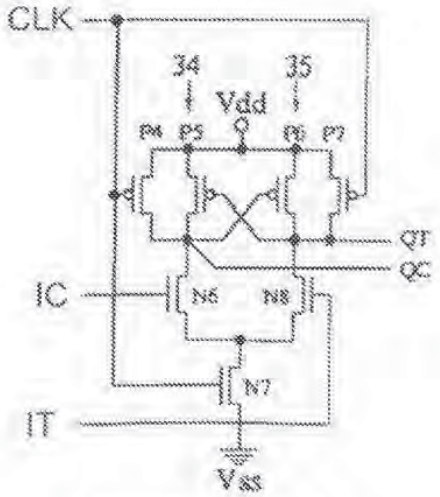
47. First of all, the operations described in Hardee 14:19-23 are in the context of a read cycle that may be refreshing the bit value after it has been read, but during which the bus drivers are isolated from the bit lines due to the YW signal being low and turning off transistors 122 and 124. It therefore does not apply to a write cycle, and therefore irrelevant to the discussion.

48. More importantly, the transistors involved are "isolation transistors" as stated by the Reexamination Request itself, and not a second stage of a latch. The isolation transistors from Hardee and the cross-coupled second latch stage from Podlesny are shown together side-by-side for reference below (with

annotations for clarity):



Hardee Fig. 8
Isolation Transistors



Podlesny Fig. 2
Second Latch Stage

49. The Hardee isolation transistors do not have any cross-coupled feedback, so they cannot retain a fixed value despite changing inputs, which is the essential property of any latch device. For that matter they don't have a connection to power and ground, a clock input, or any other ability to retain values. Rather, they are just a pair of pass transistors that pass signals in either direction rather than in a single "output" direction. Any practitioner of the art would recognize that the Hardee isolation transistors are not a second latch stage. They are simply a pair of isolation transistors as admitted by the Reexamination request.

50. Podlesny Col. 3 points out some of the advantages of using a second latch stage rather than simple isolation transistors, such as avoiding leakage currents and output glitches (Col 3:4-11). Therefore, it is clear that a

second latch stage in the context of the Podlesny specification is more than a mere pair of isolation transistors.

51. Based on the above, it is my opinion that Hardee does not teach the required claim element of an "output stage coupled to an output of said first stage."

DATA BUS AND DIFFERENTIAL DATA BUS NOT PRECHARGED IN HARDEE

52. On page 23 of the Reexamination Request, it is alleged that the differential bus and differential data bus are precharged. The reasoning given quotes Hardee: "[t]ransistors 252 and 254 have their source-drain paths connected between the bit line reference BLREF at node 246 and the bit lines 220, 222, respectively, and will therefore, when turned on, couple the bit line reference voltage to the bit lines themselves. (Hardee at 13:5-19)" However, what the Reexamination Request does ***not*** say is that this is in the context of ***read*** operations, and that this requires SHL to be on, which does not happen during writes. Since the data write buffers are only connected to the bit lines via transistors 122 and 124 during write operations, this quoted statement is irrelevant. In particular, during read operations the YW signal (which is a ***write*** signal) is off, which makes it impossible for this precharge voltage to reach nodes 126 and 136 (alleged to be the differential bus), because they are not coupled.

53. For the above reasons, it is my opinion that the Hardee reference does not teach precharging the differential bus as required by Podlesny claim 1.

54. As to the differential data bus (158/160), this can be precharged during read operations, but is not taught to be precharged during write operations

as discussed previously. Therefore, it is my opinion that the Hardee reference does not teach precharging the differential data bus as required by Podlesny claim 1.

CLAIM 1 SUMMARY

55. A significant source of confusion in the Reexamination Request is the improper combination of two distinct modes of operation – reading and writing. When the circuit is reading the alleged bus drivers (transistors 128, 130, 132, 134) are decoupled from the bit lines. When writing, the precharge circuit is decoupled from the bit lines. The description on pages 11-13 of the Reexamination and corresponding claim chart tries to have it both ways – asserting that the circuit is both reading and writing at the same time, which any practitioner would recognize is nonsensical, and is not what is taught by Hardee.

56. In summary, the Hardee reference cannot anticipate Claim 1 of the Podlesny patent for at least the following reasons. Hardee does not teach a differential bus coupled to the voltage precharge source. Hardee does not teach a latching sense amplifier coupled to the differential bus combined with two bus drivers. Hardee does not teach an output stage of the latching sense amplifier. Hardee does not teach precharging a differential data bus. Hardee does not teach precharging a data bus in combination with the claim element of two bus drivers.

THE HARDEE REFERENCE CANNOT ANTICIPATE CLAIMS 1, 2, 5, 6 OR 7 OF THE PODLESNY PATENT.

57. Claims 2, 5, 6, and 7 of the Podlesny patent all depend directly or indirectly on claim 1. Because it is my opinion that the Hardee reference does not anticipate claim 1 of the Podlesny patent, it is therefore also my opinion that claims 2, 5, 6, and 7 also are not anticipated by the Hardee reference.

58. In summary, it is my expert opinion that the Hardee reference cannot anticipate claims 1, 2, 5, 6 or 7 of the Podlesny patent for at least the following reasons. Hardee does not teach a differential bus coupled to the voltage precharge source as required by Podlesny claim 1. Hardee does not teach a latching sense amplifier coupled to the differential bus combined with two bus drivers as required by Podlesny claim 1. Hardee does not teach an output stage of the latching sense amplifier as required by Podlesny claim 1. Hardee does not teach precharging a differential data bus as required by Podlesny claim 1. Hardee does not teach precharging a data bus in combination with two bus drivers as required by Podlesny claim 1.

59. I hereby declare that the above is true to the best of my knowledge.

Signature: Philip Koopman Date: April 29, 2012

Philip Koopman, Ph.D.

CERTIFICATE OF SERVICE IN COMPLIANCE WITH 37 C.F.R. 1.903

The undersigned certifies that copies of all papers herein attached and/or being electronically filed have been served on counsel for the requesting party via first class mail at:

W. Karl Renner
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1425 K St. #1100
Washington D.C. 20005

in accordance with 37 C.F.R. §§ 1.903, 1.248 on this 1st day of May 2012.

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Facsimile: 630 428-0104

CUSTOMER NO. 74642

By /clifford kraft/
Clifford H. Kraft
Reg. No. 35,229

Electronic Patent Application Fee Transmittal

Application Number:	95000657
Filing Date:	19-Jan-2012
Title of Invention:	HIGH SPEED LOW POWER DATA TRANSFER SCHEME
First Named Inventor/Applicant Name:	6366130
Filer:	Clifford H. Kraft
Attorney Docket Number:	19968-0006RX1

Filed as Large Entity

inter partes reexam Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Reexamination claims in excess of 20	1822	4	60	240
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**240**

Electronic Acknowledgement Receipt	
EFS ID:	12672202
Application Number:	95000657
International Application Number:	
Confirmation Number:	8472
Title of Invention:	HIGH SPEED LOW POWER DATA TRANSFER SCHEME
First Named Inventor/Applicant Name:	6366130
Customer Number:	74642
Filer:	Clifford H. Kraft
Filer Authorized By:	
Attorney Docket Number:	19968-0006RX1
Receipt Date:	01-MAY-2012
Filing Date:	19-JAN-2012
Time Stamp:	12:08:32
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$240
RAM confirmation Number	11725
Deposit Account	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Response after non-final action-owner timely	130_reexam_1st_OA_response_final.pdf	664123 971054ecf9a8de26f68654d8ae24ace87c731c4c	no	20
Warnings:					
Information:					
2	Rule 130, 131 or 132 Affidavits	KOOPMAN_v5.pdf	6842587 412896107af4a17b4070a6dc267f54d1e956e843	no	24
Warnings:					
Information:					
3	Reexam Certificate of Service	certificate.pdf	14961 6bbae325abec010dfef849cfed0279a46e574fa	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30076 4ca3430e7c18fcaf1506daf199bfc399e26a6ac3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	7551747		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of Podlesny et al.	)	
	)	
INTER PARTES REEXAMINATION	)	Art Unit: 3992
of	)	
U.S. Patent No. 6,366,130	)	Examiner: HUGHES, Deandra M.
	)	
Control No. **95/000,657**	)	
	)	
Reexamination date: Jan. 19, 2012	)	
	)	
Patent Issue Date: April 2, 2002	)	Atty. Dkt. No. Cascade-130
	)	
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	)	
	)	

Response to Non-Final Office Action and Amendment

Mail Stop: *Inter Partes* Reexamination
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Honorable Commissioner:

Kindly accept this patent owner's response to the non-final office action issued March 2, 2012.

I. AMENDMENTS TO THE CLAIMS

Kindly add the following new claims:.

Claim 9. (new): The data transfer arrangement of claim 1 wherein the differential bus is precharged to a different voltage than the differential data bus.

Claim 10. (new): The data transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback.

Claim 11. (new): The data transfer arrangement of claim 1 wherein the differential bus is precharged on a different clock phase than the differential data bus.

Claim 12. (new): The data transfer arrangement of claim 1 wherein the differential bus and the differential data bus are separate circuits.

II. REMARKS

This is the Patent Owner's response to the non-final office action issued March 2, 2012 in the reexamination of U.S. Patent number 6,366,130 issued to Podlesny et al. ("the Podlesny patent" or "Podlesny"). The Patent Owner respectfully requests entry of new claims 9-12 and argues that none of the original claims are anticipated. The examiner rejected claims 1-2 and 5-7 as being anticipated by the published European application EP 0597231 A2 belonging to United Memories, Inc. and Nippon Steel Semiconductor Corp. with inventor Kim C. Hardee published May. 18, 1994 ("the Hardee reference" or "Hardee"). Hardee cannot anticipate the Podlesny claims because, among other things, Hardee fails to teach at least one element of claim 1: pre-charging two separate buses, a differential bus and a differential data bus. There are a number of other independent reasons why the claims are not anticipated, as set forth below.

In support of this response, the Patent Owner submits herewith the Declaration of Dr. Philip Koopman (the "Koopman Declaration").

A. Current Litigation Involving the Patent Under Reexamination

The Podlesny patent number 6,366,130 is currently involved in the following litigation: Cascades Computer Innovation, LLC. v. Hynix Semiconductor Inc., Civil Case 1:11-cv-04356 - Northern District of Illinois, Hon. Joan H. Lefkow.

B. Real Parties of Interest

The real parties of interest are Elbrus International Limited, assignee of the Podlesny patent, and Cascades Computer Innovation, LLC, the exclusive licensee.

C. Patent Owner's Support for New Claims

Support for new claim 9 can be found in Figs. 1 and 2 and Col. 2 where in Fig. 1, the differential bus LT/LC, pre-charges to the voltage Vpr (Col. 2, lines 19-21), and the differential data bus in Fig. 2 pre-charges to Vdd (Col. 2, lines 55-56).

Support for new claim 10 can be found in Fig. 2, which clearly shows a cross-coupled output stage.

Support for new claim 11 can be found in Col. 2, lines 12-13 and Col. 2, lines 42-43.

Support for new claim 12 can be found in Fig. 1 (14, 15), the differential bus LT/LC and Fig. 2 (lines running from lT to N8 and from lC to N6), the differential data bus, and also in Col. 2, lines 12-22 (differential bus) and Col. 2, lines 51-59 (differential data bus). These are clearly separate circuits.

D. Summary of Patent Owner's Arguments

The Hardee reference fails to teach all of the elements of claim 1 of Podlesny and therefore cannot anticipate claim 1. Since claim 1 is not anticipated, none of the dependent claims can be anticipated.

There are multiple, independent reasons why claims 1-2 and 5-7 are not anticipated by Hardee:

1. Hardee fails to teach pre-charging **both** a differential bus and a differential data bus;

2. Hardee's bus drivers are only active on a write operation, and Hardy fails to teach pre-charging before a write operation;

3. Hardee fails to teach a differential bus and a differential data bus coupled to a pre-charge source;

4. Hardee fails to teach a latching sense amp coupled to a differential bus; and,

5. Hardee fails to teach an output stage coupled to an output of a first stage including a cross-coupled latch coupled to a differential data bus.

E. Doctrine of Anticipation

Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference or embodied in a single prior art device or practice. In re Paulson, 30 F.3d 1475, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of the rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986). To anticipate a patent claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. Atlas Powder Co. v. IRECO Inc., 190 F.3d 1342, 51 USPQ2d 1943 (Fed. Cir. 1999). The reference must describe the applicant's claimed invention sufficiently to have placed a person of ordinary skill in the field of the invention in possession of it. *See*, In re Spada at 708. The question of anticipation over a printed publication (including a published patent application) is whether the claims encompass and would enable the patentee to exclude others from making, using, or selling a product described in the publication. Titanium Metals Corp. v. Banner, 778 F.2d 1570, 227 USPQ 773 (Fed. Cir. 1985).

F. The Podlesny Patent

Claim 1 of the Podlesny patent reads:

> 1. A data transfer arrangement comprising:
> two bus drivers;
> a voltage precharge source;
> a differential bus coupled to the bus drivers and to the voltage precharge source; and
> a latching sense amplifier coupled to the differential bus;
> wherein the latching sense amplifier comprises:
> a first stage including a cross-coupled latch coupled to a differential data bus; and
> an output stage coupled to an output of said first stage;
> wherein the output of the first stage is coupled to an input of the output stage;
> wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr≈K*Vdd, and K is a precharging voltage factor.

The Podlesny patent describes two separate pre-charged buses, a differential bus and a differential data bus. The differential bus of one preferred embodiment can be seen as LT (14) and LC (15) in Fig. 1 (Koopman Declaration, Par. 18):

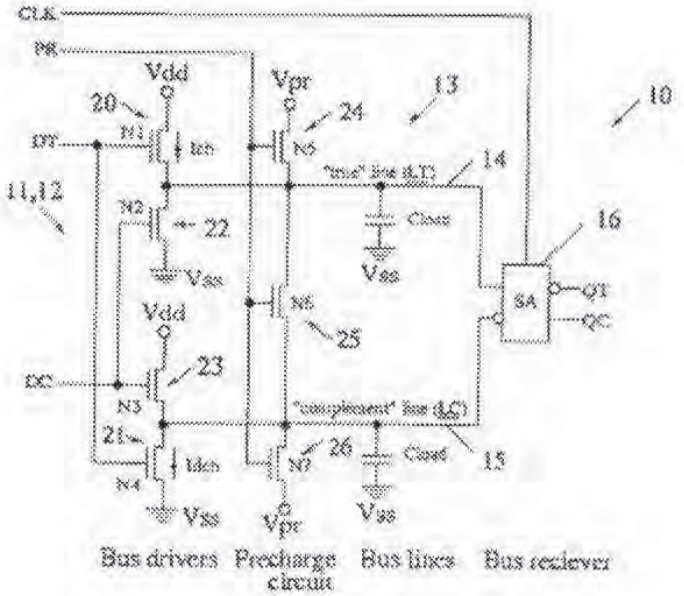


FIG.1.

In this embodiment, when the PR signal is high with DT and DC at zero, this bus is pre-charged to a particular voltage (Koopman Declaration, Par. 16).

Fig. 2 shows a preferred embodiment of the Podlesny sense amplifier stage. A second differential data bus can be seen in Fig. 2:

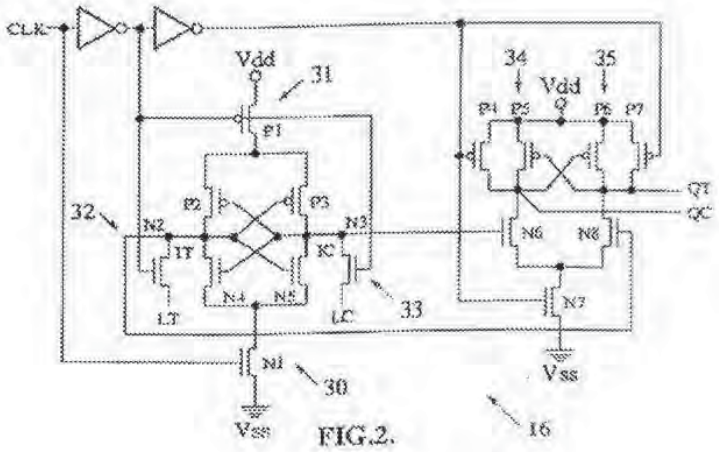


FIG.2.

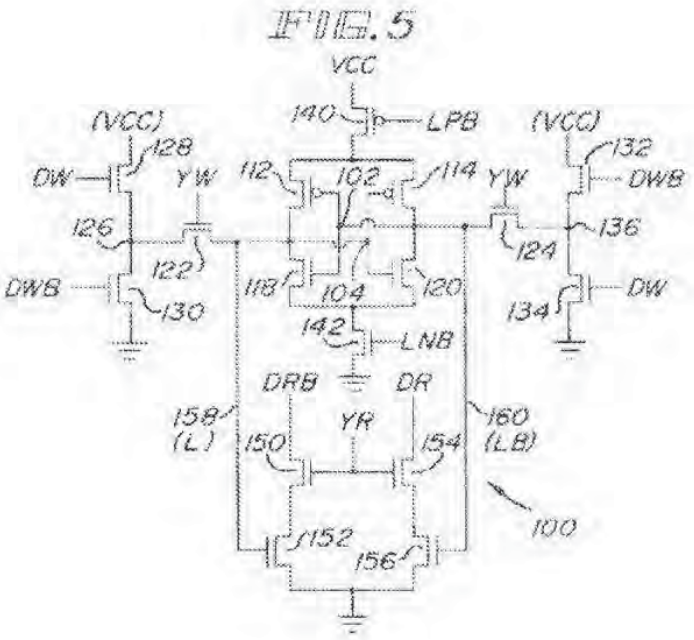
The second bus, or differential data bus, runs between the group of transistors on the left, including P2, N4, P3 and N5 which form a first stage to the group of transistors on the right, including P5, N6, P6 and N8, which form an output stage.

The output of the first stage is coupled to the input of the output stage by this differential data bus, with connections running from the junction between P3 and N5 to the gate of N6, and from the junction between P2 and N4 to the gate of N8. In a preferred embodiment, when the clock is low (CLK = 0), this second or differential data bus, pre-charges (Koopman Declaration, Par. 22). On the opposite clock phase (CLK = 1), data is transferred to the outputs QT and QC (Koopman Declaration, Par. 23).

The language of claim 1 clearly requires both a differential bus and a differential data bus to pre-charge. A preferred embodiment described in the specification includes two distinct differential data buses (one shown in Fig 1, and the other shown in Fig. 2), each of which is pre-charged on different clock phases and then operated to transfer a data value (See Col. 2, lines 12-13 and lines 42-45). Part of the circuit of this embodiment as shown in Fig. 2 also includes a latch and an output stage, each having forms of cross-coupled feedback (Koopman Declaration, Par. 24).

G. <u>The Hardee Reference</u>

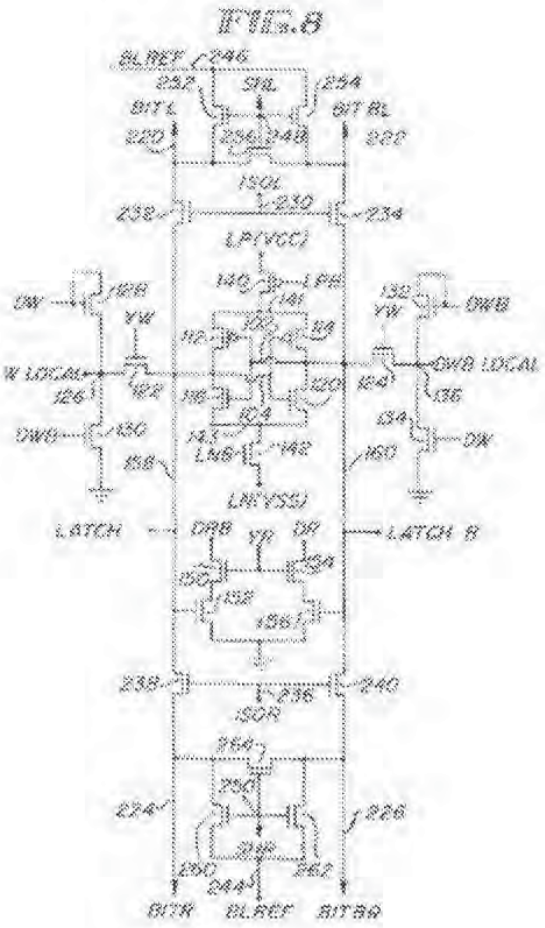
The Hardee reference describes a column sense amplifier for a large semiconductor memory array (Koopman Declaration, Par. 25). This circuit is used in both a read mode and a write mode in connection with two of the bit lines that run between memory cells on the particular column (See Hardee, Col. 1, lines 27-40), (the actual memory cells are not shown in Hardee). The Hardee circuit contains input drivers (write circuitry) (128, 130, 132, 134), a latch (112, 114, 118, 120), and a read amplifier (150, 152, 154, 156). This can be seen in Hardee Fig. 5:



There is an input data bus DW and its complement DWB (this bus carries write data ultimately destined for memory cells), which is not pre-charged, and an output data bus DR and its complement DRB (this bus carries read data out of the device), which is also not pre-charged. These buses lead in and out of the memory array and eventually to data pins on the chip. The only bus that is ever pre-charged in Hardee is the bus L and its complement LB (ref. numerals 158 and 160), which is the internal column bit bus, and this particular bus is only pre-charged on read operations (Koopman declaration, Par. 25). The pre-charging circuitry is not shown in Fig. 5, but is shown in Fig. 8

It should be noted that the additional read circuits shown in the original Fig. 8 (including transistors 150, 152, 154, 156) were omitted from the reproduction of Fig. 8 in the Reexamination Request. The fact that these were intentionally removed from the figures included in the Reexamination Request is tacit admission that the requestor deems such structures– and read operations overall –irrelevant to its Request. In particular,

during read operations, the signal YW is low, turning off transistors 122 and 124, thus decoupling the data write buffers from the bit lines (Koopman Declaration, Par. 26).



Further circuitry shown in Figure 8 includes a reference input BLREF applied to nodes 244 (bottom) and 246 (top of Fig. 8). Signals SHL at a node 248 and SHR at a node 250 are used in precharging the bit lines. At the top of Figure 8, it will be

(Hardee, Fig. 8 and Col. 12, lines 55-59).

Fig. 8, and the above-quoted text, show that the signals SLR and SHR couple and decouple the BLREF pre-charging level onto the bus BITR and BITBR during pre-

charging (BITR and BITBR in Fig. 8 are the same as L and LB in Fig. 5). However, as stated, this pre-charging only occurs during read operations (Koopman Declaration, Par. 32).

This is the only discussion, circuit or figure in the Hardee reference that explains in any way how pre-charging works, and it is clear from this that only one bus is being pre-charged, namely the BITR/BITBR bit bus, and it is only pre-charged during read operations (Koopman Declaration, Pars. 28, 31-32). However, during read operations, the input bus drivers are turned off, and hence, disconnected from the circuit.

The values of SHL and the pre-charge circuits are not mentioned by Hardee in the context of write operations. A person of ordinary skill in the art at the time of the Podlesny invention would have understood that pre-charging would not have been performed for write operations because it is typically unnecessary, as will be discussed in subsequent paragraphs. Furthermore, the values of ISOL and ISOR, which control the isolation transistors 232, 234, 238 and 240, as pointed out by the Requester, are not mentioned in the context of write operations (Koopman Declaration, Par. 28).

H. Argument: The Hardee Reference Cannot Anticipate the Podlesny Claims

The Hardee reference does no anticipate the Podlensky claims for the following reasons:

1. Hardee Fails To Teach Pre-Charging **Both** A Differential Bus and A Differential Data Bus.

The limitation of claim 1: "wherein the differential bus and the differential data bus are precharged to a voltage " is not taught by Hardee. As more fully shown above in

Section F, the Podlensky patent teaches two separate buses, while in the description of the Hardee reference in Section G we see that Hardee does not. In fact, the prosecuting examiner's reason for allowance (cited by the Requester) uses the plural "buses" when referring to pre-charging.

> applicants' arguments have been fully considered and deemed to be persuasive. The present invention teaches precharging the buses to a specific level between ground and Vdd, which results in equal, low differential Voltage swings, providing increased speed of data transfer. The prior art of Lee et al. does not teach such precharging buses as described above. Appendix B2 at page 24, Notice of Allowance mailed in Application No. 09/505,656 on February 22, 2001.

(Request for Reexamination, p. 10).

The Requester makes the additional statement:

> "Upon activating precharge circuit and the isolation transistors 232 and 234, the DW Local and DWB Local bit lines and the data lines 158 and 160 are precharged to a voltage BLREF, which is illustratively a constant voltage of 1/2 VCC. Hardee at 13:17-19" (Request, p. 12 just below the figure).

This is incorrect. Hardee does not state, teach or suggest anywhere that DW and DWB are pre-charged or connected to BLREF. Hardee Col. 13, lines 17-19, cited by the Requester to support this reads as follows:

seen that the signal SHL is applied to the gate electrodes of transistors 252, 254, and 256. Transistor 256 is generally an equilibrating transistor which shorts the two bit lines 220, 222 together whenever that transistor is turned on. Transistors 252 and 254 have their source-drain paths connected between the bit line reference BLREF at node 246 and the bit lines 220, 222 respectively and will therefore, when turned on, couple the bit line reference voltage to the bit lines themselves. Likewise, the configuration at the bottom of Figure 8 includes transistors 260, 262, and 264 which operate similarly in response to the SHR signal. Again, these transistors 252 through 264 are N channel transistors but other types of switching devices might be employed in any given embodiment. The bit line reference is illustratively a constant voltage approximately equal to ½VCC in one preferred embodiment.

This paragraph only describes connecting the L and LB or bit buses to BLREF and hence pre-charging them under control of the SHL and SHR signals; DW and DWB are not mentioned. DW and DWB represent an external bus that brings in write data to the sense amplifier for writing on the bit buses into memory cells (which are not shown in Hardee). Hardee does not pre-charge either the DW/DWB write bus or the DR/DRB read bus (Koopman Declaration, Par. 31).

For these reasons alone, Hardee cannot anticipate claim 1.

2. Hardee's bus drivers are only active on a write operation, and Hardy fails to teach pre-charging before a write operation.

On page 23 of the Reexamination Request, it is alleged that Hardee teaches that a differential bus and a differential data bus are pre-charged. The reasoning given quotes

Hardee: "[t]ransistors 252 and 254 have their source-drain paths connected between the bit line reference BLREF at node 246 and the bit lines 220, 222, respectively, and will therefore, when turned on, couple the bit line reference voltage to the bit lines themselves. (Hardee at 13:5-19)" However, what the Reexamination Request does not say is that this is in the context of read operations, and that this requires SHL to be on, which does not happen during write operations. Since the data write buffers are only connected to the bit lines via transistors 122 and 124 during write operations, this quoted statement is inapposite. In particular, during read operations the YW signal (which is a write signal) is off, which makes it impossible for this pre-charge voltage to reach nodes 126 and 136 (alleged to be the differential bus), because they are not coupled (Koopman Declaration, Par. 52).

On page 12 of the Reexamination Request, it is alleged that a write operation involves first enabling YW, turning on transistors 122, 124, then activating the pre-charge circuit. No reference from Hardee is given in the Reexamination Request for the combination of enabling YW and then enabling pre-charge (which would require enabling SHL), because no such reference exists. Hardee does not teach pre-charging while YW is enabled. Hardee only teaches pre-charging for a read operation, and the operation at issue in Podlensy is for a write operation. During writes, YW is disabled, decoupling nodes 126/136 from the bit lines (Koopman Declaration, Par. 31).

Accordingly, the differential bus in Hardee is not pre-charged at all as the Reexamination Request alleges. As to the differential data bus (158/160), it can only be pre-charged during read operations, but is not pre-charged during write operations.

Therefore, Hardee fails to teach required claim elements on two basis: first, it fails to teach that the pre-charging occurs during the write operation, hence no bus coupled to the bus drive transistors is ever pre-charged; and second, as more fully discussed above, Hardee fails to teach that both the differential bus and the differential data bus are pre-charged, (Koopman Declaration Par. 54).

For this reason alone, Hardee does not anticipate claim 1.

3. Hardee Fails To Teach A Differential Bus Coupled To A Pre-Charge Source.

On page 21 of the Reexamination Request, it is alleged that "a differential bus coupled to the bus drivers and to the voltage pre-charge source" is satisfied by node 126 being coupled to BLREF "when control signals YW, SHL, and ISOL are high." However, there is no time during a write operation when this is true (and only during the write operation are the bus drivers connected to anything), and Hardee contains no teaching that this would be a desirable mode of operation (Koopman Declaration, Par. 33). In fact, just the opposite is true. It is not necessary to pre-charge during a write operation for a structure like that of Hardee because the signals are normally strong enough. Pre-charge is typically intended to make it easier for a relatively weak voltage source resident in a memory bit to induce a slight voltage imbalance that can be read by a sense amplifier. That is the reason the sense amplifier is in the Hardee circuit. During writing there is normally a direct connection to a strong voltage source (via the Data Write blocks mentioned previously), so pre-charging is usually unnecessary, and typically such pre-charging would be avoided to minimize power consumption (Koopman Declaration, Par. 35).

Also, Hardee states that the first thing that happens during a write operation is that YW is turned on. If pre-charging were to be attempted at some point after this, it would lead to a short between BLREF and Ground via transistors 252, 232, 122, and 130, dissipating power and potentially damaging the chip. Analogous reasoning applies to the path through transistors 254, 234, 124, and 134 (Koopman Declaration, Par. 36). Therefore, it is impossible to pre-charge the Hardee circuit during a write operation.

This is further verified by noting that Hardee does not teach SHL being high during a write operation. The operation of SHL is only mentioned in the context of a read operation. The Reexamination Request tacitly admits that this is irrelevant by omitting read circuitry from Fig. 8, and by omitting any mention of read operations (Koopman Declaration, Par. 34).

For this reason alone, Hardee does not anticipate claim 1.

4. Hardee Fails To Teach A Latching Sense Amplifier Coupled To A Differential Bus.

On page 21 of the Reexamination Request, it is alleged that "a latching sense amplifier coupled to the differential bus" is satisfied by the Latch & Sense Amp shown in the figure. However, during the write cycle (which is the only cycle that the bus drivers are connected to anything), Hardee does not teach this circuit operating as a latching sense amp (Koopman Declaration, Par. 39).

While operation of the sense amplifier is described for a read operation, Hardee does not specify the values of LPB and LNB during a write operation. Thus, a person of ordinary skill in the art could not know and would be forced to speculate as to how the

latch operates during a write operation. It is only clear from Hardee's description that these signals are manipulated during read operations (Hardee 13:24-35) and are not statically set values, but there is no mention as to their values during write operations (Koopman Declaration, Par. 41). Speculation on how a particular circuit might work is insufficient for anticipation. "[A]bsence from the reference of any claimed element negates anticipation." Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

In addition, during a write operation, the "sense amp" circuit taught by Hardee is being operated as a latch, not as a "latching sense amp" as required by the claims. As a result, a person of ordinary skill in the art must assume that during a write operation there is no latching sense amplifier coupled to the differential bus, but rather the circuit is configured to provide just a latch with no sense amplifier functionality (Koopman Declaration, Par. 45). Therefore, the claim limitation, "a latching sense amplifier coupled to the differential bus", is not taught by Hardee.

For this reason alone, Hardee does not anticipate claim 1.

5. Hardee Fails To Teach An Output Stage Coupled To An Output Of A First Stage Including A Cross-Coupled Latch Coupled To A Differential Data Bus.

On page 23 of the Reexamination Request, it is alleged that the Hardee sense amplifier contains an "output stage coupled to an output of said first stage" as recited in Claim 1 of Podlesny. The Reexamination Request states, as to Hardee: "Specifically, the output stage includes two isolation transistors 232 and 234 controlled by the ISOL signal.

The differential voltage pair 158 and 160, at the output of the first stage, serve as the input of this output stage. Hardee at 14:19-23."

The operations described in Hardee 14:19-23 are in the context of a read cycle that may be refreshing the bit value after it has been read. But during the read cycle, the bus drivers are isolated from the bit lines due to the YW signal being low and turning off transistors 122 and 124. Hardee therefore does not apply to a write cycle, and therefore does not teach this element (Koopman Declaration, Par. 47).

As importantly, the transistors involved in Hardee (232 and 234) are "isolation transistors" as stated by the Reexamination Request itself, and not cross-coupled as would be required to make them the output stage of a latch (Koopman Declaration, Par. 48). The Hardee isolation transistors do not have any cross-coupled feedback, so they cannot retain a fixed value despite changing inputs. For that matter, they do not have a connection to power and ground, a clock input, or any other ability to retain values. Rather, they are just a pair of pass transistors. A person of ordinary skill in the art would recognize that the Hardee isolation transistors are not an output stage. They are simply a pair of isolation transistors, as admitted by the Reexamination Request. They serve to isolate sections of the bus from other sections. (Koopman Declaration, Par. 49).

Podlesny Col. 3 points out some of the advantages of using a second latch stage rather than simple isolation transistors, such as avoiding leakage currents and output glitches (Col 3:4-11). An output stage must be more than a mere pair of isolation transistors. Hardee fails to teach the required claim element of an "output stage coupled to an output of said first stage." (Koopman Declaration, Pars. 50-51).

For this reason alone, Hardee does not anticipate claim 1.

I. Dependent Claims 2, 5 and 7

Claim 2 adds the limitation to claim 1 of "wherein the bus drivers comprise active pull-up and active pull-down bus drivers". This additional limitation does not change the arguments above. Since the parent claim 1 is not anticipated by Hardee, it is impossible for claim 2 to be anticipated.

Claim 5 adds the limitation of the "wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage". This additional limitation also does not change the arguments above. Since the parent claim 1 is not anticipated by Hardee, it is impossible for claim 5 to be anticipated.

Claim 7 adds the limitation to claim 2, "wherein the active pull-up and active pull-down drivers are N-MOS transistors". This additional limitation also does not change the arguments above. Since the parent claim 1 and the intervening claim 2 are not anticipated by Hardee, it is impossible for claim 7 to be anticipated.

J. Conclusion

For the reasons stated above, Hardee does not anticipate claim 1 of Podlesny, and because the parent claim is not anticipated, neither are dependent claims 2, 5 and 7.

For these reasons, the examiner is therefore respectfully requested to remove the rejection of claims 1, 2, 5 and 7, to accept new claims 9-12, and to close the reexamination.

Respectfully Submitted

/clifford kraft/

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ACTION CLOSING PROSECUTION (37 CFR 1.949)	Control No. 95/000,657	Patent Under Reexamination 6366130
	Examiner Deandra M. Hughes	Art Unit 3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:
Patent Owner on 01 May, 2012
Third Party(ies) on 06 July, 2012

Patent owner may once file a submission under 37 CFR 1.951(a) within 1 month(s) from the mailing date of this Office action. Where a submission is filed, third party requester may file responsive comments under 37 CFR 1.951(b) within 30-days (not extendable- 35 U.S.C. § 314(b)(2)) from the date of service of the initial submission on the requester. **Appeal cannot be taken from this action.** Appeal can only be taken from a Right of Appeal Notice under 37 CFR 1.953.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892
2. ☐ Information Disclosure Citation, PTO/SB/08
3. ☐ _____

PART II. SUMMARY OF ACTION:

1a. ☒ Claims 1,2,5-7 and 9-12 are subject to reexamination.
1b. ☒ Claims 3,4 and 8 are not subject to reexamination.
2. ☐ Claims _____ have been canceled.
3. ☒ Claims 1,2 and 5-7 are confirmed. [Unamended patent claims]
4. ☒ Claims 12 are patentable. [Amended or new claims]
5. ☒ Claims 9-11 are rejected.
6. ☐ Claims _____ are objected to.
7. ☐ The drawings filed on _____ ☐ are acceptable ☐ are not acceptable.
8 ☐ The drawing correction request filed on _____ is: ☐ approved. ☐ disapproved.
9 ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has: ☐ been received. ☐ not been received. ☐ been filed in Application/Control No _____
10. ☐ Other _____

INTER PARTES REEXAMINATION ACTION CLOSING PROSECUTION

1. This is an action closing prosecution in the *inter partes* reexamination of USP 6,366,130. ("**'130 patent**")

- **Claims 1-2 and 5-7** were ordered for reexamination.
- **Claims 3-4 and 8** were not ordered for reexamination.
- New **claims 9-12** of the claim amendment filed May 1, 2012 have been entered.
- Patent Owner's ("PO") remarks filed May 1, 2012 have been entered.
- Third Party Requester's ("3PR") comments filed July 6, 2012 have been entered.

2. Accordingly, **claims 1-2, 5-7, and 9-12** are under reexamination.

References

3. The following references are applied in this action:

- EP 0 597 231 to Hardee published May 18, 1994. ("**Hardee**")
- Declaration of David L. Taylor executed Jul. 6, 2012. ("**Taylor Declaration**")
- Declaration of Dr. Philip Koopman executed Apr. 29, 2012. ("**Koopman Declaration**")

Summary of this Action

4. The following is a summary of this action:

- **Claims 1-2 and 5-7** are confirmed as patentable.
- **Claim 12** is allowed as patentable.
- **Claims 9-11** are rejected under 35 USC 112-1st ¶.

Response to PO's Remarks and 3PR's Comments

5. PO's remarks, 3PR's comments, the **Taylor Declaration**, and the **Koopman Declaration** have been considered and weighed and 3PR's argument is found not persuasive for the reasons below. As such, the rejection of **claims 1-2 and 5-7** as being anticipated by **Hardee** is withdrawn.

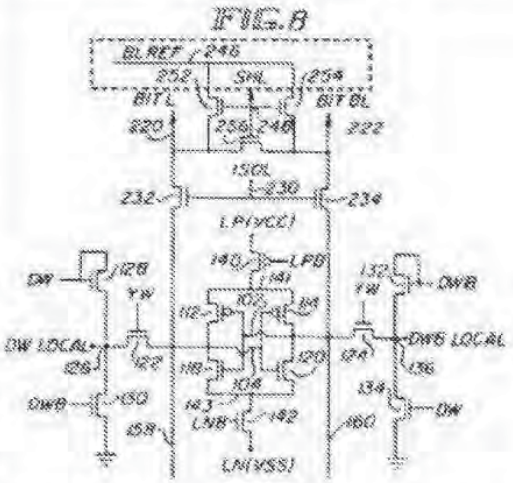
6. **Claims 1-2, 5-7, and 9-12** require, *inter alia*, (1) a voltage precharge source, (2) differential bus, and (3) a differential data bus.

The Examiner's outline of **claim 1**, which is the only independent claim under reexamination, is reproduced below.

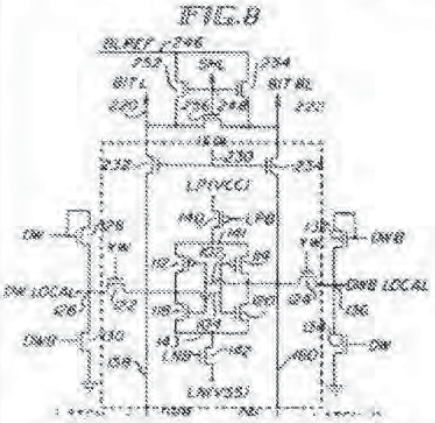
A data transfer arrangement comprising:

- two bus drivers;
- a voltage precharge source;
- a differential bus coupled to the bus drivers and to the voltage precharge source;
- a latching sense amplifier coupled to the differential bus;
- wherein the latching sense amplifier comprises:
    - a first stage including a cross-coupled latch coupled to a differential data bus; and
    - an output stage coupled to an output of said first stage;
    - wherein the output of the first stage is coupled to an input of the output stage;
    - wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.

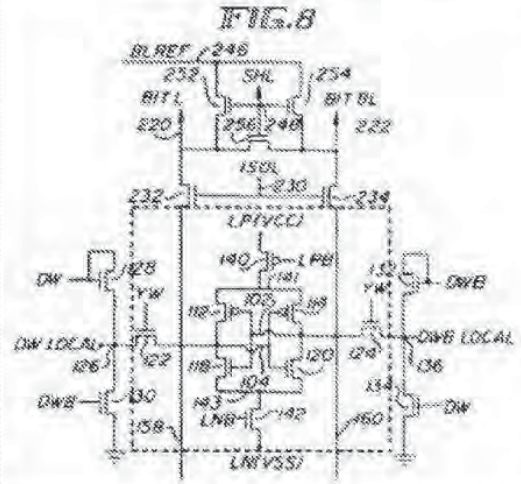
As to the claimed '*voltage precharge source*', 3PR argues the *BLREF #246* (*figure 8*) of **Hardee** reads on this limitation. (*Request, pg. 20*)

a voltage precharge source;	FIG. 8 of Hardee shows voltage precharge source, indicated by the dashed box below:  Hardee discloses the BLREF reference, which is configured to provide a precharge source for data line pairs 158/160 and 126/136, where the BLREF value is illustratively a constant voltage of ½ VCC. Hardee at 13:17-19.

As to the claimed '*differential bus*', 3PR argues *DW LOCAL #126* or *DWB LOCAL #136* of **Hardee** reads on this limitation. (*Request, pg. 21*)

and a latching sense amplifier coupled to the differential bus;	Hardee discloses a latching sense amplifier, as replicated in the annotated [illegible] indicating the version of FIG. 8 reproduced below, coupled to the differential bus pair 126 and 136: 

As to the claimed '*differential data bus*', 3PR argues *Data Line #158* of **Hardee** reads on this limitation. (*Request, pg. 22*)

wherein the latching sense amplifier comprises: a first stage including a cross-coupled latch coupled to a differential data bus;	Hardee discloses a cross-latched circuit as the first stage of the latching sense amplifier, as indicated by the dashed box, analogous to element 4[illegible] as produced below. The first stage is coupled to differential data bus 158, where the complement differential data bus is 160.  To write the memory cell on the column, DW or DWB is enabled while YW remains high, and a pair of translator gates 128/134 or 130/132 turn on. The DW Local and the DWB Local bit lines experience a change in voltage, one bit line going high while the other bit line goes low. The differential voltage enables the cross-latched sense amplifier and drives one of the data lines 158 or 160 to VCC and the other line to ground. Hardee at 13:43-53.

It is found that the only disclosure of **Hardee** pertaining to 'precharging' refers to precharging the bit lines, *BIT L* and *BIT BL*. (*col.12:55-58; col.13:5-18*)

> Further circuitry shown in Figure 8 includes a reference input BLREF applied to nodes 244 (bottom) and 246 (top of Fig. 8). Signals SHL at a node 248 and SHR at a node 250 are used in precharging the bit lines. At the top of Figure 8, it will be

As such, it is found that **Hardee** does not disclose "*the differential bus (#126) and the differential data bus (#158) are precharge to a voltage V_{pr} between V_{dd} and ground, where $V_{pr}=K*V_{dd}$, and K is a precharging voltage factor*" in combination with the other limitations of the claims because it is found that **Hardee**'s *BLREF* (i.e., 'the voltage

precharge source') is disclosed as precharging bit lines *#220* and *#226*. (*col.13:5-18*) Thus, for the reason that **Hardee**'s *BLREF* (i.e. *'the voltage precharge source'*) is not disclosed as precharging *DW LOCAL #126* or *DWB LOCAL #136* (i.e., '*the differential bus*') or *Data Line #158* (i.e. '*the differential data bus*'), the anticipation rejection of independent **claim 1** and its dependent claims is withdrawn.

Claim Rejections - 35 USC § 112

7. The following is a quotation of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.
>
> The following is a quotation of 35 U.S.C. 112 (pre-AIA), first paragraph:
> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. **Claims 9-11** are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to **claim 9**, PO states that this claim is described by *figures 1-2* and *column 2* where in *figure 1*, the differential bus LT/LC, precharges to the voltage V_{pr} (*col.2:19-21*) and the differential data bus in *figure 2* precharges to V_{dd} (*col.2:55-56*). (*Comments, pg. 4*)

First, it is found that *figure 1* describes V_{pr} but does not describe 'precharging'. Second, it is found that *figure 2* describes V_{dd} but does not describe precharging. Third, it is found that *col.2:19-21* discusses precharging V_{pr} but does not describe that the '*differential bus*' is precharged to a different voltage than the '*differential data bus*' because the value of V_{pr} with respect to the voltage at which the '*differential data bus*' is not disclosed. Fourth, it is found that *col.2:55-56* discusses precharging V_{dd} but does not describe the '*differential bus*' is precharged to a different voltage than the '*differential data bus*' because the value of V_{pr} with respect to V_{dd} is not disclosed.

As to **claim 10**, PO states *figure 2* clearly shows a cross-coupled output stage. (*Comments, pg. 4*) Although it is agreed that *figure 2* clearly shows a cross-coupled output stage, it is not agreed that *figure 2* describes "*the output stage includes a cross-coupled feedback*", as claimed, because *figure 2* does not describe the 'feedback' limitation.

As to **claim 11**, PO states *col.2:12-13* and *col.2:42-43* describes this claim. First, it is found that *col.2:12-13* describes the following:

> Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

Second, it is found that *col.2:42-43* describes the following:

> The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

As such, *col.2:12-13 or 42-43* does not describe "*wherein the differential bus is precharged to a different clock phase than the differential data bus*" because they do not

describe: (1) clock phases, (2) the clock phase of the differential bus, or (3) the clock phase of the differential data bus.

Therefore, **claims 9-11** have not been described in the specification in such a way as to reasonably convey that the inventor(s), at the time the application was filed, had possession of the invention of **claims 9-11**.

Reasons for Confirmation/Allowance

9. As to **claims 1-2 and 5-7** are confirmed as patentable because, as set forth above, PO has successfully traversed the anticipation rejection over **Hardee**. Further, it is agreed that *figures 1 and 2* describe the 'differential bus' and 'differential data bus' as different circuits. Thus, it is found that **claim 12** is described by the **'130 patent** specification and is allowed as patentable because it depends upon **claim 1**, which has been confirmed as patentable.

Conclusion

10. All correspondence relating to this *inter partes* reexamination proceeding should be directed:

By Mail to: Mail Stop *Inter Partes* Reexam
Attn: Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at:

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EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

/Deandra M. Hughes/
Primary Examiner, AU 3992

Conferees:

/Christina Y. Leung/
Primary Examiner, Art Unit 3992

/Daniel J Ryman/
Supervisory Patent Examiner, Art Unit 3992

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of Podlesny et al.	)	
	)	
INTER PARTES REEXAMINATION	)	Art Unit: 3992
of	)	
U.S. Patent No. 6,366,130	)	Examiner: HUGHES, Deandra M.
	)	
Control No. **95/000,657**	)	
	)	
Reexamination date: Jan. 19, 2012	)	
	)	
Patent Issue Date: April 2, 2002	)	Atty. Dkt. No. Cascade-130
	)	
For: HIGH SPEED LOW POWER DATA	)	
TRANSFER SCHEME	)	
	)	

BRIEF ON CROSS-APPEAL BY PATENT OWNER

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This is a cross-appeal from the Right of Appeal Notice issued on April 5, 2013 The Requester filed a notice of appeal on April 12, 2013. The Patent Owner filed a notice of cross-appeal on April 24, 2013.

I. Real Party of Interest

The real party of interest is the Assignee: Elbrus International, Limited, and the Exclusive Licensee: Cascades Computer Innovation, LLC.

II. Related Appeals and Interferences

There are no other related appeals or interferences.

III. Status of the Claims

Claims 1, 2, 5-7 and 9-12 are subject to reexamination. Claims 3, 4 and 8 are not subject to reexamination. Claims 1, 2 and 5-7 stand confirmed. New claim 12 stands patentable. New claims 9-11 stand rejected.

Claims 9-11 are being appealed in this Cross-Appeal.

Claims 9-11 do not stand or fall together.

IV. Status of Amendments

There have been no amendments since the April 5, 2013 Right to Appeal Notice.

V. Summary of Claimed Subject Matter

A. General Description

The Podlesny patent number 6,366,130 that is the subject of this reexamination relates to a data transfer arrangement such as might be used in a semiconductor memory device. The arrangement includes two separate pre-charged buses, a differential bus and a differential data bus. These two buses may be precharged to either the same or to different voltages. These buses operate on alternate clock phases: one bus is being precharged while the other is transferring data and vice versa. This invention leads to increased transfer speed and results in circuits that are not sensitive to circuit parameter mismatches, noise and deviations in various applied voltages. See Abstract and Col. 1, lines 10-22.

B. Mapping of the Independent Claim to the Specification

There are no independent claims involved in this cross-appeal; however, dependent claims 9-11 which are being appealed depend on independent claim 1.

Therefore, even though claim 1 is not a subject of this cross-appeal, a mapping of its limitations to the specification will be given.

Claim 1: A data transfer arrangement [**Abst., line 1**] comprising:

two bus drivers [**Col. 2, lines 9-11**];

a voltage precharge source [**Fig. 1, terminal marked Vpr, and Abst., line 3**];

a differential bus coupled to the bus drivers and to the voltage precharge source [**Fig. 1, (14) and (15)**];

a latching sense amplifier coupled to the differential bus [**Fig. 1, (16), Col. 2, lines 39-40**];

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch [**Fig. 2, P2,N4, P3, N5**] coupled to a differential data bus [**Fig. 2, line from N3 to N6 and line from N2 to N8, Col. 2, lines 39-40, Col. 2, line 46 to Col. 3, line3**];

an output stage [**Fig. 2, P5, N6, P6, N8**] coupled to an output of said first stage wherein the output of the first stage is coupled to an input of the output stage [**Fig. 2, line from N3 to N6 and line from N2 to N8**];

wherein the differential bus and the differential data bus are precharged to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor [**Col. 3, lines 24-30**].

VI. <u>Issues to be Reviewed on Appeal</u>

1) Claims 9-11 stand rejected under 35 U.S.C. §112(a) or 35 U.S.C. §112, first paragraph (Pre-AIA) as failing to comply with the written description requirement.

VII. Argument

Claims 9-11 have sufficient support in the specification to satisfy 35 U.S.C. §112(a).

In the case of a newly added claim, in order to reject on the written description requirement, the examiner has the burden to present reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the new claim. See M.P.E.P. 2163.04(I)(B). This is particularly true when the claim presents a limitation that does not exactly mimic language in the specification. The test is: Does the description clearly allow persons of ordinary skill in the art to recognize that the inventor has invented what is claimed? In re Gosteli, 872 F.2d 1008, 1012 (Fed. Cir. 1989) as cited in M.P.E.P. 2163.02.

The dependent claims on appeal introduce three new limitations into those of claim 1, namely "different voltage" (claim 9), "cross-coupled feedback" (claim 10), and "precharged on a different clock phase" (claim 11). The examiner contends that these are not adequately supported by the written description.

The Patent Owner will show that the term "different voltage" in claim 9 is supported by relational statements (formulas) in the specification that are very clear to a person of ordinary skill; "cross-coupled feedback" would be understood by a person of ordinary skill simply by examining the topology of Figure 2; and"precharged on a different clock phase" is very clear from examination of Figures 1 and 2 as well as the written description.

The examiner fails to make out a *prima facie* case.

A. Claim 9 Has Sufficient Support under 35 U.S.C. §112(a).

Claim 9: The data transfer arrangement of claim 1 wherein the differential bus is precharged to a different voltage than the differential data bus.

Col. 2, lines 19-21 describe precharging of the differential bus (1st bus). "*...the complement phase driver on transistors **22** and **23** are in high impedance state and both bus lines are equalized and precharged to a potential Vpr (buses precharging level) through the turned on transistors **24**, **25** and **26**."*

This establishes that the differential bus is precharged to the voltage level Vpr.

Col. 2, lines 25-28 state: "*One of the drivers is pulled up and charges the appropriate bus line from the precharged level Vpr toward a more positive Vdd-Vt (where Vt is the threshold voltage of the pull up NMOS transistor of the driver).*"

This establishes that voltage value Vdd-Vt can be higher (more positive) than Vpr. It is well-known to a person of ordinary skill in the art that the threshold voltage of an NMOS transistor (here called Vt) is a very small positive voltage that may be very close to, or even equal to, zero. Hence, a person of ordinary skill in the art knows from reading this that Vdd can be, but does not have to be, more positive than Vpr because Vdd-Vt is greater than Vpr by the statement on line 27 *supra* "*a more positive Vdd-Vt*". In other words, the specification teaches that Vpr can be different than Vdd.

This is also supported by Col. 3, line 24 where it states: "(Vpr = K*Vdd, where K=1/3 for the ideal MOS model)..". This means that typically, Vpr is 1/3 of Vdd. However, in Col. 2, lines 55-56, it states: "The output nodes of both dynamic gates are precharged to Vdd ..". This describes precharging of the differential data bus (2nd bus).

Since the differential bus (1st bus) is charged to Vpr, and the differential data bus (2nd bus) is charged to Vdd, and Vpr does NOT have to equal Vdd, a person of ordinary skill in the art would know that the differential bus can be charged to a different voltage than the differential data bus, and claim 9 is sufficiently supported.

The examiner admits that Col. 2:19-21 discusses precharging one bus to Vpr and that Col.2:55-56 discusses precharging the other bus to Vdd. The examiner appears to be looking for an explicit statement that the differential bus is precharged to a different voltage that the differential data bus. However, the law does not require an explicit statement to satisfy the written description requirement under 35 U.S.C. §112(a). The written description mathematically recites that Vpr and Vdd can be different voltages.

The declaration of Philip Koopman, dated April 29, 2012. (the "Koopman Declaration"), at pars. 22-23, clearly points out the locations of these two buses in Figures 1-2.

For these reasons, claim 9 should be allowed.

B. Claim 10 Has Sufficient Support under 35 U.S.C. §112(a).

Claim 10: The data transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback.

Here the examiner admits that that Figure 2 shows a cross-coupled output stage. The examiner however, states that Figure 2 does not show cross-coupled feedback.

It is well-known in the art of electrical engineering that feedback is the description of a loop in the topography of a circuit where, in addition to its input being connected to its output, its output is also connected to its input via a different path.

Upon examination of the right-hand part of Figure 2 (the output stage) consisting of transistors P4, P5, P6, P7, N6, N7 and N8, it can be clearly seen that there are two outputs, QT and QC.

Tracing the output QT, it can be seen that it is the output of the transistor P6. The input to that transistor is the gate of P6 (this can be seen on the left side of P6 where there is a small circle). Thus the output QT is electrically connected to the input which is the gate of P6. This is the normal (or forward) path. However, the output QT is directly connected to the gate of P5 (this can be seen on the right side of P5 where there is another small circle). But, the output of P5 (which is QC) is directly tied to the input of P6 (namely its gate as just discussed). This is the feedback path (or reverse path). Topologically, this forms a loop in the graph. The output of P6 is tied to the input of P5, and the output of P5 is tied to the input of P6. This is cross-coupled feedback. (See Koopman Declaration par. 20).

Therefore, Figure 2 alone provides sufficient support for the limitation of claim 10 that the output stage includes cross-coupled feedback. This is clearly shown in the figure below as a marked loop.

For the

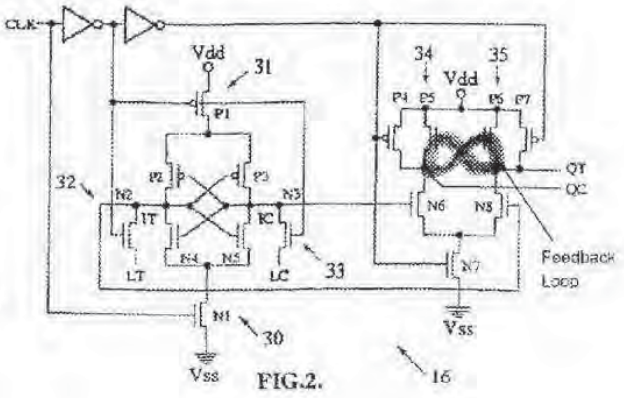

FIG.2.

For these reasons claim 10 should be allowed.

C. Claim 11 Has Sufficient Support under 35 U.S.C. §112(a).

Claim 11: The data transfer arrangement of claim 1 wherein the differential bus is precharged on a different clock phase than the differential data bus.

The examiner admits that Col. 2, lines 12-13 state: "Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase."

A person of ordinary skill in the art knows 1) digital circuits are operated by clocks and control lines; 2) all clocks have at least two phases; 3) when a circuit is clocked, it becomes active on one of the two clock phases.

The circuits shown in Figures 1-2 are driven by clocks and control lines, namely the signal marked CLK is a clock, and the signal marked PR is a control line. The output circuit shown in Figure 2 has two parts, the first part on the left of Figure 2, and the second part on the right of Figure 2. It can be seen from the two inverters in the clock line CLK (the two triangular devices at the top of Figure 2) that the left half operates on the opposite clock phase as the right half. (See Koopman Declaration par. 17).

The differential data bus is precharged by the turning on of transistors N2 and N3. This happens when the signal CLK is in a low state. This is supported by Col. 2, lines 45-56: "When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode." This refers to the left and right halves of Figure 2. (id.)

As shown in Figure 1, the differential bus is precharged by the turning on of the transistors N5, N6 and N7 when the control line PR is in the high state. (See Koopman Declaration par. 16).

Thus, the only question is what is relationship between the CLK signal and the PR signal? This is supplied by Col. 2, line 23: "During the data transfer phase, the control input PR is low."

Thus, from Col. 2: 45-46 we know that the data transfer mode occurs when the clock signal CLK is low, and from Col. 2: 23 that PR is also low during this phase. In other words, persons of skill in the art would understand from this disclosure that in this preferred embodiment the CLK and PR signals are in phase with one another. That means PR is high (precharging the differential bus) when the clock signal CLK is high.

Since the differential bus charges when the clock CLK is in the high phase, and the differential data bus charges when the clock CLK is in the low phase, there is sufficient support for the claim limitation: "wherein the differential bus is precharged on a different clock phase than the differential data bus". (See Koopman Declaration pars 16-18).

For these reasons, claim 11 should be allowed.

VIII. Conclusion

The Appellant respectfully submits that claims 9-11 have sufficient support in the specification to satisfy 35 U.S.C. §112(a). The applicant respectfully requests the Board to reverse the examiner's rejections and allow these claims.

Respectfully submitted

/clifford kraft/

Clifford H. Kraft
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Attorney of Record

APPENDIX I. Claims on appeal

Claim 9: The data transfer arrangement of claim 1 wherein the differential bus is precharged to a different voltage than the differential data bus.

Claim 10: The data transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback.

Claim 11: The data transfer arrangement of claim 1 wherein the differential bus is precharged on a different clock phase than the differential data bus.

For convenience, parent claim 1 is also listed even though it is not part of this cross-appeal:

Claim 1: A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source;

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus;

an output stage coupled to an output of said first stage wherein the output of the first stage is coupled to an input of the output stage,

wherein the differential bus and the differential data bus are precharged to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.

APPENDIX II. Evidence Appendix

Declaration of Dr. Philip Koopman, April 29, 2012.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,657	01/19/2012	6366130	19968-0006RX1	8472

74642 7590 03/27/2014

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NAPERVILLE, IL 60540

EXAMINER	
HUGHES, DEANDRA M	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
03/27/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX SEMICONDUCTOR INC.
Requester

v.

ELBRUS INTERNATIONAL, LIMITED and exclusive licensee:
CASCADES COMPUTER INNOVATION, LLC.
Patent Owner

Appeal 2014-000434
Reexamination Control No. 95/000,657
Patent 6,366,130 B1
Technology Center 3900

Before RICHARD M. LEBOVITZ, DAVID M. KOHUT, and ANDREW J. DILLON, *Administrative Patent Judges*.

KOHUT, *Administrative Patent Judge*

DECISION ON APPEAL

Requester filed a withdrawal of appeal on January 7, 2014 after the parties reached a settlement. The oral hearing scheduled for May 5, 2014 was waived by Patent Owner on January 24, 2014 and Patent Owner requested that the cross-appeal be decided on the briefs. Thus, this is a decision on the cross-appeal by the Patent Owner of the Examiner's decision to reject claims 9-11. Even though Third Party Requester, SK Hynix Semiconductor Inc., withdrew their appeal, we will address the Examiner's decision not to reject claim 12 under 35 U.S.C. § 112(a). The Board's jurisdiction for this appeal is under 35 U.S.C. §§ 6(b), 134, and 315. We affirm-in-part.

STATEMENT OF THE CASE

This proceeding arose from a request by SK Hynix Semiconductor Inc. for an *inter partes* reexamination of U.S. Patent 6,366,130 B1, titled "High Speed Low Power Data Transfer Scheme," and issued to Podlesny et al. on April 2, 2002 (the "'130 patent").

The '130 patent describes a data transfer arrangement circuit that uses low power and operates at a high speed.

Claims 9-12 on appeal were added during reexamination and are dependent upon claim 1 which reads as follows:

> 1. A data transfer arrangement comprising:
> two bus drivers;
> a voltage precharge source;
> a differential bus coupled to the bus drivers and to the voltgage precharge source;
> a latching sense amplifier coupled to the differential bus;
> wherein the latching sense amplifier comprises:

> a first stage including a cross-coupled latch coupled to a differential data bus;
>
> an output stage coupled to an output of said first stage;
>
> wherein the output of the first stage is coupled to an input of the output stage;
>
> wherein the differential bus and the differential data bus are precharge[d] to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.

Patent Owner appeals the Examiner's adoption of the following rejection of claims 9-11 under 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA), as failing to comply with the written description requirement.

Third Party Requester appealed the Examiner's determination (1) not to adopt Requester's proposed rejection of claims 1,2, and 5-7 as anticipated by European Patent Publication No 0 597 231; and (2) not to adopt Requester's proposed rejection of claim 12 as failing to comply with the written description and enablement requirement of 35 U.S.C. § 112, first and second paragraphs. Since Requester withdrew the Appeal, we shall not consider Ground 1). However, we shall address proposed rejection 2).

ISSUES

Did the Examiner err in finding that newly added claims 9-11 fail to comply with the written description requirement set forth by 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA)?

Did the Examiner err in failing to adopt Requester's proposed rejection claim 12 under 35 U.S.C. § 112?

ANALYSIS

During reexamination, Patent Owner added claims 9-12 and alleged support for these claims could be found in Figures 1 and 2 and various parts of the Specification.[1] The Examiner, in both the Action Closing Prosecution (ACP), mailed Jan. 23, 2013, and the Right of Appeal Notice (RAN), mailed April 5, 2013, disagreed and rejected claims 9-11 under 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (ACP 6-8; RAN 3-4), while finding claim 12 to be patentable (ACP 8; RAN 5).

Title 35 U.S.C. § 112 requires a patentee to provide a written description that allows a person of skill in the art to recognize that the patentee invented what is claimed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). To that end, to satisfy the written description requirement, the inventor "must . . . convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention." *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991).

Claim 9 recites "[t]he data transfer arrangement of claim 1 wherein the differential bus is precharged to a different voltage than the differential data bus." Patent Owner contends that Figure 1 and column 2, lines 19-21 of the '130 Patent, show that the differential bus (LT/LC) is precharged to a voltage Vpr while Figure 2 and column 2, lines 55-56, of the '130 Patent, show that the differential data bus is precharged to a voltage Vdd, where

[1] Response to Non-Final Office Action and Amendment, filed May 1, 2012, 2 (hereinafter Resp. Non-Final).

Vdd is different than Vpr. Resp. Non-Final 4. While the Examiner agrees that the differential bus is precharged to the voltage Vpr, the Examiner disagrees that the Figures and the Specification show that the differential data bus is precharged to a different voltage than the differential data bus because "the value of Vpr with respect to Vdd is not disclosed." RAN 3.

In response to the Examiner, Patent Owner argues that it is clear from the Specification that Vpr can be different than Vdd because column 2, lines 25-28, states that Vdd-Vt can be more positive than Vpr. PO App. Br. 5. Additionally, Patent Owner cites to column 3, line 24, which indicates the following formula: "Vpr=K*Vdd, where K=1/3 for the ideal MOS model." PO App. Br. 5. Thus, Patent Owner contends that Vpr is less than, and different, than Vdd. PO App. Br. 5.

On page 3 of the Patent Owner's Appeal Brief, Patent Owner indicates that the differential data bus is described as being segments N3 to N6 and N2 to N8 shown in Figure 2 of the '130 Patent. *See also* 3PR Resp. Br. 3. As a result, Requester argues that Patent Owner misinterpreted the '130 Patent as indicating that the differential data bus is precharged to Vdd. 3PR Resp. Br. 3. First, Requester argues that in the precharge phase, transistor P1 is not activated and the segments indicated above are, therefore, not coupled to Vdd. 3PR Resp. Br. 3. Second, Requester argues that the section of the '130 Patent cited to by Patent Owner for support regarding precharging the differential data bus (col. 2, ll. 55-56), while discussing precharging to Vdd, applies to output nodes QT and QC and not to the differential data bus. 3PR Resp. Br. 3-4. Lastly, Requester points to both

parties' experts who each indicate that QT and QC are precharged to Vdd, not the differential data bus. 3PR Resp. Br. 4.

We agree with Requester and the Examiner that the '130 Patent does not provide adequate written description for newly added claim 9. While one of ordinary skill in the art might use the disclosure to figure out a way to precharge the indicated differential data bus to a voltage that is different than the differential bus, a description which renders obvious a claimed invention is not sufficient to satisfy the written description requirement of that invention. *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (1997). Thus, the rejection of claim 9 as lacking written descriptive support in the '130 Patent is affirmed.

Claim 10 recites "[t]he data transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback." Patent Owner contends that Figure 2 of the '130 Patent provides a written description for this claim. Resp. Non-Final 4. However, the Examiner finds that Figure 2 does not describe "feedback." RAN 4. In response, Patent Owner contends that one of ordinary skill in the art knows that a "feedback [loop] is the description of a loop in the topography of a circuit where, in addition to its input being connected to its output, its output is also connected to its input via a different path." PO App. Br. 6. Patent Owner argues that the aforementioned configuration is shown in Figure 2 where the output of QT is connected to the gate of P5 and the output of P5 is tied to the input of P6 and the output of P6 is tied to the input of P5. PO App. Br. 7. Patent Owner also provides expert testimony by Dr. Philip Koopman that the setup found in Figure 2 is

designed as a cross-coupled feedback loop. PO App. Br. 7; *see also* Koopman Decl. ¶ [0020].

Requester provides several modes of operation of the circuit in Figure 2 that Requester argues proves the circuit lacks an output stage feedback loop. 3PR Resp. Br. 5-8. However, we do not find this evidence to be persuasive that a cross-coupled feedback loop does not exist, especially in light of the fact that Requester does not argue that Patent Owner's definition of cross-coupled feedback is in error or that the circuit is not set up in a cross-coupled feedback loop configuration. Additionally, we disagree with the Examiner that "feedback" is not described by the Figure. While Patent Owner's Specification might not make mention of the term, we agree with Patent Owner that one of ordinary skill in the art would know what a feedback circuit looks like and that one is disclosed by Figure 2. As such, we cannot sustain the Examiner's rejection of claim 10.

Claim 11 recites "[t]he data transfer arrangement of claim 1 wherein the differential bus is precharged on a different clock phase than the differential data bus." We affirm the Examiner's rejection of claim 11 because, as indicated above, we agree with the Examiner and Requester that the '130 Patent lacks support regarding precharging the differential data bus.

Third Party Appeal

Claim 12 recites "[t]he data arrangement of claim 1 wherein the differential bus and the differential data bus are separate circuits." Patent Owner argues that support for this limitation is found in Figures 1 and 2, wherein the differential bus and the differential data bus are shown and

described as parts of two separate circuits. PO Resp. Br. 11-12. The Examiner agrees and indicates the claim as allowable. RAN 4-5. Requester, however, contends that the '130 Patent does not describe differential bus or differential data bus as circuits themselves, one of ordinary skill in the art would know that a bus is not a circuit in and of itself, and there is nothing in the '130 Patent that describes the buses as being separate circuits.. 3PR App. Br. 21. We agree with Requester's reasoning. We also agree with Requester that claim 12 should have been rejected for lacking enablement since a circuit requires something more than just wires. 3PR App. Br. 21. As such, we reverse the Examiner's decision not to adopt the proposed rejection of claim 12 under 35 U.S.C. § 112 (a) or 35 U.S.C. § 112, first paragraph (pre-AIA) for lacking written description and enablement. A reversal of an Examiner's decision not to adopt a rejection is a new ground of rejection.

CONCLUSION

The Examiner did not err in finding that newly added claims 9 and 11 fail to comply with the written description requirement set forth by 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA).

The Examiner erred in finding that newly added claim 10 fails to comply with the written description requirement set forth by 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA).

The Examiner erred in in failing to adopt Requester's proposed rejection of claim 12 under 35 U.S.C. § 112

DECISION

We affirm the Examiner's decision to reject claims 9 and 11 under 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA).

We reverse the Examiner's decision to reject claim 10 under 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA).

We reverse the Examiner's decision not to adopt the proposed rejection of claim 12 under 35 U.S.C. § 112(a) or 35 U.S.C. § 112, first paragraph (pre-AIA).

The decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.77(b). Section 41.77(b) provides that "a new ground of rejection . . . shall not be considered final for judicial review." That section also provides that Patent Owner, WITHIN ONE MONTH FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal proceeding as to the rejected claims:

> (1) *Reopen prosecution.* The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.
>
> (2) *Request rehearing.* The owner may request that the proceeding be reheard under § 41.79 by the Board upon the same record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

In accordance with 37 C.F.R. § 41.79(a)(1), the "[p]arties to the appeal may file a request for rehearing of the decision within one month of the date of: . . . [t]he original decision of the Board under § 41.77(a)." A request for rehearing must be in compliance with 37 C.F.R. § 41.79(b). Comments in opposition to the request and additional requests for rehearing must be in accordance with 37 C.F.R. § 41.79(c), respectively. Under 37 C.F.R. § 41.79(e), the times for requesting rehearing under paragraph (a) of this section, for requesting further rehearing under paragraph (c) of this section, and for submitting comments under paragraph (b) of this section may not be extended.

An appeal to the United States Court of Appeals for the Federal Circuit under 35 U.S.C. §§ 141-144 and 315 and 37 C.F.R. § 1.983 for an *inter partes* reexamination proceeding "commenced" on or after November 2, 2002 may not be taken "until all parties' rights to request rehearing have been exhausted, at which time the decision of the Board is final and appealable by any party to the appeal to the Board." 37 C.F.R. § 41.81. *See also* MPEP § 2682 (8th ed., Rev. 7, July 2008).

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

AFFIRMED-IN-PART
37 C.F.R. § 41.77(b)

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