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Attorney Docket No. 20181-5US  
Client Ref No. PPA-5

02-22-00

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BOX PATENT APPLICATION  
Washington, D.C. 20231

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By: \_\_\_\_\_

*Kevin T. LeMond*

Jc678 U.S. PTO  
09/505656  
02/17/00

02/17/00  
Jc600 U.S. PTO

Transmitted herewith for filing is the  
 patent application of

Inventor(s)/Applicant Identifier: Andrew V. Podlesny et al.

For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

This application claims priority from each of the following Application Nos./filing dates:  
60/120,531/Filed 2/17/99  
the disclosure(s) of which is (are) incorporated by reference.

Enclosed are:

- 1 sheet(s) of [ ] formal  informal drawing(s).
- A [ ] signed  unsigned Declaration.
- A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27  is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.

**In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.**

**DO NOT CHARGE THE FILING FEE AT THIS TIME.**

*Kevin T. LeMond*

Kevin T. LeMond  
Reg No.: 35,933  
Attorneys for Applicant

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SF 1036480 v1

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS  
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov  
Application or Patent No.: \_\_\_\_\_  
Filed or Issued: \_\_\_\_\_  
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

- the owner of the small business concern identified below
- an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Elbrus International Limited  
Address of Small Business Concern: P.O. Box 265  
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov described in:

- the specification filed herewith;
- Application No. \_\_\_\_\_, filed \_\_\_\_\_;
- Patent No. \_\_\_\_\_, issued \_\_\_\_\_.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below\* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

\*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

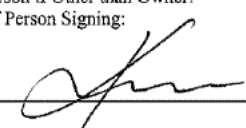
Name: \_\_\_\_\_  
Address: \_\_\_\_\_  
 Individual                       Small Business Concern                       Nonprofit Organization

Name: \_\_\_\_\_  
Address: \_\_\_\_\_  
 Individual                       Small Business Concern                       Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim  
Title of Person if Other than Owner: President  
Address of Person Signing: 14 Bolshoy Savvinsky per.  
Moscow 119435, Russia

Signature 

Date 02/04/2000

SF 1058186 v1

**PATENT APPLICATION**

**HIGH SPEED LOW POWER DATA TRANSFER SCHEME**

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Assignee:

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Entity: Small business concern

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PATENT

Attorney Docket No.: 20181-5US

Client Reference No.: PPA-5

**HIGH SPEED LOW POWER DATA TRANSFER SCHEME**

5                    This application claims priority from U.S. Provisional Patent Application  
No. 60/120,531, filed February 17, 1999, the disclosure of which is incorporated herein  
by reference in its entirety.

## BACKGROUND OF THE INVENTION

## 10    1.    Field Of The Invention

The present invention relates to a data transfer scheme, and more particularly, to a high speed and low power CMOS data transfer scheme.

## 15    2.    Description Of The Prior Art

Today's requirements for electronic circuits require high speed. Additionally, the circuits should be as small and simple as possible due to the ever increasing number of circuits that are crowding today's chip devices. Furthermore, circuits for data transfer should not be sensitive to circuit parameter mismatches, noise, and deviations in various applied voltages.

20

## SUMMARY OF THE INVENTION

The present invention provides a high speed and low power CMOS data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier  
25    that serves as a bus receiver.

In accordance with one embodiment of the present invention, a data transfer arrangement includes two bus drivers, a voltage precharge source, a differential bus coupled to the bus drivers and to the voltage precharge source, and a latching sense amplifier coupled to the differential bus.

30                    In accordance with another embodiment of the present invention, the latching sense amplifier is arranged as a cross coupled latched amplifier.

In accordance with a further embodiment of the present invention, the two bus drivers consist of active pull up/pull down bus drivers.

Thus, the present invention provides a data transfer arrangement that operates at a high speed and uses low power. The data transfer arrangement is faster  
 5 because the bus voltage swing passes directly to high gain nodes of the cross-coupled latched amplifier. Additionally, the data transfer arrangement uses a lower number of stacked transistors coupled between the supply voltage and the high gain nodes when compared to the prior art. Additionally, the arrangement according to the present invention is less sensitive to deviations in voltage sources and the deviation of threshold  
 10 voltage concerns of the input transistors. Additionally, the arrangement is less sensitive to circuit parameter mismatches, data bus common mode noise and power bus noises.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred embodiments below, in conjunction with reference to the drawings, in which like numerals represent  
 15 like elements.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a differential data transfer arrangement in accordance with the present invention; and

Figure 2 is a schematic of a circuit for a sense amplifying latch for use in  
 20 the data transfer arrangement illustrated in Figure 1.

#### DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a data transfer arrangement circuit 10 that includes two bus drivers 11, 12, a precharge circuit 13, and two complementary bus lines 14, 15. The  
 25 bus lines are inputs to a bus receiver 16 that is arranged as a latching sense amplifier.

The two bus drivers are complementary and consist, preferably, of two active pull up/active pull down bus drivers.

Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

30 During the bus precharge phase, the control input PR (control signal for bus precharge circuit 13) is high and signal inputs DT (true phase of dual-rail data function) and DC (complement phase of dual-rail data function) are low. The true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23

are in high impedance state and both bus lines are equalized and precharged to a potential  $V_{pr}$  (buses precharging voltage level) through the turned on transistors 24, 25 and 26.

During the data transfer phase, the control input PR is low. The signal inputs become differential: DT is high and DC is low, and vice versa. One of the drivers is pulled up and charges the appropriate bus line from the precharged level  $V_{pr}$  toward a more positive  $V_{dd} - V_t$  (where  $V_t$  is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged level  $V_{pr}$  towards a more negative level  $V_{ss}$  (ground). This provides a differential voltage:  $+dV$  and  $-dV$  from the precharging level  $V_{pr}$  between true and complement bus lines. To provide proper operation of the bus receiver (the sensing amplifier), the minimum voltage difference  $2 * dV_{min}$  (swing) between the lines may be about 0.05-- 0.20V. This low voltage swing is a basis to obtain high frequency of data transfer through the bus.

Figure 2 illustrates sensing amplifier 16. Preferably, the sensing amplifier is a cross-coupled latched amplifier.

The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode. The cross-coupled latched amplifier is isolated from the power buses (transistors 30 and 31 are turned off). Transistors 32 and 33 are turned on and thus, the bus voltage swing passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to  $V_{dd}$  and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high.

When the control input CLK is high and the bus driver is in the precharge mode, the sensing amplifier is in the data transfer mode. Transistors 32 and 33 are turned off and isolate the internal nodes IT and IC of the latched amplifier from the bus lines. The cross-coupled latched amplifier is connected to power buses (transistors 30 and 31 are turned on) and it begins to amplify the low voltage swings of the internal nodes IT

and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low.

The use of domino output stages in accordance with the present invention instead of static inverters is necessary to avoid leakage currents and output glitches, which may appear because potentials of nodes IT and IC are approximately equal to  $V_{pr}$  during the operating cycle of the bus driver. Weak PMOS transistors 34 and 35 are preferably included in the sensing amplifier to help prevent output glitches.

The data transfer arrangement in accordance with the present invention provides an increase in speed due to the differential low voltage swing bus driver in combination with the use of the latched differential sense amplifier as the bus receiver.

A further increase in speed is attained with the data transfer arrangement due to the pull up/pull down bus drivers, which provide equal low differential voltage swings  $+dV/ -dV$  in both bus lines. This allows both bus lines to be active during the data transfer phase, eliminates the necessity to use special circuits for holding the precharged level and leads to a reduction in the capacitance load of the driver.

The buses precharging to the specific level between ground and  $V_d$  ( $V_{pr} = K * V_{dd}$ , where  $K = 1/3$  for the ideal MOS model) also provides: equal charge and discharge driver currents  $I_{ch} = I_{dch}$ , provided by the NMOS pull up follower and the NMOS pull down switch, respectively, and therefore, equal differential voltage swings  $dV$  in both charged and discharged bus during the data transfer phase  $P_{dtf}$ :  $+dV = I_{ch} * D_{dtf} / C_{LOAD}$ ; and  $-dV = I_{dch} * T_{dtf} / C_{LOAD}$ .  $I_{ch}$  represents the driver pull up output current (which provides the  $C_{LOAD}$  charging from  $V_{pr}$  up to  $V_{dd}$ );  $I_{dch}$  represents the driver pull down output current (providing the  $C_{LOAD}$  discharging from  $V_{pr}$  up to  $V_{ss}$ );  $C_{LOAD}$  represents the bus lines' capacitances;  $+dV$  represents the bus voltage change up from  $V_{pr}$  during data transfer phase;  $-dV$  represents the bus voltage change down from  $V_{pr}$  during data transfer phase; and  $T_{dtf}$  represents the data transfer phase duration. The buses precharging to the specific level between ground and  $V_{dd}$  also provides high noise immunity due to active mode for both buses that equal low output resistances of the drivers in pull up and pull down mode and; low total power consumed by drivers during the cycle of operation (transfer plus precharge).

The latched sense amplifier is faster due to the bus voltage swing passing directly to the high-gain nodes IT and IC of the cross-coupled latched amplifier, the lower number of stacked transistors that are connected between the supply voltage  $V_{dd}$  (or

$V_{cc}$ ) and nodes IT and IC, the fact that during latching of the IT and IC nodes, the nodes are charged by  $K \cdot V_{dd}$  and  $(1-K) \cdot V_{dd}$  instead of simply  $V_{dd}$ . Additionally, the speed of the latched sensing amplifier is effected little by the deviation of voltage  $V_{pr}$  and the deviation of the threshold voltage of the input transistors.

5                    In addition to the higher speed and low power consumption of the data transfer arrangement in accordance with the present invention, the arrangement is also less sensitive to circuit parameters mismatching, data bus common mode noise and power buses' noises since both drivers are active during data transfer phase. During the appropriate bus precharge phase, the bus receiver is isolated from the bus lines.

10                    Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.



WHAT IS CLAIMED IS:

- 1                   1.     A data transfer arrangement comprising:  
2                   two bus drivers;  
3                   a voltage precharge source;  
4                   a differential bus coupled to the bus drivers and to the voltage precharge  
5 source; and  
6                   a latching sense amplifier coupled to the differential bus.
  
- 1                   2.     A data transfer arrangement in accordance with claim 1 wherein  
2 the latching sense amplifier comprises a cross coupled latched amplifier.
  
- 1                   3.     A data transfer arrangement in accordance with claim 1 wherein  
2 the bus drivers consist of active pull up/pull down bus drivers.



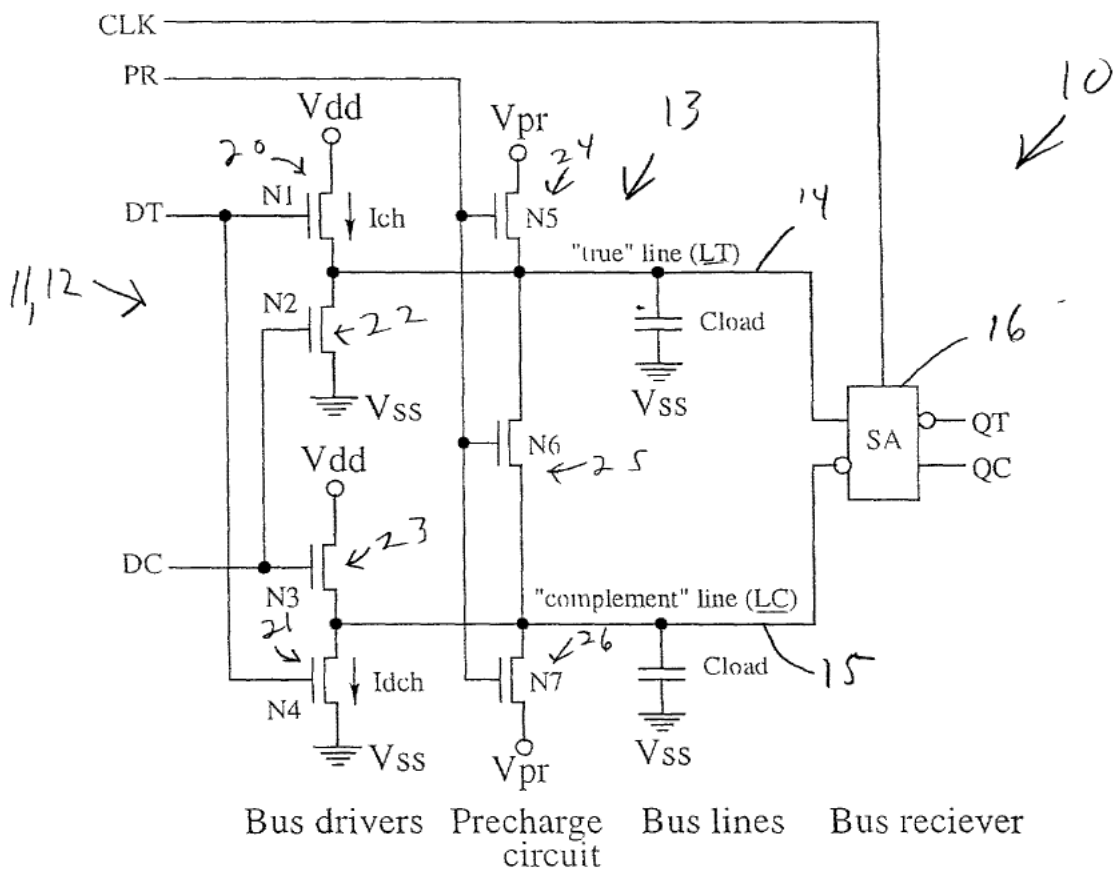


Fig. 1.

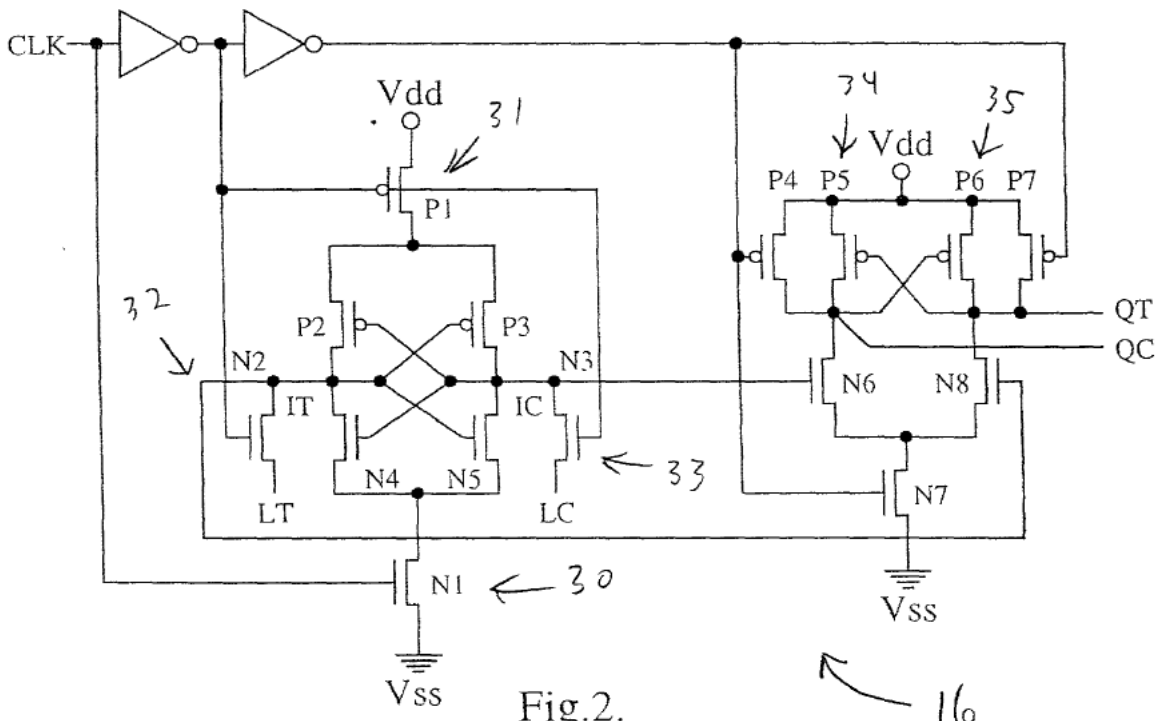


Fig. 2.

**DECLARATION AND POWER OF ATTORNEY**

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which  X  is attached hereto or   was filed on   as Application No.   and was amended on   (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

**Prior Foreign Application(s)**

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

J. Georg Seka, Reg. No. 24,491  
 Robert J. Bennett, Reg. No. 27,533  
 Charles E. Krueger, Reg. No. 30,077  
 Charles J. Kulas, Reg. No. 35,809  
 Kevin T. LeMond, Reg. No. 35,933  
 George B.F. Yee, Reg. No. 37,478

Chad S. Hilyard, Reg. No. 40,647  
 Gerald T. Gray, Reg. No. 41,797  
 Daniel D. Tagliaferri, Reg. No. 43,178  
 Thomas D. Franklin, Reg. No. 43,616  
 Patrick M. Boucher, Reg. No. 44,037

Send Correspondence to: <b>Kevin T. LeMond</b> <b>TOWNSEND and TOWNSEND and CREW LLP</b> <b>Two Embarcadero Center, 8<sup>th</sup> Floor</b> <b>San Francisco, California 94111-3834</b>	Direct Telephone Calls to: (Name, Reg. No., Telephone No.) Name: Kevin T. LeMond Reg. No.: 35933 Telephone: 415-576-0200
------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------

Full Name of Inventor 1:	Last Name: <b>Podlesny</b>	First Name: <b>Andrew</b>	Middle Name or Initial: <b>V.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
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Full Name of Inventor 2:	Last Name: <b>Malshin</b>	First Name: <b>Alexander</b>	Middle Name or Initial: <b>V.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
Post Office Address:	Post Office Address: <b>Apt. 608, 50 Frunzenskaya Nabergnaya</b>	City: <b>Moscow</b>	State/Country: <b>Russia</b>	Postal Code: <b>119270</b>
Full Name of Inventor 3:	Last Name: <b>Solomatnikov</b>	First Name: <b>Alexander</b>	Middle Name or Initial: <b>Y.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
Post Office Address:	Post Office Address: <b>14, Bolshoi Savvinski Per.</b>	City: <b>Moscow</b>	State/Country: <b>Russia</b>	Postal Code: <b>119435</b>

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  _____ Andrew V. Podlesny	Signature of Inventor 2  _____ Alexander V. Malshin	Signature of Inventor 3  _____ Alexander Y. Solomatnikov
Date	Date	Date

SF 1060790 v1

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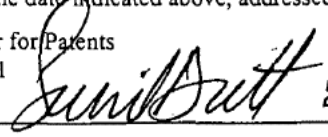
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Date of Deposit: February 17, 2000

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Assistant Commissioner for Patents  
Washington, D.C. 20231

By: \_\_\_\_\_



Sir:

Transmitted herewith for filing is the  
[ X ] patent application of

Inventor(s)/Applicant Identifier: Andrew V. Podlesny et al.

For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

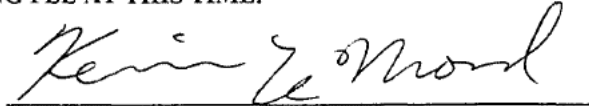
[ X ] This application claims priority from each of the following Application Nos./filing dates:  
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Kevin T. LeMond  
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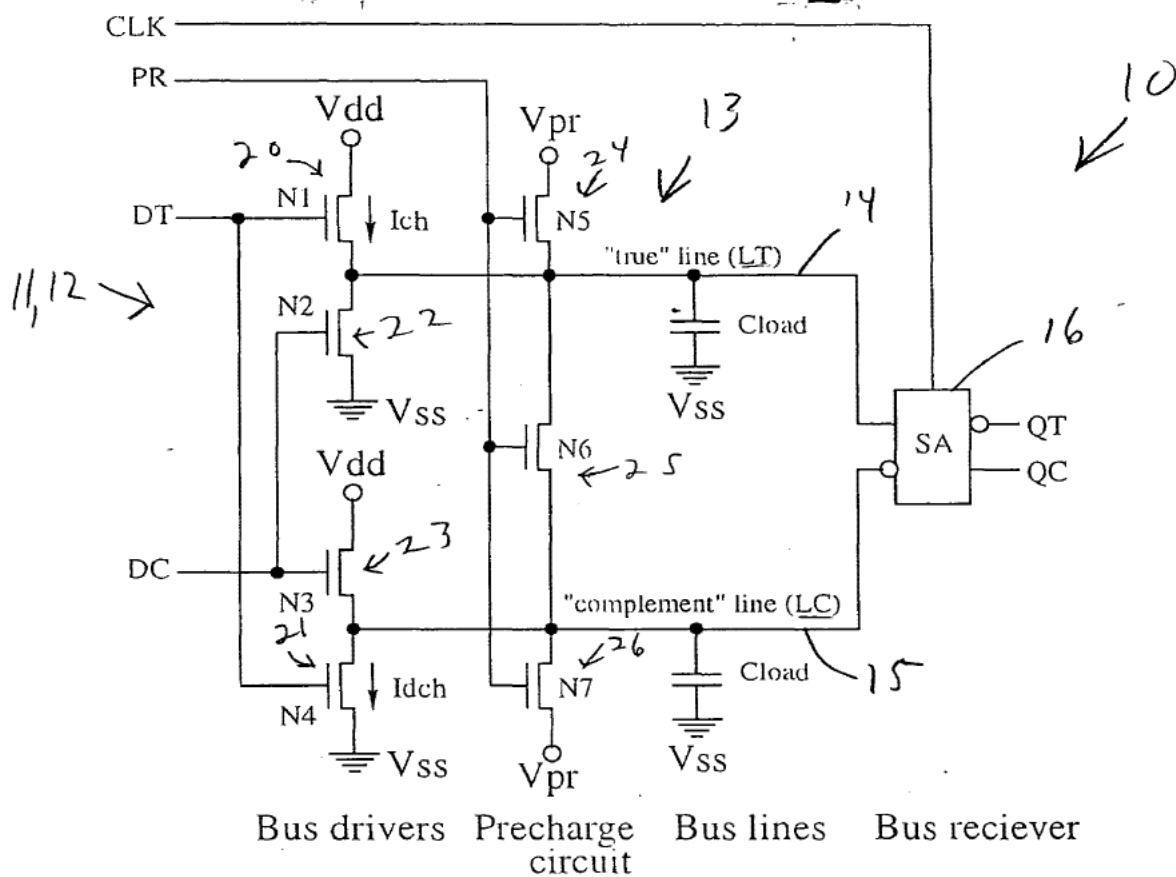
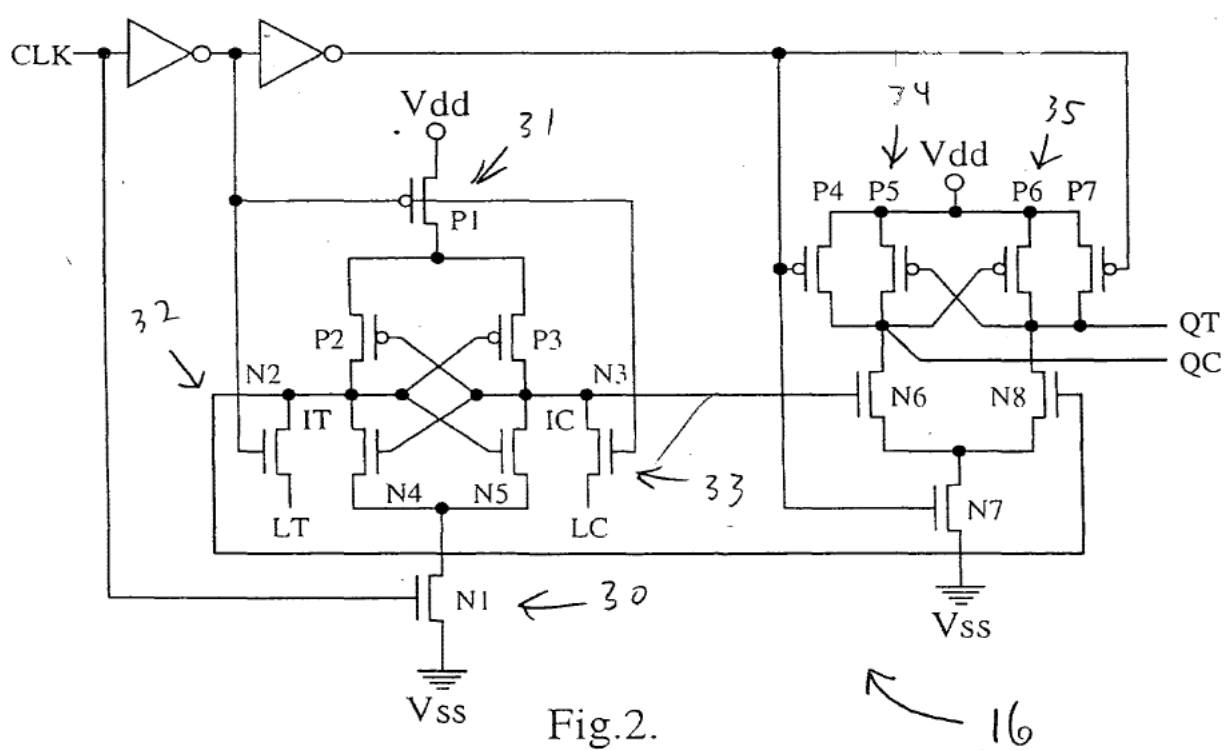


Fig. 1.



2

**PATENT APPLICATION**

**HIGH SPEED LOW POWER DATA TRANSFER SCHEME**

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Moscow, Russia 119435

Entity: Small business concern

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**BACKGROUND OF THE INVENTION**

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                  The present invention relates to a data transfer scheme, and more  
particularly, to a high speed and low power CMOS data transfer scheme.

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**SUMMARY OF THE INVENTION**

                  The present invention provides a high speed and low power CMOS data  
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transfer arrangement includes two bus drivers, a voltage precharge source, a differential  
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30

                  In accordance with another embodiment of the present invention, the  
latching sense amplifier is arranged as a cross coupled latched amplifier.

In accordance with a further embodiment of the present invention, the two bus drivers consist of active pull up/pull down bus drivers.

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Figure 1 is a schematic of a differential data transfer arrangement in accordance with the present invention; and

Figure 2 is a schematic of a circuit for a sense amplifying latch for use in  
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#### DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a data transfer arrangement circuit 10 that includes two bus drivers 11, 12, a precharge circuit 13, and two complementary bus lines 14, 15. The  
 25 bus lines are inputs to a bus receiver 16 that is arranged as a latching sense amplifier.

The two bus drivers are complementary and consist, preferably, of two active pull up/active pull down bus drivers.

Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

30 During the bus precharge phase, the control input PR (control signal for bus precharge circuit 13) is high and signal inputs DT (true phase of dual-rail data function) and DC (complement phase of dual-rail data function) are low. The true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23

are in high impedance state and both bus lines are equalized and precharged to a potential  $V_{pr}$  (buses precharging voltage level) through the turned on transistors 24, 25 and 26.

During the data transfer phase, the control input PR is low. The signal inputs become differential: DT is high and DC is low, and vice versa. One of the drivers is pulled up and charges the appropriate bus line from the precharged level  $V_{pr}$  toward a more positive  $V_{dd} - V_t$  (where  $V_t$  is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged level  $V_{pr}$  towards a more negative level  $V_{ss}$  (ground). This provides a differential voltage:  $+dV$  and  $-dV$  from the precharging level  $V_{pr}$  between true and complement bus lines. To provide proper operation of the bus receiver (the sensing amplifier), the minimum voltage difference  $2 * dV_{min}$  (swing) between the lines may be about 0.05-- 0.20V. This low voltage swing is a basis to obtain high frequency of data transfer through the bus.

Figure 2 illustrates sensing amplifier 16. Preferably, the sensing amplifier is a cross-coupled latched amplifier.

The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode. The cross-coupled latched amplifier is isolated from the power buses (transistors 30 and 31 are turned off). Transistors 32 and 33 are turned on and thus, the bus voltage swing passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to  $V_{dd}$  and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high.

When the control input CLK is high and the bus driver is in the precharge mode, the sensing amplifier is in the data transfer mode. Transistors 32 and 33 are turned off and isolate the internal nodes IT and IC of the latched amplifier from the bus lines. The cross-coupled latched amplifier is connected to power buses (transistors 30 and 31 are turned on) and it begins to amplify the low voltage swings of the internal nodes IT

4

and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low.

The use of domino output stages in accordance with the present invention instead of static inverters is necessary to avoid leakage currents and output glitches, which may appear because potentials of nodes IT and IC are approximately equal to  $V_{pr}$  during the operating cycle of the bus driver. Weak PMOS transistors 34 and 35 are preferably included in the sensing amplifier to help prevent output glitches.

The data transfer arrangement in accordance with the present invention provides an increase in speed due to the differential low voltage swing bus driver in combination with the use of the latched differential sense amplifier as the bus receiver.

A further increase in speed is attained with the data transfer arrangement due to the pull up/pull down bus drivers, which provide equal low differential voltage swings  $+dV/-dV$  in both bus lines. This allows both bus lines to be active during the data transfer phase, eliminates the necessity to use special circuits for holding the precharged level and leads to a reduction in the capacitance load of the driver.

The buses precharging to the specific level between ground and  $V_d$  ( $V_{pr} = K * V_{dd}$ , where  $K = 1/3$  for the ideal MOS model) also provides: equal charge and discharge driver currents  $I_{ch} = I_{dch}$ , provided by the NMOS pull up follower and the NMOS pull down switch, respectively, and therefore, equal differential voltage swings  $dV$  in both charged and discharged bus during the data transfer phase  $P_{dtf}$ :  $+dV = I_{ch} * D_{dtf} / C_{LOAD}$ ; and  $-dV = I_{dch} * T_{dtf} / C_{LOAD}$ .  $I_{ch}$  represents the driver pull up output current (which provides the  $C_{LOAD}$  charging from  $V_{pr}$  up to  $V_{dd}$ );  $I_{dch}$  represents the driver pull down output current (providing the  $C_{LOAD}$  discharging from  $V_{pr}$  up to  $V_{ss}$ );  $C_{LOAD}$  represents the bus lines' capacitances;  $+dV$  represents the bus voltage change up from  $V_{pr}$  during data transfer phase;  $-dV$  represents the bus voltage change down from  $V_{pr}$  during data transfer phase; and  $T_{dtf}$  represents the data transfer phase duration. The buses precharging to the specific level between ground and  $V_{dd}$  also provides high noise immunity due to active mode for both buses that equal low output resistances of the drivers in pull up and pull down mode and; low total power consumed by drivers during the cycle of operation (transfer plus precharge).

The latched sense amplifier is faster due to the bus voltage swing passing directly to the high-gain nodes IT and IC of the cross-coupled latched amplifier, the lower number of stacked transistors that are connected between the supply voltage  $V_{dd}$  (or

$V_{cc}$ ) and nodes IT and IC, the fact that during latching of the IT and IC nodes, the nodes are charged by  $K \cdot V_{dd}$  and  $(1-K) \cdot V_{dd}$  instead of simply  $V_{dd}$ . Additionally, the speed of the latched sensing amplifier is effected little by the deviation of voltage  $V_{pr}$  and the deviation of the threshold voltage of the input transistors.

5                    In addition to the higher speed and low power consumption of the data transfer arrangement in accordance with the present invention, the arrangement is also less sensitive to circuit parameters mismatching, data bus common mode noise and power buses' noises since both drivers are active during data transfer phase. During the appropriate bus precharge phase, the bus receiver is isolated from the bus lines.

10                    Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.

WHAT IS CLAIMED IS:

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A1

1. A data transfer arrangement comprising:  
two bus drivers;  
a voltage precharge source;  
a differential bus coupled to the bus drivers and to the voltage precharge source; and  
a latching sense amplifier coupled to the differential bus.

1  
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2. ~~The~~ A data transfer arrangement in accordance with claim 1 wherein the latching sense amplifier comprises a cross coupled latched amplifier.

1  
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sub  
A2

3. ~~The~~ A data transfer arrangement in accordance with claim 1 wherein the bus drivers consist of active pull up/pull down bus drivers.

add A3

## HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

## ABSTRACT OF THE DISCLOSURE

A data transfer arrangement. The data transfer arrangement includes two active pull up/active pull down bus drivers and a voltage precharge source. A differential bus is coupled to the bus drivers and to the voltage precharge source. A latching sense amplifier is coupled to the differential bus and serves as the bus receiver. The bus drivers operate in a precharge phase and a data transfer phase. The bus receiver operates in an analogous but opposite manner, i.e., when the bus drivers are in the precharge phase, the bus receiver is in the data transfer phase and when the bus drivers are in the data transfer phase, the bus receiver is in a precharge phase

SF 1068801 v1

**DECLARATION AND POWER OF ATTORNEY**

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which  X  is attached hereto or   was filed on   as Application No.   and was amended on   (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

**Prior Foreign Application(s)**

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

J. Georg Seka, Reg. No. 24,491  
 Robert J. Bennett, Reg. No. 27,533  
 Charles E. Krueger, Reg. No. 30,077  
 Charles J. Kulas, Reg. No. 35,809  
 Kevin T. LeMond, Reg. No. 35,933  
 George B.F. Yee, Reg. No. 37,478

Chad S. Hilyard, Reg. No. 40,647  
 Gerald T. Gray, Reg. No. 41,797  
 Daniel D. Tagliaferri, Reg. No. 43,178  
 Thomas D. Franklin, Reg. No. 43,616  
 Patrick M. Boucher, Reg. No. 44,037

Send Correspondence to: <b>Kevin T. LeMond</b> <b>TOWNSEND and TOWNSEND and CREW LLP</b> Two Embarcadero Center, 8 <sup>th</sup> Floor San Francisco, California 94111-3834	Direct Telephone Calls to: (Name, Reg. No., Telephone No.) Name: Kevin T. LeMond Reg. No.: 35933 Telephone: 415-576-0200
-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------



Full Name of Inventor 1:	Last Name: <b>Podlesny</b>	First Name: <b>Andrew</b>	Middle Name or Initial: <b>V.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
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Full Name of Inventor 2:	Last Name: <b>Malshin</b>	First Name: <b>Alexander</b>	Middle Name or Initial: <b>V.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
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Full Name of Inventor 3:	Last Name: <b>Solomatnikov</b>	First Name: <b>Alexander</b>	Middle Name or Initial: <b>Y.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
Post Office Address:	Post Office Address: <b>14, Bolshoi Savvinski Per.</b>	City: <b>Moscow</b>	State/Country: <b>Russia</b>	Postal Code: <b>119435</b>

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  _____	Signature of Inventor 2  _____	Signature of Inventor 3  _____
Andrew V. Podlesny	Alexander V. Malshin	Alexander Y. Solomatnikov
Date	Date	Date

1060790 v1

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS  
(37 CFR 1.9(f) & 1.27(e)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov  
Application or Patent No.: \_\_\_\_\_  
Filed or Issued: \_\_\_\_\_  
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

- the owner of the small business concern identified below
- an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Elbrus International Limited  
Address of Small Business Concern: P.O. Box 265  
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme, by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov, described in:

- the specification filed herewith;
- Application No. \_\_\_\_\_, filed \_\_\_\_\_;
- Patent No. \_\_\_\_\_, issued \_\_\_\_\_.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below\* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

\*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

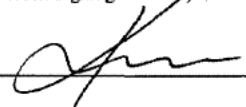
Name: \_\_\_\_\_  
Address: \_\_\_\_\_  
 Individual                       Small Business Concern                       Nonprofit Organization

Name: \_\_\_\_\_  
Address: \_\_\_\_\_  
 Individual                       Small Business Concern                       Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim  
Title of Person if Other than Owner: President  
Address of Person Signing: 14 Bolshov Savvinsky per.  
Moscow 119435, Russia

Signature  Date 02/0/2000



Bib Data Sheet



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS,  
Washington, D.C. 20231

<b>SERIAL NUMBER</b> 09/505,656	<b>FILING DATE</b> 02/17/2000 <b>RULE</b> -	<b>CLASS</b> 326	<b>GROUP ART UNIT</b> 2819	<b>ATTORNEY DOCKET NO.</b> 20181-5US	
<b>APPLICANTS</b> ✓ Andrew V. Podlesny, Moscow, RUSSIAN FEDERATION; ✓ Alexander V. Malshin, Moscow, RUSSIAN FEDERATION; ✓ Alexander Y. Solomatnikov, Moscow, RUSSIAN FEDERATION;					
** CONTINUING DATA ***** THIS APPLN CLAIMS BENEFIT OF 60/120,531 02/17/1999 <i>OR</i> <i>LTW</i>					
* FOREIGN APPLICATIONS *****					
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY ** ** 04/26/2000					
Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		STATE OR COUNTRY RUSSIAN FEDERATION	SHEETS DRAWING 1	TOTAL CLAIMS 3	INDEPENDENT CLAIMS 1
35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance					
Verified and Acknowledged Examiner's Signature <i>[Signature]</i> Initials					
<b>ADDRESS</b> 20350					
<b>TITLE</b> High speed low power data transfer scheme					
<b>FILING FEE RECEIVED</b> 410	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees ( Filing ) <input type="checkbox"/> 1.17 Fees ( Processing Ext. of time ) <input type="checkbox"/> 1.18 Fees ( Issue ) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective December 29, 1999

Application or Docket Number

09/505654

**CLAIMS AS FILED - PART I**

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	3	minus 20= *
INDEPENDENT CLAIMS	1	minus 3= *
MULTIPLE DEPENDENT CLAIM PRESENT		

\* If the difference in column 1 is less than zero, enter "0" in column 2

**SMALL ENTITY TYPE**  **OR** **OTHER THAN SMALL ENTITY**

RATE	FEE	OR	RATE	FEE
	345.00			690.00
X\$ 9=			X\$18=	
X39=			X78=	
+130=			+260=	
TOTAL			TOTAL	690

**CLAIMS AS AMENDED - PART II**

AMENDMENT A	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 5	Minus ** 20	=
Independent	* 2	Minus *** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

**SMALL ENTITY**  **OR** **OTHER THAN SMALL ENTITY**

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=			X\$18=	
X39=			X78=	
+130=			+260=	
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AMENDMENT B	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=			X\$18=	
X39=			X78=	
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AMENDMENT C	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=			X\$18=	
X39=			X78=	
+130=			+260=	
TOTAL ADDIT. FEE			TOTAL ADDIT. FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

3678 U.S. PTO  
09/505656  
02/17/00

326	95	CLASS	SUBCLASS	ISSUE CLASSIFICATION
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PATENT NUMBER
6386130
6386130

U.S. UTILITY Patent Application

O.I.P. # <i>26</i>	PATENT DATE
SCANNED <i>CHC</i> <i>oa</i> <i>me</i>	APR 02 2002

APPLICATION NO. 09/505656	CONT/PRIOR D	CLASS 326	SUBCLASS 95	ART UNIT 2819	EXAMINER V. TAN
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APPLICANTS  
Andrew Podlesny  
Alexander Malshin  
Alexander Solomatnikov

TITLE  
High speed low power data transfer scheme

PTO-2940  
12/99

ISSUING CLASSIFICATION						
ORIGINAL		CROSS REFERENCE(S)				
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
326	95	326	96	97	90	
INTERNATIONAL CLASSIFICATION		327	57	55	52	
H03K	19/0185					
G11C	7/06					

Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <i>13</i>	Figs. Drwg. <i>2</i>	Print Fig. <i>1</i>	Total Claims <i>8</i>	Print Claim for O.G. <i>1</i>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<i>ILK</i> <i>8/15/01</i> (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED <i>8/17/01</i>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____	<i>Michael J. Tokar</i> (Primary Examiner) <i>8/6/01</i> (Date)			ISSUE FEE <i>(w)</i> Amount Due <i>620</i> - Date Paid <i>11-6-01</i>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<i>John</i> <i>8/6/01</i> (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER <i>K75</i>	

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A  
(Rev. 5/92)

FILED WITH:  DISK (CRF)  FICHE  CD-ROM  
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(FACE)



ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	smc		2/28/02
O.I.P.E. CLASSIFIER			7/28/02
FORMALITY REVIEW	JW	65246	4-21-00
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

- ✓ ..... Rejected
- ..... Allowed
- (Through numeral)..... Canceled
- + ..... Restricted
- N ..... Non-elected
- I ..... Interference
- A ..... Appeal
- O ..... Objected

Claim	Final	Original	Date
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If more than 150 claims or 10 actions  
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## FORMALITIES LETTER



\*OC00000005078578\*

UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark OfficeAddress: COMMISSIONER OF PATENT AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

20350  
TOWNSEND AND TOWNSEND AND CREW LLP  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO, CA 94111

Date Mailed: 04/27/2000

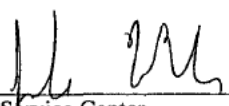
**NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION****FILED UNDER 37 CFR 1.53(b)***Filing Date Granted*

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.  
*Applicant must submit \$ 690 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).*
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is \$ 820.**

---

*A copy of this notice **MUST** be returned with the reply.*

  
Customer Service Center  
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY



**FORMALITIES LETTER**



\*OC00000005078578\*



**UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office**

Address: COMMISSIONER OF PATENT AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

20350  
TOWNSEND AND TOWNSEND AND CREW LLP  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO, CA 94111



Date Mailed: 04/27/2000

**NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION**

**FILED UNDER 37 CFR 1.53(b)**

*Filing Date Granted*

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.  
*Applicant must submit \$ 690 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).*
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is \$ 820.**

*A copy of this notice **MUST** be returned with the reply.*

Customer Service Center  
Initial Patent Examination Division (703) 308-1202

**PART 2 - COPY TO BE RETURNED WITH RESPONSE**

06/29/2000 GTEFFERA 00000070 201430 09505656

01 FC:201 345.00 CH  
02 FC:205 65.00 CH

Secretary  
\$

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

PATENT  
Attorney Docket No. 20181-000500US  
Client Ref. No.: PPA-5

Assistant Commissioner for Patents  
Attn: Box Missing Parts  
Washington, D.C. 20231



on 6/22/00  
TOWNSEND and TOWNSEND and CREW LLP  
By Rahym Gole

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Andrew V. Podlesny et al.

Examiner: Not Yet Assigned

Application No.: 09/505,656

Art Unit: 2819

Filed: February 17, 2000

TRANSMITTAL LETTER -  
RESPONSE TO NOTICE OF MISSING  
PARTS

For: HIGH-SPEED LOW-POWER DATA  
TRANSFER SCHEME

Attn: Box Missing Parts  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Pursuant to the Notice to File Missing Parts of Application - Filing Date Granted mailed April 27, 2000, enclosed are the following to be made of record in the above-identified application:

- 1) Executed Declaration and Power of Attorney
- 2) Verified Statement Claiming Small Entity Status
- 3) Copy of Notice of Missing Parts

Please charge Deposit Account No. 20-1430 for the following fees:

Small entity:	(a)	Filing Fee (§ 1.16(a)) (Small Entity)	\$ 345.00
	(c)	Missing Parts Surcharge	\$ 65.00

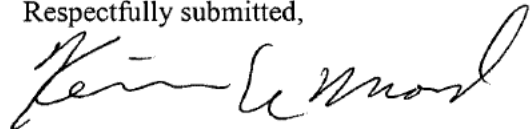
Andrew V. Podlesny et al.  
Application No.: 09/505,656  
Page 2

**TOTAL FEES TO BE CHARGED**

\$410.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment, to Deposit Account No. 20-1430. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,



Kevin T. LeMond  
Reg. No. 35, 933

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8th Floor  
San Francisco, California 94111-3834  
(415) 576-0200  
Fax (415) 576-0300  
KTL:rg

SF 1107691 v1



**DECLARATION AND POWER OF ATTORNEY**

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which    is attached hereto or   X   was filed on February 17, 2000 as Application No. 09/505,656.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

**Prior Foreign Application(s)**

Country	Application No.	Date of Filing	Priority Claimed Under, 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

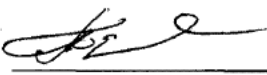
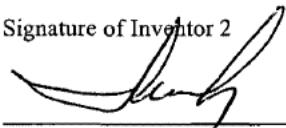
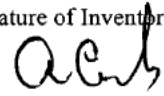
J. Georg Seka, Reg. No. 24,491  
 Robert J. Bennett, Reg. No. 27,533  
 Charles E. Krueger, Reg. No. 30,077  
 Charles J. Kulas, Reg. No. 35,809  
 Kevin T. LeMond, Reg. No. 35,933  
 George B.F. Yee, Reg. No. 37,478

Chad S. Hilyard, Reg. No. 40,647  
 Gerald T. Gray, Reg. No. 41,797  
 Daniel D. Tagliaferri, Reg. No. 43,178  
 Thomas D. Franklin, Reg. No. 43,616  
 Patrick M. Boucher, Reg. No. 44,037

Send Correspondence to: <b>Kevin T. LeMond</b> <b>TOWNSEND and TOWNSEND and CREW LLP</b> Two Embarcadero Center, 8 <sup>th</sup> Floor San Francisco, California 94111-3834	Direct Telephone Calls to: (Name, Reg. No., Telephone No.) Name: Kevin T. LeMond Reg. No.: 35933 Telephone: 415-576-0200
-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------

Full Name of Inventor 1:	Last Name: <b>Podlesny</b>	First Name: <b>Andrew</b>	Middle Name or Initial: <b>V.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
Post Office Address:	Post Office Address: <b>Apt. 192, 38/2 Menzinsky St.</b>	City: <b>Moscow</b>	State/Country: <b>Russia</b>	Postal Code: <b>129281</b>
Full Name of Inventor 2:	Last Name: <b>Malshin</b>	First Name: <b>Alexander</b>	Middle Name or Initial: <b>V.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
Post Office Address:	Post Office Address: <b>Apt. 608, 50 Frunzenskaya Nabernaya</b>	City: <b>Moscow</b>	State/Country: <b>Russia</b>	Postal Code: <b>119270</b>
Full Name of Inventor 3:	Last Name: <b>Solomatnikov</b>	First Name: <b>Alexander</b>	Middle Name or Initial: <b>Y.</b>	
Residence and Citizenship:	City: <b>Moscow</b>	State/Foreign Country: <b>Russia</b>	Country of Citizenship: <b>Russia</b>	
Post Office Address:	Post Office Address: <b>14, Bolshoi Savvinski Per.</b>	City: <b>Moscow</b>	State/Country: <b>Russia</b>	Postal Code: <b>119435</b>

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1 	Signature of Inventor 2 	Signature of Inventor 3 
Andrew V. Podlesny	Alexander V. Malshin	Alexander Y. Solomatnikov
Date 06/14/2000	Date 06/14/2000	Date 06/14/2000

SF 1060790 v1



Attorney Docket 020181-000500US (PPA-5)

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS  
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov  
Application or Patent No.: \_\_\_\_\_  
Filed or Issued: \_\_\_\_\_  
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

- the owner of the small business concern identified below
- an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Eibus International Limited  
Address of Small Business Concern: P.O. Box 265  
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov described in:

- the specification filed herewith;
- Application No. \_\_\_\_\_, filed \_\_\_\_\_;
- Patent No. \_\_\_\_\_, issued \_\_\_\_\_.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below\* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

\*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name: \_\_\_\_\_  
Address: \_\_\_\_\_  
 Individual                       Small Business Concern                       Nonprofit Organization

Name: \_\_\_\_\_  
Address: \_\_\_\_\_  
 Individual                       Small Business Concern                       Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim  
Title of Person if Other than Owner: President  
Address of Person Signing: 14 Bolshoy Savvinskyy per.  
Moscow 119435, Russia

Signature:  Date: 02/16/2000

SF 1058186 v1

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Attorney Docket No.: 20181-000500US  
Client Reference No.: PPA-5

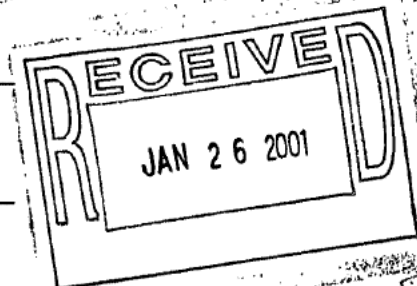
2819  
PATENT  
#5/Suppl  
IPB  
3/2/01  
29

Assistant Commissioner for Patents  
Washington, D.C. 20231

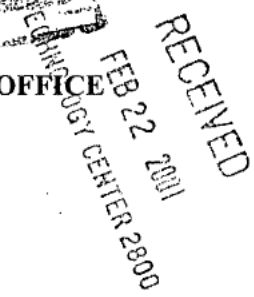
On 1/24/01

TOWNSEND and TOWNSEND and CREW LLP

By: AClini8



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re application of:

Andrew V. Podlesny et al.

Application No.: 09/505,656

Filed: Herewith

For: HIGH-SPEED LOW-POWER  
DATA TRANSFER SCHEME

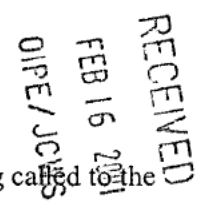
Examiner: Unassigned

Art Unit: 2819

SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT UNDER 37  
CFR §1.97 and §1.98

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:



The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copy of the reference is enclosed. It is respectfully requested that the cited reference be expressly considered during the prosecution of this application, and the reference be made of record therein and appear among the "references cited" on any patent to issue therefrom.

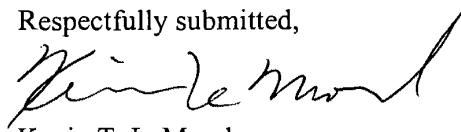
As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Andrew V. Podlesny et al.  
Application No.: 09/505,656  
Page 2

PATENT

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Kevin T. LeMond  
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8<sup>th</sup> Floor  
San Francisco, California 94111-3834  
Tel: 415-576-0200  
Fax: 415-576-0300  
KTL:lo

SF 1178827 v1





**UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office** *DB* *RJ*

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/505,656	02/17/00	PODLESNY	A 20181-5US

020350 MM92/0222  
TOWNSEND AND TOWNSEND AND CREW  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO CA 94111-3834

EXAMINER

TAN, V  

ART UNIT	PAPER NUMBER
----------	--------------

2819

DATE MAILED: 02/22/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

<b>Office Action Summary</b>	<b>Application No.</b> 09/505,656	<b>Applicant(s)</b> PODLESNY ET AL.	
	<b>Examiner</b> Vibol Tan	<b>Art Unit</b> 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1)  Responsive to communication(s) filed on 17 February 2000.
- 2a)  This action is **FINAL**.                      2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4)  Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) 1-3 is/are rejected.
- 7)  Claim(s) \_\_\_\_\_ is/are objected to.
- 8)  Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11)  The proposed drawing correction filed on \_\_\_\_\_ is: a)  approved b)  disapproved.
- 12)  The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

- 13)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a)  All    b)  Some \*    c)  None of:
1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14)  Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

- |                                                                                               |                                                                              |
|-----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| 15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 17) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 20) <input type="checkbox"/> Other:                                          |

## DETAILED ACTION

### *Claim Objections*

1. In claims 2 and 3 Change "A" to "The".

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. PAT. 5,598,371) in view of Hayakawa (U.S. PAT. 6,184,722 B1).

Lee et al. teaches all claimed features of claim 1 in Fig. 1, a data transfer arrangement comprising: two bus drivers (114, 116; 120, 122); a differential bus (line DIO and line DIOB) coupled to the bus drivers and to the voltage precharge source (PRECH); with the exception of teaching a latching sense amplifier coupled to the differential bus. However, Hayakawa teaches in Fig. 5A a latching sense amplifier (2) coupled to the differential bus (4, 6).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicants' invention to have combined the circuit of Lee et al. along with the circuit of Hayakawa to provide a sense amplifier that can sense a low level differential quickly and can amplifier low level differential small swing input signals.

Regarding claim 2, Hayakawa further teaches in Fig. 5A the data transfer arrangement of claim 1, wherein the latching sense amplifier comprises a cross coupled latch amplifier (Q3-Q6).


Regarding claim 3, Lee et al. further teaches in Fig. 1, the data transfer arrangement of claim 1, wherein the bus drivers consist of active pull up/pull down bus drivers (114, 114, 120, 122).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Proebsting teaches a differential sense amplifier circuit. Shiratake teaches a sense amplifier circuit. Yamauchi teaches a signal transmitting circuit, small receiving circuit, signal transmitting/receiving circuit. Yoon teaches a sense amplifiers including bipolar transistor input buffers and field effect transistor latch circuits. Decuir teaches a system and method for a switch data bus termination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

  
**PATRICK WAMSLEY**  
**PRIMARY EXAMINER**

Vibol Tan

Patent Examiner, AU 2819

<b>Notice of References Cited</b>	Application/Control No. 09/505,656	Applicant(s)/Patent Under Reexamination PODLESNY ET AL.	
	Examiner Vibol Tan	Art Unit 2819	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number	Date	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY			
	A	US-6154064-	11-2000	Proebsting	327	55
	B	US-6147514-	11-2000	Shiratake	327	55
	C	US-6028455-	02-2000	Yamauchi	327	52
	D	US-6184722-B1	02-2001	Hayakawa	327	55
	E	US-5894233-	04-1999	Yoon	327	55
	F	US-5781028-	07-1998	Decuir	326	30
	G	US-5598371-	01-1997	Lee et al.	365	189.05
	H	US- -				
	I	US- -				
	J	US- -				
	K	US- -				
	L	US- -				
	M	US- -				

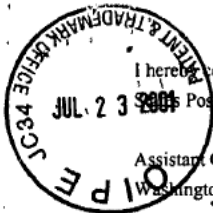
**FOREIGN PATENT DOCUMENTS**

*		Document Number	Date	Country	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY				
	N	- -					
	O	- -					
	P	- -					
	Q	- -					
	R	- -					
	S	- -					
	T	- -					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents  
Washington, D.C. 20231

On July 20, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Julie Taylor Clough

PATENT  
Attorney Docket No.: 20181-5  
Client Reference No.: 20181-5

*Handwritten:* A6/a  
RECEIVED  
JUL 27 2001  
TECHNOLOGY CENTER 2800

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Andrew V. Podlesny et al.

Application No.: 09/505,656

Filed: June 27, 2000

For: HIGH-SPEED LOW-POWER  
DATA TRANSFER SCHEME

Examiner: Vibol Tan

Art Unit: 2819

AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Applicants request a two-month extension of time from May 22, 2001 to July 22, 2001 and authorize the Commissioner to charge the fee therefor to our deposit account in accordance with the attached Fee Transmittal.

In response to the Office Action mailed February 22, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1 and 3. Please cancel claim 2 and add new claims 4-9.

1. (AMENDED) A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge

07/25/2001 WARRHAN1 00000017 201430

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source; and

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data bus; and  
stage.

a latching sense amplifier coupled to the differential bus;  
wherein the latching sense amplifier comprises:  
a first stage including a cross-coupled latch coupled to a differential  
an output stage coupled to an output of said first stage;  
wherein the output of the first stage is coupled to an input of the output

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(AMENDED) The data transfer arrangement in accordance with claim 1  
wherein the bus drivers comprise active pull-up and active pull-down bus drivers.

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(NEW) The data transfer arrangement in accordance with claim 1, wherein the  
first stage of the latching sense amplifier comprises:

a plurality of input pass transistors each having a gate, a source terminal, and a  
drain; and

a plurality of NMOS and PMOS transistors each having a gate, a source  
terminal, and a drain;

wherein the drains of the input pass transistors are coupled to the drains of the  
cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass  
transistors is coupled to an input, the sources of the cross-coupled latch amplifier NMOS transistors  
are coupled to the drain of the NMOS transistor coupled to a clock signal input, and the sources of  
the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an  
inverted clock signal input.

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(NEW) The data transfer arrangement in accordance with claim 1, wherein the  
output stage of the latching sense amplifier comprises:

a plurality of input transistors each having a gate, a source terminal, and a  
drain; and

a pair of cross-coupled PMOS transistors each having a gate, a source  
terminal, and a drain;

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a first PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of the first of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the first of the input transistors; and

a second PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of a second of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the second of the input transistors;

wherein the sources of the input transistors are coupled to a source of an NMOS transistor having a gate coupled to a clock signal input;

wherein the sources of the cross-coupled PMOS transistors are coupled to a voltage supply, the drains of the cross-coupled PMOS transistors are coupled to the drains of the input transistors; and

wherein the drains of the cross-coupled transistors provide a true and a complement phase of a data output signal.

9.3  
Cont

5 x (NEW) The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.

6 x (NEW) The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.

7 x (NEW) The data transfer arrangement in accordance with claim 3 } wherein the active pull up and pull down bus drivers are NMOS transistors.

8 x (NEW) A method of operation of a data transfer arrangement comprising:  
two bus drivers;  
a voltage precharge source;  
a differential bus coupled to the bus drivers and to the voltage precharge source; and

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a latching sense amplifier coupled to the differential bus;  
wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;  
wherein the output of the first stage is coupled to an input, and  
wherein the sense amplifier operates in two phases:

a precharge phase and a data transfer phase;

wherein the precharge phase operates when a control input clock signal is low, said phase comprising the steps of:

isolating the cross-coupled latch amplifier from a plurality of power buses by turning off an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to the inverted clock signal input;

passing a bus voltage swing to a plurality of internal nodes IT and IC of the latched amplifier;

precharging both dynamic gates to Vdd; and

providing a high true phase and a high complement phase of a data output signal; and

wherein the data transfer phase operates when a control input clock signal is high, said phase comprising the steps of:

isolating the internal nodes of the latched amplifier from the bus lines by turning off the pass input transistors;

connecting the cross-coupled latched amplifier to power buses by turning on an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to an inverted clock signal input;

amplifying each low voltage swing of the internal nodes to full logic levels;

discharging an output node of one of the dynamic gates to ground; and  
providing a low true phase and a low complement phase of the data

output signal.

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REMARKS

Upon entry of this Amendment, which amends claims 1 and 3, cancels claim 2, and adds claims 4-9, claims 1 and 3-9 remain pending.

Claims 1-3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. PAT. 5,598,371) in view of Hayakawa (U.S. PAT. 6,184,722 B1).

These rejections are respectfully traversed and reconsideration is respectfully requested on the grounds that the Examiner has not shown claim 1 would have been obvious in view of prior art.

With regard to Lee et al., it is respectfully submitted that Lee et al. teaches a data transfer arrangement comprising two bus drivers and a differential bus coupled to the bus drivers and to the voltage precharge source (PRECH), where the voltage precharge source (PRECH) is coupled to a supply voltage Vcc.

In contrast, the present invention teaches precharging the buses to a specific level between ground and Vdd ( $V_{pr} = K \cdot V_{dd}$ , where K is precharging voltage factor), as set out in the specification on page 4, lines 16-30. Precharging the buses to a specific level between ground and Vdd results in equal low differential voltage swings  $+dV, -V_d$ , providing increased speed of data transfer, high noise immunity due to the active mode and equal low output resistance of the driver in pull up and pull down modes, and low power consumption by the drivers during the cycle of operation.

Hayakawa teaches a latching sense amplifier coupled to the differential bus. Applicant respectfully submits that the circuit implementation of the latching sense amplifier in Hayakawa is different from the present embodiment.

The latch-type sense amplifier of the present invention has an output stage to avoid leakage currents and output glitches, which may appear because the potentials of nodes IT and IC are approximately equal to  $V_{pr}$  during the operating cycle of bus driver because the bus driver is precharged to a predetermined level between the ground and the supply voltage. Hayakawa does not teach a latching sense amplifier comprising two stages, where the input of the output stage is coupled to the output of the first stage.

The sources of cross-coupled latch amplifier NMOS transistors of the Hayakawa latch-type sense amplifier are coupled to the drains of the input pass transistors Q1 and Q2. In the present invention the sources of cross-coupled latch amplifier NMOS transistors are coupled to the drain of NMOS transistor N1, having a gate coupled to the clock signal input. The drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier MOS transistors and the input swing passes directly to the high-gain nodes IT and IC of the cross-coupled latched amplifier, providing a higher noise immunity than Hayakawa's.

In the present invention the sources of the PMOS transistors are coupled to the drain of a PMOS transistor having a gate coupled to the inverted clock input, whereas Hayakawa discloses a latch-type sense amplifier with the sources of the PMOS transistors coupled to the supply voltage.

Thus, it is respectfully submitted that none of the prior art, either alone or in combination, discloses, teaches or even suggests the latch-type sense amplifier disclosed in the present invention. Accordingly it is respectfully submitted that claim 1 is allowable.

Claims 3-8 depend, either directly or indirectly on claim 1 and, therefore, they are allowable for at least the reasons claim 1 is allowable. These claims further define and augment the features of applicant's invention.

New independent claim 9 was added. Claim 9 is directed to a method of operation of a data transfer arrangement. The support for claim 9 can be found in Specification on pages 2-5, lines 22-12. As discussed above none of the cited prior art references teach a data transfer arrangement as disclosed in the present invention, and, therefore claim 9 is allowable.

#### CONCLUSION:

Attached hereto is a marked-up version of the changes made to the claims by the current amendment along with a complete set of claims has been provided for convenience. The attached pages are captioned "Version With Markings To Show Changes Made" and "Claims Appendix."

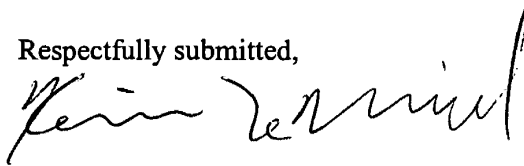
In view of the foregoing, applicant submits that this application is now in condition for allowance. The issuance of a formal notification to that effect at an early date is requested.

Andrew V. Podlesny et al.  
Application No.: 09/505,656  
Page 7

PATENT

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Kevin T. LeMond  
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SF 1237142 v3

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**Versions with Markings to Show Changes Made**

1. (AMENDED) A data transfer arrangement comprising:  
two bus drivers;  
a voltage precharge source;  
a differential bus coupled to the bus drivers and to the voltage precharge  
source; and  
  
a latching sense amplifier coupled to the differential bus;  
wherein the latching sense amplifier comprises:  
a first stage including a cross-coupled latch coupled to a differential  
data bus; and  
  
an output stage coupled to an output of said first stage;  
wherein the output of the first stage is coupled to an input of the output  
stage.
  
3. (AMENDED) The data transfer arrangement in accordance with claim 1  
wherein the bus drivers [**consist of**] comprise active pull-up and active pull-down bus drivers.

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Claims Appendix

1. (AMENDED) A data transfer arrangement comprising:
  - two bus drivers;
  - a voltage precharge source;
  - a differential bus coupled to the bus drivers and to the voltage precharge source; and
  - a latching sense amplifier coupled to the differential bus;wherein the latching sense amplifier comprises:
  - a first stage including a cross-coupled latch coupled to a differential data bus; and
  - an output stage coupled to an output of said first stage;wherein the output of the first stage is coupled to an input of the output stage.
2. (CANCELED)
3. (AMENDED) The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers.
4. (NEW) The data transfer arrangement in accordance with claim 1, wherein the first stage of the latching sense amplifier comprises:
  - a plurality of input pass transistors each having a gate, a source terminal, and a drain; and
  - a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain;wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass transistors is coupled to an input, the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input, and the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input.

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5. (NEW) The data transfer arrangement in accordance with claim 1, wherein the output stage of the latching sense amplifier comprises:

a plurality of input transistors each having a gate, a source terminal, and a drain; and

a pair of cross-coupled PMOS transistors each having a gate, a source terminal, and a drain;

a first PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of the first of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the first of the input transistors; and

a second PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of a second of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the second of the input transistors;

wherein the sources of the input transistors are coupled to a source of an NMOS transistor having a gate coupled to a clock signal input;

wherein the sources of the cross-coupled PMOS transistors are coupled to a voltage supply, the drains of the cross-coupled PMOS transistors are coupled to the drains of the input transistors; and

wherein the drains of the cross-coupled transistors provide a true and a complement phase of a data output signal.

6. (NEW) The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.

7. (NEW) The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.

8. (NEW) The data transfer arrangement in accordance with claim 3 wherein the active pull up and pull down bus drivers are NMOS transistors.

9. (NEW) A method of operation of a data transfer arrangement comprising:  
two bus drivers;  
a voltage precharge source;  
a differential bus coupled to the bus drivers and to the voltage precharge source; and  
a latching sense amplifier coupled to the differential bus;  
wherein the latching sense amplifier comprises:  
a first stage including a cross-coupled latch coupled to a differential data bus; and  
an output stage coupled to an output of said first stage;  
wherein the output of the first stage is coupled to an input, and  
wherein the sense amplifier operates in two phases:  
a precharge phase and a data transfer phase;  
wherein the precharge phase operates when a control input clock signal is low, said phase comprising the steps of:  
isolating the cross-coupled latch amplifier from a plurality of power buses by turning off an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to the inverted clock signal input;  
passing a bus voltage swing to a plurality of internal nodes IT and IC of the latched amplifier;  
precharging both dynamic gates to Vdd; and  
providing a high true phase and a high complement phase of a data output signal; and  
wherein the data transfer phase operates when a control input clock signal is high, said phase comprising the steps of:  
isolating the internal nodes of the latched amplifier from the bus lines by turning off the pass input transistors;

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connecting the cross-coupled latched amplifier to power buses by turning on an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to an inverted clock signal input;

amplifying each low voltage swing of the internal nodes to full logic levels;

discharging an output node of one of the dynamic gates to ground; and providing a low true phase and a low complement phase of the data output signal.

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PTO/SB/21 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

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# TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/505,656
Filing Date	June 27, 2000
First Named Inventor	Andrew V. Podlesny, et al.
Group Art Unit	2819
Examiner Name	Vibol Tan
Attorney Docket Number	020181000500

Total Number of Pages in This Submission 14

### ENCLOSURES (check all that apply)

<input checked="" type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers (for an Application)	<input type="checkbox"/> After Allowance Communication to Group
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input checked="" type="checkbox"/> Amendment / Response	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
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<input type="checkbox"/> Response to Missing Parts/ Incomplete Application	Remarks	The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430. <b>APPLICANTS HEREBY REQUEST A 2-MONTH EXTENSION OF TIME.</b>
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		

### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm and Individual name	Townsend and Townsend and Crew LLP Kevin T. LeMond	Reg No. 35,933
Signature		
Date	July 20, 2001	

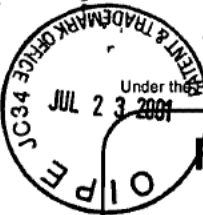
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# FEE TRANSMITTAL for FY 2001

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Application Number	09/505,856
Filing Date	June 27, 2000
First Named Inventor	Andrew V. Podlesny, et al.
Examiner Name	Vibol Tan
Group Art Unit	2819
Attorney Docket No.	020181-000500US

TOTAL AMOUNT OF PAYMENT (\$) 195.00

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ADDITIONAL FEES</b> <table border="1"> <thead> <tr> <th>Large Fee Code</th> <th>Entity Fee (\$)</th> <th>Small Fee Code</th> <th>Entity Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr><td>105</td><td>130</td><td>205</td><td>65</td><td>Surcharge - late filing fee or oath</td><td></td></tr> <tr><td>127</td><td>50</td><td>227</td><td>25</td><td>Surcharge - late provisional filing fee or cover sheet.</td><td></td></tr> <tr><td>139</td><td>130</td><td>139</td><td>130</td><td>Non-English specification</td><td></td></tr> <tr><td>147</td><td>2,520</td><td>147</td><td>2,520</td><td>For filing a request for reexamination</td><td></td></tr> <tr><td>112</td><td>920*</td><td>112</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td><td></td></tr> <tr><td>113</td><td>1,840*</td><td>113</td><td>1,840*</td><td>Requesting publication of SIR after Examiner action</td><td></td></tr> <tr><td>115</td><td>110</td><td>215</td><td>55</td><td>Extension for reply within first month</td><td></td></tr> <tr><td>116</td><td>390</td><td>216</td><td>195</td><td>Extension for reply within second month</td><td>195</td></tr> <tr><td>117</td><td>890</td><td>217</td><td>445</td><td>Extension for reply within third month</td><td></td></tr> <tr><td>118</td><td>1,390</td><td>218</td><td>695</td><td>Extension for reply within fourth month</td><td></td></tr> <tr><td>128</td><td>1,890</td><td>228</td><td>945</td><td>Extension for reply within fifth month</td><td></td></tr> <tr><td>119</td><td>310</td><td>219</td><td>155</td><td>Notice of Appeal</td><td></td></tr> <tr><td>120</td><td>310</td><td>220</td><td>155</td><td>Filing a brief in support of an appeal</td><td></td></tr> <tr><td>121</td><td>270</td><td>221</td><td>135</td><td>Request for oral hearing</td><td></td></tr> <tr><td>138</td><td>1,510</td><td>138</td><td>1,510</td><td>Petition to institute a public use proceeding</td><td></td></tr> <tr><td>140</td><td>110</td><td>240</td><td>55</td><td>Petition to revive - unavoidable</td><td></td></tr> <tr><td>141</td><td>1,240</td><td>241</td><td>620</td><td>Petition to revive - unintentional</td><td></td></tr> <tr><td>142</td><td>1,240</td><td>242</td><td>620</td><td>Utility issue fee (or reissue)</td><td></td></tr> <tr><td>143</td><td>440</td><td>243</td><td>220</td><td>Design issue fee</td><td></td></tr> <tr><td>144</td><td>600</td><td>244</td><td>300</td><td>Plant issue fee</td><td></td></tr> <tr><td>122</td><td>130</td><td>122</td><td>130</td><td>Petitions to the Commissioner</td><td></td></tr> <tr><td>123</td><td>50</td><td>123</td><td>50</td><td>Petitions related to provisional applications</td><td></td></tr> <tr><td>126</td><td>180</td><td>126</td><td>180</td><td>Submission of Information Disclosure Stmt</td><td></td></tr> <tr><td>581</td><td>40</td><td>581</td><td>40</td><td>Recording each patent assignment per property (times number of properties)</td><td></td></tr> <tr><td>146</td><td>710</td><td>246</td><td>355</td><td>Filing a submission after final rejection (37 CFR § 1.129(a))</td><td></td></tr> <tr><td>149</td><td>710</td><td>249</td><td>355</td><td>For each additional invention to be examined (37 CFR § 1.129(b))</td><td></td></tr> <tr><td>179</td><td>710</td><td>279</td><td>355</td><td>Request for Continued Examination (RCE)</td><td></td></tr> <tr><td>169</td><td>900</td><td>169</td><td>900</td><td>Request for expedited examination of a design application</td><td></td></tr> </tbody> </table>		Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	105	130	205	65	Surcharge - late filing fee or oath		127	50	227	25	Surcharge - late provisional filing fee or cover sheet.		139	130	139	130	Non-English specification		147	2,520	147	2,520	For filing a request for reexamination		112	920*	112	920*	Requesting publication of SIR prior to Examiner action		113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action		115	110	215	55	Extension for reply within first month		116	390	216	195	Extension for reply within second month	195	117	890	217	445	Extension for reply within third month		118	1,390	218	695	Extension for reply within fourth month		128	1,890	228	945	Extension for reply within fifth month		119	310	219	155	Notice of Appeal		120	310	220	155	Filing a brief in support of an appeal		121	270	221	135	Request for oral hearing		138	1,510	138	1,510	Petition to institute a public use proceeding		140	110	240	55	Petition to revive - unavoidable		141	1,240	241	620	Petition to revive - unintentional		142	1,240	242	620	Utility issue fee (or reissue)		143	440	243	220	Design issue fee		144	600	244	300	Plant issue fee		122	130	122	130	Petitions to the Commissioner		123	50	123	50	Petitions related to provisional applications		126	180	126	180	Submission of Information Disclosure Stmt		581	40	581	40	Recording each patent assignment per property (times number of properties)		146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))		149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))		179	710	279	355	Request for Continued Examination (RCE)		169	900	169	900	Request for expedited examination of a design application	
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149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))																																																																																																																																																																													
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<b>FEE CALCULATION</b> <b>1. BASIC FILING FEE</b> <table border="1"> <thead> <tr> <th>Large Fee Code</th> <th>Entity Fee (\$)</th> <th>Small Fee Code</th> <th>Entity Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr><td>101</td><td>710</td><td>201</td><td>355</td><td>Utility filing fee</td><td></td></tr> <tr><td>106</td><td>320</td><td>206</td><td>160</td><td>Design filing fee</td><td></td></tr> <tr><td>107</td><td>490</td><td>207</td><td>245</td><td>Plant filing fee</td><td></td></tr> <tr><td>108</td><td>710</td><td>208</td><td>355</td><td>Reissue filing fee</td><td></td></tr> <tr><td>114</td><td>150</td><td>214</td><td>75</td><td>Provisional filing fee</td><td></td></tr> </tbody> </table> SUBTOTAL (1) (\$)		Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	101	710	201	355	Utility filing fee		106	320	206	160	Design filing fee		107	490	207	245	Plant filing fee		108	710	208	355	Reissue filing fee		114	150	214	75	Provisional filing fee																																																																																																																																													
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		Other fee (specify) The Commissioner is authorized to charge any additional fees to the above noted Deposit Account. *Reduced by Basic Filing Fee Paid <b>SUBTOTAL (3) (\$)</b> 195																																																																																																																																																																															

SUBMITTED BY		Complete (if applicable)			
Name (Print/Type)	Kevin T. LeMond	Registration No. (Attorney/Agent)	35,933	Telephone	415-576-0200
Signature	<i>Kevin T. LeMond</i>	Date	July 20, 2001		

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231. SF 1249286 v1

A

I hereby certify that this correspondence is being sent by facsimile transmission to: **1 703 - 746-4043**  
Examiner Vibol Tan  
Patent & Trademark Office  
Washington, DC 20231

PATENT

**FAX RECEIVED**  
AUG 14 2001  
T.C. 2800

# 7/B  
K. Ranga  
8/16/01

On August 14, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: *Lata Olivier*  
Lata Olivier

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:  
**Andrew V. Podlesny et al.**  
**Application No.: 09/505,656**  
**Filed: June 27, 2000**  
**For: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME**

Examiner: Vibol Tan  
Art Unit: 2819  
SUPPLEMENTAL AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:  
In response to our telephone conversation of this morning attached is Supplemental Amendment to Claim 1.

IN THE CLAIMS:

*B*

- 1 1. (TWICE AMENDED) A data transfer arrangement comprising:
- 2 two bus drivers;
- 3 a voltage precharge source;
- 4 a differential bus coupled to the bus drivers and to the voltage precharge
- 5 source; and
- 6 a latching sense amplifier coupled to the differential bus;
- 7 wherein the latching sense amplifier comprises:
- 8 a first stage including a cross-coupled latch coupled to a differential
- 9 data bus; and

//

*B*

Andrew V. Podlesny et al.  
Application No.: 09/505,656  
Page 2

*Amended  
10/1*

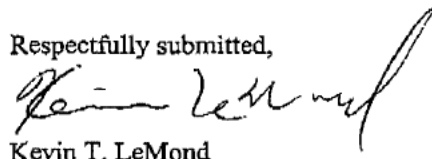
10 an output stage coupled to an output of said first stage;  
 11 wherein the output of the first stage is coupled to an input of the output  
 12 stage;  
 13 wherein the differential bus and the differential data bus are precharged to a  
 14 voltage  $V_{pr}$  between  $V_{dd}$  and ground, where  $V_{pr} = K \cdot V_{dd}$ , and  $K$  is a precharging voltage factor.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Kevin T. LeMond  
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8<sup>th</sup> Floor  
San Francisco, California 94111-3834  
Tel: (415) 576-0200  
Fax: (415) 576-0300  
KTL:lo  
SF 1258563 v1

*12*

*9*

Andrew V. Podlesny et al.  
Application No.: 09/505,656  
Page 3

Version With Markings To Show Changes Made

IN THE CLAIMS:

- 1                   1.   (TWICE AMENDED) A data transfer arrangement comprising:
- 2                           two bus drivers;
- 3                           a voltage precharge source;
- 4                           a differential bus coupled to the bus drivers and to the voltage precharge
- 5 source; and
- 6                           a latching sense amplifier coupled to the differential bus;
- 7                           wherein the latching sense amplifier comprises:
- 8                                   a first stage including a cross-coupled latch coupled to a differential
- 9 data bus; and
- 10                                   an output stage coupled to an output of said first stage;
- 11                                   wherein the output of the first stage is coupled to an input of the output
- 12 stage[.];
- 13                                   wherein the differential bus and the differential data bus are precharged to a
- 14 voltage  $V_{pr}$  between  $V_{dd}$  and ground, where  $V_{pr} = K * V_{dd}$ , and  $K$  is a precharging voltage factor.

B

Atty Docket No. 020181-000400

PTO FAX NO.: 1 703- 746-4043

ATTENTION: Examiner Vibol Tan  
Group Art Unit 2819

**OFFICIAL COMMUNICATION**  
**FOR THE PERSONAL ATTENTION OF**  
**EXAMINER Vibol Tan**

**CERTIFICATION OF FACSIMILE TRANSMISSION**

I hereby certify that the following documents, in re Application of Podlesney et al., Application No. 09/505,656, filed June 27, 2000, for HIGH SPEED LOW POWER DATA TRANSFER SCHEME is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Documents Attached

- 1. SUPPLEMENTAL AMENDMENT TO CLAIM 1

Number of pages being transmitted, including this page: 3

Dated: August 14, 2001

  
\_\_\_\_\_  
Lata Olivier

*PLEASE CONFIRM RECEIPT OF THIS PAPER BY  
RETURN FACSIMILE AT (415) 576-0300*

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8th Floor  
San Francisco, CA 94111-3834  
Telephone: (415) 576-0200  
Fax: (415) 576-0300  
SF 1258556 v1





UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

**NOTICE OF ALLOWANCE AND ISSUE FEE DUE**

020350 MN91/0817  
TOWNSEND AND TOWNSEND AND CREW  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO CA 94111-3834

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/505,656	02/17/00	008	TAN, V	2819 08/17/01
First Named Applicant	PODLESNY,		35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION HIGH SPEED LOW POWER DATA TRANSFER SCHEME

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 20181-5US	326-095.000	K75	UTILITY	YES	\$620.00	11/19/01

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.**

**THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.**

**HOW TO RESPOND TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.  
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

If the SMALL ENTITY is shown as NO:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- B. If the status is the same, pay the FEE DUE shown above.

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.  
Please direct all communications prior to issuance to Box ISSUE FEE-unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

PATENT AND TRADEMARK OFFICE COPY





**UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

*M*

*Ma*

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/505,656	02/17/00	PODLESNY	A 20181-5US

020350 MM91/0817  
TOWNSEND AND TOWNSEND AND CREW  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO CA 94111-3834

EXAMINER

TAN, V

ART UNIT	PAPER NUMBER
2819	

2819

DATE MAILED: 08/17/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/505,656	PODLESNY ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vibol Tan	2819	

**- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to the supplemental amendment filed 08/14/2001.
2.  The allowed claim(s) is/are 1 and 3-9.
3.  The drawings filed on \_\_\_\_\_ are accepted by the Examiner.
4.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All    b)  Some\*    c)  None    of the:
    1.  Certified copies of the priority documents have been received.
    2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.
5.  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
  - (a)  The translation of the foreign language provisional application has been received.
6.  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8.  CORRECTED DRAWINGS must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
    - 1)  hereto or 2)  to Paper No. \_\_\_\_\_.
  - (b)  including changes required by the proposed drawing correction filed \_\_\_\_\_, which has been approved by the Examiner.
  - (c)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |                                                                                                        |                                                                                     |
|--------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1 <input type="checkbox"/> Notice of References Cited (PTO-892)                                        | 2 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)          |
| 3 <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                    | 4 <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____             |
| 5 <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449), Paper No. <u>5</u> | 6 <input type="checkbox"/> Examiner's Amendment/Comment                             |
| 7 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8 <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
|                                                                                                        | 9 <input type="checkbox"/> Other                                                    |

**DETAILED ACTION**

1. The application having been allowed, formal drawings are required in response to this Office Action.
2. The following is an examiner's statement of reasons for allowance: applicants' arguments have been fully considered and deemed to be persuasive. The present invention teaches precharging the buses to a specific level between ground and Vdd, which results in equal low differential voltage swings, providing increased speed of data transfer. The prior art of Lee et al. does not teach such precharging buses as described above.
3. Claims 1 and 3-9 are allowed. Applicants have canceled claim 2.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-3432 for After Final communications.

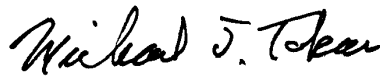
Application/Control Number: 09/505,656  
Art Unit: 2819

Page 3

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

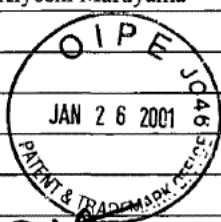
Vibol Tan

Patent Examiner, AU 2819



Michael Tokar  
Supervisory Patent Examiner  
Technology Center 2800

FORM PTO-1449 (Modified)		Attorney Docket No.: 20181-000500US		Application No.: 09/505,656		
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant: Andrew V. Podlesny et al.				
		Filing Date: February 17, 2000		Group: 2819		
Reference Designation			U.S. PATENT DOCUMENTS			Page 1
Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
<i>Jan</i> A	Article "On the Parallel Evaluation of Polynomials" in IEEE Transactions On Computer, Vol. C-22, No. 1, January 1973 by Kiyoshi Maruyama					
_____ B						
_____ C						
_____ D						
_____ E						
EXAMINER	<i>[Signature]</i>		DATE CONSIDERED	8/9/01		



EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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 FEB 22 2001  
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Form PTO 948 (Rev. 03/01)

U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office

Application No.

09/505656

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 2/17/00

A. [ ] approved by the Draftsperson under 37 CFR 1.84 or 1.152.
B. [X] objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color.
Color drawings are not acceptable until petition is granted. Fig(s)
Pencil and non black ink not permitted. Fig(s)
2. PHOTOGRAPHS. 37 CFR 1.84(b)
Full-tone sets required. Fig(s)
Photographs may not be mounted. 37 CFR 1.84(e)
Poor quality (half-tone). Fig(s)
3. TYPE OF PAPER. 37 CFR 1.84(e)
Paper not flexible, strong, white, and durable. Fig(s)
Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s)
Mylar, velum paper is not acceptable (too thin). Fig(s)
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
21.0 cm by 29.7 cm (DIN size A4)
21.6 cm by 27.9 cm (8 1/2 x 11 inches)
All drawing sheets not the same size. Sheet(s)
Drawings sheets not an acceptable size. Fig(s)
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
SIZE: A4 Size
Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: 8 1/2 x 11
Margins not acceptable. Fig(s)
Top (T) Left (L) Right (R) Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
REMINDER: Specification may require revision to correspond to drawing changes.
Partial views. 37 CFR 1.84(h)(2)
Brackets needed to show figure as one entity. Fig(s)
Views not labeled separately or properly. Fig(s)
Enlarged view not labeled separately or properly. Fig(s)
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
Hatching not indicated for sectional portions of an object. Fig(s)
Sectional designation should be noted with Arabic or Roman numbers. Fig(s)
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s)
9. SCALE. 37 CFR 1.84(k)
Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s)
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s)
11. SHADING. 37 CFR 1.84(m)
Solid black areas pale. Fig(s)
Solid black shading not permitted. Fig(s)
Shade lines, pale, rough and blurred. Fig(s)
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
Numbers and reference characters not plain and legible. Fig(s)
Figure legends are poor. Fig(s)
Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s)
English alphabet not used. 37 CFR 1.84(p)(2) Fig(s)
Numbers, letters and reference characters must be at least 32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s)
13. LEAD LINES. 37 CFR 1.84(q)
Lead lines cross each other. Fig(s)
Lead lines missing. Fig(s)
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s)
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s)
16. CORRECTIONS. 37 CFR 1.84(w)
Corrections not made from prior PTO-948 dated
17. DESIGN DRAWINGS. 37 CFR 1.152
Surface shading shown not appropriate. Fig(s)
Solid black shading not used for color contrast. Fig(s)

COMMENTS

REVIEWER

77

DATE

8/15/07

TELEPHONE NO.

308-0011

ATTACHMENT TO PAPER NO.

**Attachment for PTO-948 (Rev. 03/01, or earlier)**  
**6/18/01**

**The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.**

**INFORMATION ON HOW TO EFFECT DRAWING CHANGES**

**1. Correction of Informalities – 37 CFR 1.85**

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may **NOT** be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

**2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.**

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

**Timing of Corrections**

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.

06/01/01

PART B—ISSUE FEE TRANSMITTAL

*158/m*

Complete this form, together with applicable fees, to: **Box ISSUE FEE**  
**Assistant Commissioner for Patents**  
**Washington, D.C. 20231**



**MAILING INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, Patent, maintenance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

**Certificate of Mailing**

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

**Donald Nixon** (Depositor's name)

*Donald Nixon* (Signature)

**November 6, 2001** (Date)

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

020350 MM91/0817  
 TOWNSEND AND TOWNSEND AND CREW  
 TWO EMBARCADERO CENTER  
 EIGHTH FLOOR  
 SAN FRANCISCO CA 94111-3834

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/505,656	02/17/00	008	TAN, V	2819 08/17/01
First Named Applicant	PODLESNY,		35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: **HIGH SPEED LOW POWER DATA TRANSFER SCHEME**

ATTYS DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3	20181-5US	326-095.000	K75	UTILITY	YES \$640.00	11/19/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.
- Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

**Townsend and Townsend and Crew LLP**

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)  
 PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.
- (A) NAME OF ASSIGNEE: **Elbrus International Limited**
- (B) RESIDENCE: (CITY & STATE OR COUNTRY) **George Town Grand Cayman, Grand Cayman Islands**
- Please check the appropriate assignee category indicated below (will not be printed on the patent)
- Individual  corporation or other private group entity  government

- 4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
- Issue Fee
- Advance Order - # of Copies \_\_\_\_\_

- 4b. The following fees or deficiency in these fees should be charged to:
- DEPOSIT ACCOUNT NUMBER **20-1430**  
 (ENCLOSE AN EXTRA COPY OF THIS FORM)
- Issue Fee **11**
- Advance Order - # of Copies \_\_\_\_\_

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) *Kevin T. LeHond* Reg. No. 933 (Date) **11/06/01**

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

**Burden Hour Statement:** This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

02/05/2002 EAREGAY2 00000153 201430 09505656  
 01 FC:242 640.00 CH  
 02 FC:561 33.00 CH

TRANSMIT THIS FORM WITH FEE



2-1-2

PTO UTILITY GRANT  
Paper Number 6

**The Commissioner of Patents  
and Trademarks**

*Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.*

Therefore, this

**United States Patent**

*Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.*

*If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.*

*If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to a statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.*

*Bruce Lehman*  
Commissioner of Patents and Trademarks

Attest *Mary J. Quinn*

The  
United  
States  
of  
America



Form PTD-1584 (Rev. 2/97)

(RIGHT INSIDE)

FR-10M

Best Available Copy

I hereby certify that correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

PATENT  
Attorney Docket No.: 020181-000500US

Box Issue Fee  
Assistant Commissioner for Patents  
Washington, D.C. 20231

#9 2001

On November 6, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Donald M. ...

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Andrew V. Podlesny et al.

Application No.: 09/505,656

Filed: February 17, 2000

For: HIGH SPEED LOW POWER  
DATA TRANSFER SCHEME

Examiner: E. Peavey

Art Unit: 3626

TRANSMITTAL OF FORMAL  
DRAWINGS

Box Issue Fee  
Assistant Commissioner for Patents  
Washington, D.C. 20231

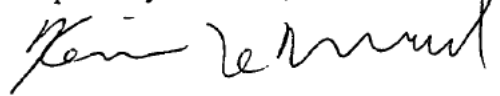
Attn: Official Draftsman

Sir:

Applicant submits herewith a set of corrected drawings in connection with the above captioned application. The new drawings includes the changes required by the Examiner in form of the Examiner's Comment which was issued in conjunction with the Notice of Allowance and Issue Fee dated August 17, 2001.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Kevin T. LeMond  
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8<sup>th</sup> Floor  
San Francisco, California 94111-3834  
Tel: (415) 576-0200  
Fax: (415) 576-0300  
KTL/dxm  
SF 128079 v1

8/6

6366130

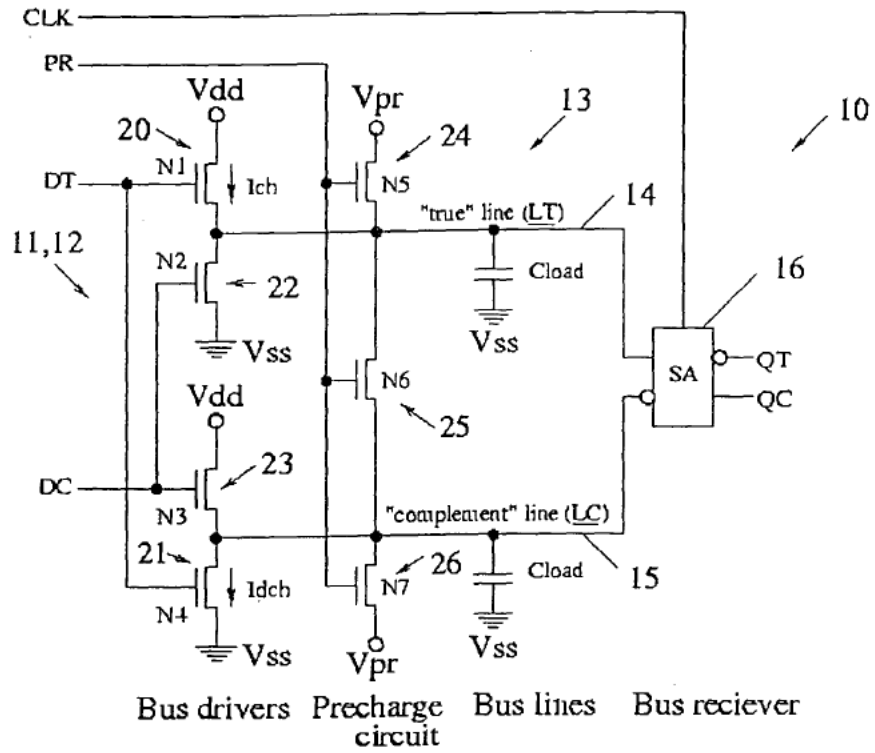
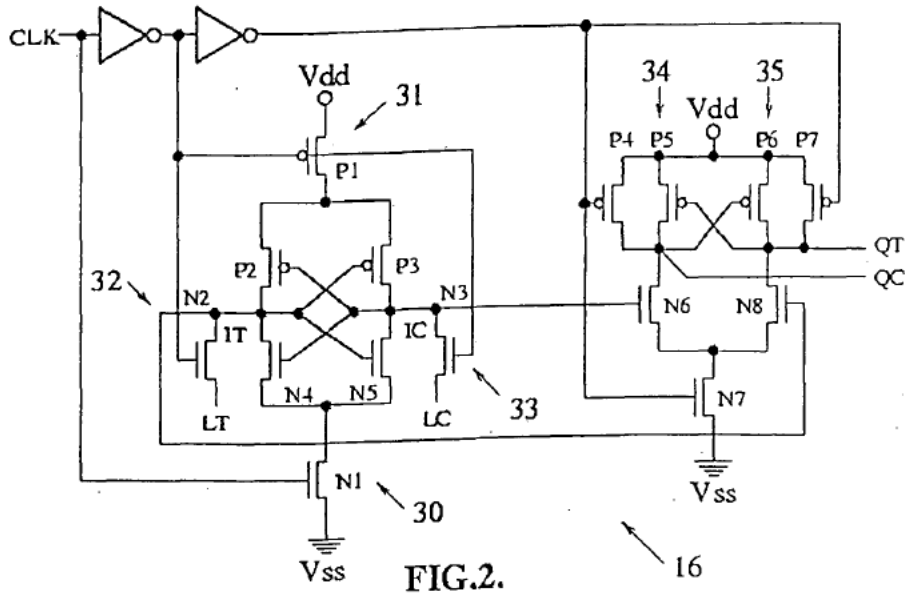


FIG. 1.



I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11

PATENT  
Docket No.: 020181-000500US

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julia Taylor Clough

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Andrew V. Podlesny, et al.

Patent No.: 6,366,130

Issued: April 2, 2002

Application No.: 09/505,656

Filed: February 17, 2000

For: HIGH SPEED LOW POWER  
DATA TRANSFER SCHEME

Customer No.: 20350

Confirmation No.:

Examiner:

Art Unit:

CORRECTION OF ENTITY  
STATUS AND PAYMENT OF  
DEFICIENCY OWED UNDER 37  
CFR §§ 1.27(g) and 1.28(c)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

The following submission of deficiency payment and itemization is believed to meet the requirements of 37 C.F.R. §§ 1.28(c)(1) and (c)(2). Furthermore, Applicants understand that under 37 CFR § 1.28(d) this submission is treated under § 1.27(g)(2) as a notification of loss of entitlement to small entity status. Therefore, Applicants respectfully request the deficiency payment be processed and the correct entity status be accorded to the application.


ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

DATE OF PAYMENT	TYPE OF FEE	SMALL ENTITY FEE ACTUALLY PAID	(CURRENT) LARGE ENTITY FEE FOR ACTION	DEFICIENCY PAYMENT OWED
June 22, 2000	Filing	\$345	\$850	\$505
June 22, 2000	Missing Parts Surcharge	\$65	\$130	\$65
November 6, 2001	Issue Fee	\$640	\$1510	\$870
October 3, 2005	4 <sup>th</sup> Maintenance Fee	\$450	\$980	\$530
September 22, 2009	8 <sup>th</sup> Maintenance Fee	\$1240	\$2480	\$1240
				<b>Total \$3210</b>

**TOTAL DEFICIENCY PAYMENT OWED: \$3210**

Applicant hereby authorizes the Commissioner to deduct the total deficiency owed of \$3210 from Deposit Account No. 20-1430. Please deduct any additional fees due from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

  
J. Georg Seka  
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, Eighth Floor  
San Francisco, California 94111-3834  
Tel: (415) 576-0200  
Fax: (415) 576-0300  
JGS:jtc  
63318995 v1

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	10032923
<b>Application Number:</b>	09505656
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	7462
<b>Title of Invention:</b>	High speed low power data transfer scheme
<b>First Named Inventor/Applicant Name:</b>	Andrew V. Podlesny
<b>Customer Number:</b>	20350
<b>Filer:</b>	J. Georg Seka/Julie Clough
<b>Filer Authorized By:</b>	J. Georg Seka
<b>Attorney Docket Number:</b>	20181-5US
<b>Receipt Date:</b>	05-MAY-2011
<b>Filing Date:</b>	17-FEB-2000
<b>Time Stamp:</b>	19:02:19
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Entity_020181_005000US.pdf	68881 60745883f62fa9632990d7e6fdf029592bbd c8aa	no	2

### Warnings:

### Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



#10

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11

PATENT  
Docket No.: 020181-000500US

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julia Taylor Clough

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Andrew V. Podlesny, et al.

Patent No.: 6,366,130

Issued: April 2, 2002

Application No.: 09/505,656

Filed: February 17, 2000

For: HIGH SPEED LOW POWER  
DATA TRANSFER SCHEME

Customer No.: 20350

Confirmation No.:

Examiner:

Art Unit:

CORRECTION OF ENTITY  
STATUS AND PAYMENT OF  
DEFICIENCY OWED UNDER 37  
CFR §§ 1.27(g) and 1.28(c)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

The following submission of deficiency payment and itemization is believed to meet the requirements of 37 C.F.R. §§ 1.28(c)(1) and (c)(2). Furthermore, Applicants understand that under 37 CFR § 1.28(d) this submission is treated under § 1.27(g)(2) as a notification of loss of entitlement to small entity status. Therefore, Applicants respectfully request the deficiency payment be processed and the correct entity status be accorded to the application.


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				<b>Total \$3210</b>

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Respectfully submitted,

  
J. Georg Seka  
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, Eighth Floor  
San Francisco, California 94111-3834  
Tel: (415) 576-0200  
Fax: (415) 576-0300  
JGS:jtc  
63318995 v1

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	10032923
<b>Application Number:</b>	09505656
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	7462
<b>Title of Invention:</b>	High speed low power data transfer scheme
<b>First Named Inventor/Applicant Name:</b>	Andrew V. Podlesny
<b>Customer Number:</b>	20350
<b>Filer:</b>	J. Georg Seka/Julie Clough
<b>Filer Authorized By:</b>	J. Georg Seka
<b>Attorney Docket Number:</b>	20181-5US
<b>Receipt Date:</b>	05-MAY-2011
<b>Filing Date:</b>	17-FEB-2000
<b>Time Stamp:</b>	19:02:19
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Entity_020181_005000US.pdf	68881 <small>60745883162fa9632990d7e6fd029592bbd c30a</small>	no	2

**Warnings:**

**Information:**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11

PATENT  
Docket No.: 020181-000500US

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julie Taylor Clough

05/16/2011 DALLEN 00000005 201430 09505656  
01 FC:1461 1440.00 DA

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2011 MAY -9 PM 4: 20

USPTO  
COMMUNICATIONS SECTION

In re application of:  
Andrew V. Podlesny, et al.  
Patent No.: 6,366,130  
Issued: April 2, 2002  
Application No.: 09/505,656  
Filed: February 17, 2000  
For: HIGH SPEED LOW POWER  
DATA TRANSFER SCHEME  
Customer No.: 20350

Confirmation No.:  
Examiner:  
Art Unit:  
CORRECTION OF ENTITY  
STATUS AND PAYMENT OF  
DEFICIENCY OWED UNDER 37  
CFR §§ 1.27(g) and 1.28(c)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

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05/16/2011 DALLEN 00000006 201430 6366130  
01 FC:1599 1770.00 DA


ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

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				<b>Total \$3210</b>

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Respectfully submitted,

  
J. Georg Seka  
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, Eighth Floor  
San Francisco, California 94111-3834  
Tel: (415) 576-0200  
Fax: (415) 576-0300  
JGS:jtc  
63318995 v1

#11

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PATENT  
Docket No.: 020181-000500US

KILPATRICK TOWNSEND & STOCKTON LLP

05/16/2011 DALLEN 00000005 201430 09505656  
01 FC:1461 1440.00 DA

By: Julia Taylor Clough

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2011 MAY -9 PM 4:20  
USPTO  
RECEIVED

In re application of:  
Andrew V. Podlesny, et al.  
Patent No.: 6,366,130  
Issued: April 2, 2002  
Application No.: 09/505,656  
Filed: February 17, 2000  
For: HIGH SPEED LOW POWER  
DATA TRANSFER SCHEME  
Customer No.: 20350

Confirmation No.:  
Examiner:  
Art Unit:  
CORRECTION OF ENTITY  
STATUS AND PAYMENT OF  
DEFICIENCY OWED UNDER 37  
CFR §§ 1.27(g) and 1.28(c)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

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05/16/2011 DALLEN 00000006 201430 6366130  
01 FC:1599 1770.00 DA

Adjustment date: 06/10/2011 CKHLOK  
05/16/2011 DALLEN 00000006 201430 6366130  
01 FC:1599 1770.00 CR

06/10/2011 CKHLOK 00000019 201430 6366130  
01 FC:1559 1770.00 DA


ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

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Respectfully submitted,

  
J. Georg Seka  
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP  
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SAN FRANCISCO, CA 94111-3834

**MAILED**  
**JUN 13 2011**  
**OFFICE OF PETITIONS**

In re Patent of Podlesny et al. :  
Patent No. 6,366,130 :  
Issue Date: April 2, 2002 :  
Application No. 09/505,656 :  
Filing Date: February 17, 2000 :  
Attorney Docket No. 020181-000500US :

Letter

This is a notice regarding the request for acceptance of a fee deficiency submission under 37 CFR 1.28(c) filed May 5, 2011.<sup>1</sup>

The deficiency payment of \$3,210 is hereby accepted.

The change of status to large entity has been entered and made of record.

Telephone inquiries regarding this communication should be directed to Petitions Attorney Steven Brantley at (571) 272-3203.

Charles Steven Brantley  
Senior Petitions Attorney  
Office of Petitions

<sup>1</sup> The Office notes a duplicate copy of the request was filed on May 9, 2011.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
www.uspto.gov

Patent No. 6366130

**NOTICE OF *INTER PARTES* REEXAMINATION**

Notice is hereby given that a request for *inter partes* reexamination of U.S. Patent No. 6366130 was filed on 1-19-12 under 35 U.S.C. § 311 and 37 C.F.R. § 1.913.

The reexamination proceeding has been assigned Control No. 95/ 000657.

This Notice incorporates by reference into the patent file, all papers entered into the reexamination file.

**Note: This Notice should be entered into the patent file.**

Patent

<p><b>TO:</b></p> <p style="text-align: center;">COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450</p>	<p style="text-align: center;"><b>REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT</b></p>
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In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

<b>DOCKET</b> 11-cv-04356	<b>DATE FILED</b> 06/27/2011	<b>UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION</b>
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<b>PLAINTIFF</b> Cascades Computer Innovation, LLC	<b>DEFENDANT</b> Hynix Semiconductor, Inc, et al
-------------------------------------------------------	-----------------------------------------------------

PATENT NO.	DATE OF PATENT	PATENTEE
6,366,130	April 2, 2002	High Speed Low Power Data Transfer Scheme

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY	
	<input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

<p>DECISION/JUDGMENT</p>		
<p>CLERK Michael W. Dobbins</p>	<p>(BY) DEPUTY CLERK <i>Haydee Pawlowski</i> Haydee Pawlowski</p>	<p>DATE June 29, 2011</p>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

POWER OF ATTORNEY PATENT REEXAMINATION AND CHANGE OF  
CORRESPONDENCE ADDRESS

The undersigned patent owner hereby appoints: Clifford H. Kraft, attorney registered with the United States Patent and Trademark Office hold registration number 35,229 to represent it in all transactions involving Reexamination number 95/000,657 of United States Patent number 6,366,130 entitled:

**"High Speed Low Power Data Transfer Scheme"**

All prior powers of attorneys and appointments are hereby revoked.

The Correspondence Address for all correspondence in this case should be sent to:

Clifford H. Kraft  
320 Robin Hill Dr.  
Naperville IL. 60540

CUSTOMER NUMBER: 74642

Telephone: 708 528-9092

ELBRUS INTERNATIONAL LIMITED

BY:

Signed: *[Signature]* Date: 04/06/2012  
Name: Leonid N. Nazarov Title: Manager



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 7462

<b>SERIAL NUMBER</b> 09/505,656	<b>FILING OR 371(c) DATE</b> 02/17/2000 <b>RULE</b>	<b>CLASS</b> 326	<b>GROUP ART UNIT</b> 2819	<b>ATTORNEY DOCKET NO.</b> 20181-5US
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**APPLICANTS**  
 Andrew V. Podlesny, Moscow, RUSSIAN FEDERATION;  
 Alexander V. Malshin, Moscow, RUSSIAN FEDERATION;  
 Alexander Y. Solomatnikov, Moscow, RUSSIAN FEDERATION;

**\*\* CONTINUING DATA \*\*\*\*\***  
 This appln claims benefit of 60/120,531 02/17/1999

**\*\* FOREIGN APPLICATIONS \*\*\*\*\***

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED**  
**\*\* 04/26/2000**

Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no	<b>STATE OR COUNTRY</b> RUSSIAN FEDERATION	<b>SHEETS DRAWING</b> 1	<b>TOTAL CLAIMS</b> 3	<b>INDEPENDENT CLAIMS</b> 1	
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance					
Verified and Acknowledged	Examiner's Signature _____	Initials _____			

**ADDRESS**  
74642

**TITLE**  
High speed low power data transfer scheme

<b>FILING FEE RECEIVED</b> 410	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees ( Filing ) <input type="checkbox"/> 1.17 Fees ( Processing Ext. of time ) <input type="checkbox"/> 1.18 Fees ( Issue ) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit
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UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

**CONFIRMATION NO. 7462**

**POWER OF ATTORNEY NOTICE**

20350  
KILPATRICK TOWNSEND & STOCKTON LLP  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO, CA 94111-3834



Date Mailed: 04/10/2012

**NOTICE REGARDING CHANGE OF POWER OF ATTORNEY**

This is in response to the Power of Attorney filed 04/06/2012.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/rbell/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

**CONFIRMATION NO. 7462**

**POA ACCEPTANCE LETTER**

74642  
CLIFFORD H. KRAFT  
320 ROBIN HILL DR.  
NAPERVILLE, IL 60540



Date Mailed: 04/10/2012

**NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY**

This is in response to the Power of Attorney filed 04/06/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/rbell/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

AO 121 (6/90)

<b>TO:</b>	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

<b>DOCKET</b> 14 cv 5691	<b>DATE FILED</b> 7/24/14	<b>UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION</b>
<b>PLAINTIFF</b> Cascades Computer Innovation, LLC		<b>DEFENDANT</b> Samsung Electronics Co., Ltd.
<b>PATENT NO.</b>	<b>DATE OF PATENT</b>	<b>PATENTEE</b>
6,366,130 B1	4/2/2002	Elbrus International Limited

In the above-entitled case, the following patent(s) have been included:

<b>DATE INCLUDED</b>	<b>INCLUDED BY</b> <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading			
<b>PATENT NO.</b>	<b>DATE OF PATENT</b>	<b>PATENT</b>		

In the above-entitled case, the following decision has been rendered or judgment issued:

<b>DECISION/JUDGMENT</b>		
<b>CLERK</b> Thomas G. Bruton	<b>(BY) DEPUTY CLERK</b> Marlan Cowan	<b>DATE</b> 8/12/14



AO 121 (6/90)

<b>TO:</b>  COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	<b>REPORT ON THE                  FILING OF DETERMINATION OF AN ACTION OR APPEAL                  REGARDING A COPYRIGHT</b>
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In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

<b>DOCKET</b> 14 cv 5691	<b>DATE FILED</b> 7/24/14	<b>UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION</b>
<b>PLAINTIFF</b> Cascades Computer Innovation, LLC		<b>DEFENDANT</b> Samsung Electronics Co., Ltd.
<b>PATENT NO.</b>	<b>DATE OF PATENT</b>	<b>PATENTEE</b>
6,366,130 B1	4/2/2002	Elbrus International Limited

In the above-entitled case, the following patent(s) have been included:

<b>DATE INCLUDED</b>	<b>INCLUDED BY</b> <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading		
<b>PATENT NO.</b>	<b>DATE OF PATENT</b>	<b>PATENT</b>	

In the above-entitled case, the following decision has been rendered or judgment issued:

<b>DECISION/JUDGMENT</b>		
<b>CLERK</b> Thomas G. Bruton	<b>(BY) DEPUTY CLERK</b> Marlan Cowan 	<b>DATE</b> 8/12/14