Filed on behalf of: Samsung Electronics Co., Ltd.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

ELBRUS INTERNATIONAL LIMITED
Patent Owner

U.S. Patent No. 6,366,130

DECLARATION OF DR. R. JACOB BAKER

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I, R. Jacob Baker, declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. ("Petitioner") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office. Although I am being compensated at my rate of $450 per hour for the time I spend on this matter, no part of my compensation is dependent on the outcome of this proceeding, and I have no other interest in this proceeding.

2. I understand that this proceeding involves U.S. Patent No. 6,366,130 ("the '130 Patent") (Ex. 1001), the application for which was filed on February 17, 2000, as U.S. Patent Application No. 09/505,656, and issued on April 2, 2002. I also understand, as demonstrated by the face of the '130 Patent, that the '130 Patent purports to claim priority to February 17, 1999, the filing date of U.S. Provisional Application No. 60/120,531 ("the '531 provisional application").

3. I have been asked to consider whether certain references disclose or suggest the features recited in the claims of the '130 Patent. My opinions are set forth below.

II. QUALIFICATIONS

4. I serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas ("UNLV"). I have been teaching electrical

engineering at UNLV since 2012. Before this, I was a Professor of Electrical and Computer Engineering with Boise State University beginning in 2000. Before my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and an Assistant Professor of Electrical Engineering between 1993 and 1998, both at the University of Idaho. I have been teaching electrical engineering since 1991. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

5. As further described in my CV, I am a licensed Professional Engineer in the State of Idaho and have more than 25 years of experience, including extensive experience in circuit design and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips and CMOS Image Sensors (CISs) at Micron in Boise, Idaho. I also spent considerable time working on the development of Flash memory while at Micron. My efforts resulted in more than a dozen Flash-memory related patents. Among many other experiences, I led the development of the delay-locked loop (DLL) in the late 1990s so that Micron DRAM products could transition to the DDR memory standard. I also provided technical assistance with Micron's acquisition of Photobit during 2001 and 2002. This assistance included help transitioning the manufacture of CIS products into Micron's DRAM process technology. I have worked as a

consultant at other companies designing memory chips, including Sun, Oracle, and Contour Semiconductor. I have worked at other companies designing CISs, including Aerius Photonics, Lockheed-Martin, and OmniVision.

6. I am the author of several books covering the area of integrated circuit design including: *DRAM Circuit Design: Fundamental and High-Speed Topics* (two editions), *CMOS Circuit Design, Layout, and Simulation* (three editions), and *CMOS Mixed-Signal Circuit Design* (two editions). I have authored, and/or co-authored, more than 100 papers and presentations in the areas of solid-state circuit design and packaging.

7. As a professor, I have been the main advisor to five Doctoral students and over 65 Masters students.

8. I am the named inventor on over 137 granted U.S. patents in integrated circuit design including flash memory, DRAM, and CMOS image sensors.

9. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

10. I have also received the IEEE Circuits and Systems Education Award (2011), the IEEE Power Electronics Best Paper Award (2000), and I am a Fellow of the IEEE for contributions to memory circuit design.

11. In addition, I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award the three years I have been at UNLV.

12. I have also given over 50 invited talks at conferences and universities in the areas of integrated circuit design including: AMD, Arizona State University, Beijing Jiaotong University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), École Polytechnique de Montréal, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey, ITESM (Mexico), Iowa State University, Laval University, Lehigh University, Princeton University, Temple University, University of Alabama, University of Arkansas, University of Buenos Aires (Argentina), University of Illinois, Urbana-Champaign, Utah State University, University of Nevada, Las Vegas, University of Houston, University of Idaho, University of Nevada, Reno, University of Macau, University

of Toronto, University of Utah, Yonsei University (Seoul, Korea), University of Maryland, IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), the Franklin Institute, National Semiconductor, AMI semiconductor, Micron Technology, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Tower (Israel), Foveon, ICySSS keynote, and Xilinx.

13. Details of my professional and educational background, as well as a listing of other matters on which I have provided consulting and/or provided testimony as a technical expert, are provided in my Curriculum Vitae, attached as Appendix A to this Declaration.

III. SUMMARY OF OPINIONS

14. All of the opinions contained in this Declaration are based on the documents I reviewed, my experience and background, and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, I reviewed the ’130 Patent (Ex. 1001); the prosecution file history for the ’130 Patent (Ex. 1003); the file history of the *inter partes* reexamination (control no. 95/000,657) (“the ’657 proceeding”) for the ’130 Patent, excerpts of which I understand are being submitted as Ex. 1004; U.S. Patent No. 5,828,241 to Sukegawa (“*Sukegawa*”) (Ex. 1005); U.S. Patent No. 6,249,469 to Hardee

("*Hardee*") (Ex. 1007); U.S. Patent No. 6,108,254 to Watanabe et al. ("*Watanabe*") (Ex. 1006); "Half-VDD Bit-Line Sensing Scheme in CMOS DRAM's," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4, August 1984 by Nicky Chau-Chun Lu et al. ("*Lu*") (Ex. 1008); and excerpts from the Modern Dictionary of Electronics (7th ed. 1999) (Ex. 1009), while drawing on my experience and knowledge in the field.

15. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '130 Patent at the time of the alleged invention, which I have been asked to initially assume is February 17, 1999, the filing date of the '531 provisional application from which the '130 Patent purports to claim priority. At the time of the alleged invention, a person of ordinary skill in the art related to the technology of the '130 Patent would have had an undergraduate degree in Electrical Engineering or equivalent and at least two to three years of experience in the design and/or analysis of data transfer circuits or the equivalent. In determining the level of ordinary skill, I was asked to consider, for example, the types of problems encountered in the art, prior solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

16. Based on my experience and expertise, it is my opinion that certain references disclose or suggest all the features recited in claims 1-3, 5-7, and 9 ("the challenged claims") of the '130 Patent.

IV. THE '130 PATENT

17. The '130 Patent is purportedly directed to a data transfer scheme that includes two bus drivers, a precharge circuit, two complementary bus lines, and a latching sense amplifier. *See, e.g.*, Ex. 1001 2:1-8. Figure 1 of the '130 Patent illustrates two bus drivers 11, 12 (consisting of transistors 20, 21, 22, and 23) and two complementary bus lines 14, 15 as inputs to a latching sense amplifier 16:

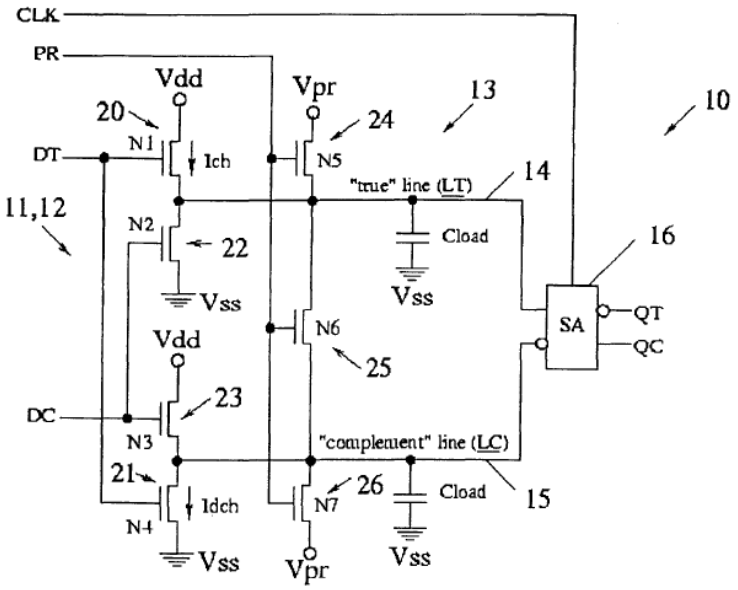


FIG.1.

18. The data transfer scheme operates in two phases: a precharge phase and a data transfer phase (Ex. 1001 2:12-13), with the bus drivers and

complementary bus lines operating in opposite phases to the latching sense amplifier (Ex. 1001 2:43-44). In other words, when the complementary bus lines and the bus drivers are in the precharge phase, the sense amplifier is in data transfer phase and vice versa.

19. Figure 2 of the ’130 Patent discloses a latching sense amplifier:

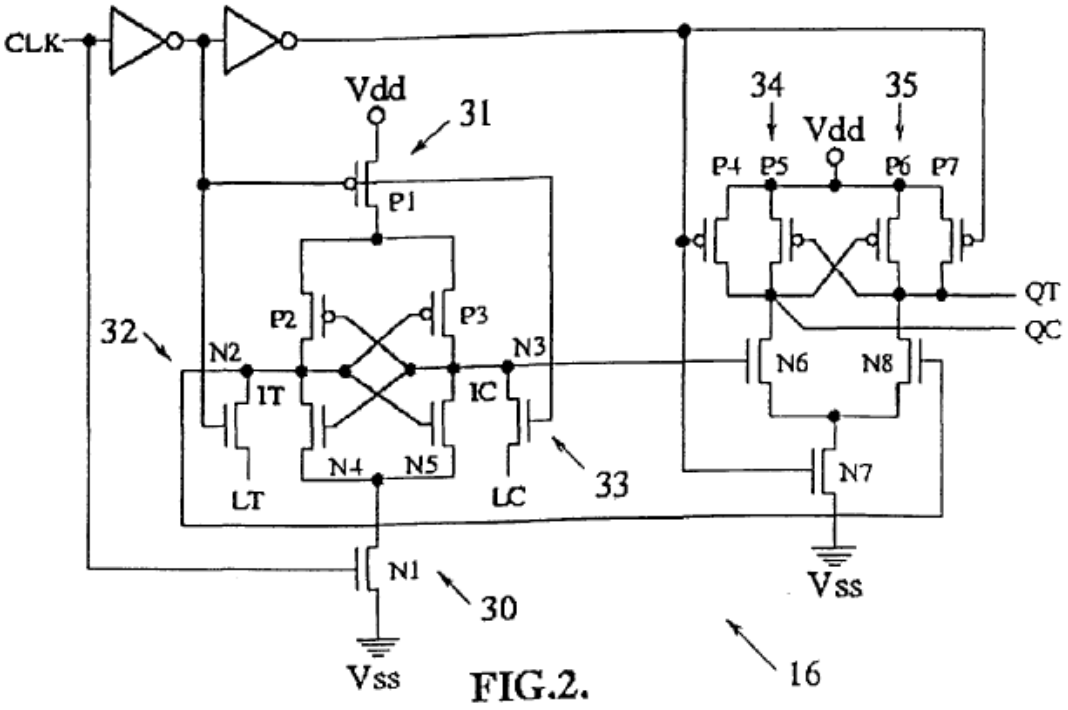


FIG.2.

20. I understand that the ’130 Patent includes 9 claims with claims 1 and 8 being independent and claims 2-7 and 9 being dependent from claim 1. I further understand that claim 9 was added during reexamination. As I note above, I was asked to opine with respect to some of the claims of the ’130 Patent. I have reproduced claim 1 below:

1. A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; aid [sic]

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage;

wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor.

V. CLAIM CONSTRUCTION

21. I understand that a claim subject to *inter partes* review receives the broadest reasonable construction in light of the specification of the patent in which it appears. I also understand that in these proceedings, any term that is not construed should be given its plain and ordinary meaning under the broadest reasonable construction. I have followed these principles in my analysis. I discuss

a few terms below and what I understand to be Petitioner's constructions of these terms.

A. Latching Sense Amplifier (Claims 1 and 3)

22. Independent claim 1 and dependent claim 3 of the '130 Patent recite a "latching sense amplifier." I understand Petitioner has offered that the broadest reasonable construction of the term "latching sense amplifier" that is consistent with the use of the term in the claims and specification of the '130 Patent is "a circuit, including a latch, that detects and amplifies signals." I have used this construction in my analysis and agree with it because the specification describes its latching sense amplifier to include a latch (*see, e.g.*, Ex. 1001 2:39-40, 2:48-50) for detecting (*see, e.g.*, Ex. 1001 2:33-38, 2:64-67) and amplifying received signals (*see, e.g.*, Ex. 1001 2:64-67). Furthermore, latching sense amplifiers were well known at the time of the alleged invention of the '130 Patent, and this construction is consistent with the understanding of one of ordinary skill in the art at the time of the alleged invention of the '130 Patent as well as dictionary definitions for similar terms (*see, e.g.*, Ex. 1009 at 679 (defining "sense amplifier" as "[a] circuit used to sense low-level voltages … and to amplify these signals to the logic voltage levels of the system"). In my opinion, the claims additionally specify what a "latching sense amplifier" has to include. For example, claim 1 requires that the "latching

sense amplifier" include both a first stage with a cross-coupled latch and an output stage. *See, e.g.*, Ex. 1001 4:8-13.

B. Stage (Claims 1, 3, and 9)

23. Independent claim 1 and dependent claims 3 and 9 recite a "stage." I understand Petitioner has offered that the broadest reasonable construction of the term "stage" that is consistent with the use of the term in the claims of the '130 Patent is "portion of a circuit." I have used this construction in my analysis and agree with it. In my experience and in the field, the term "stage" is sometimes used to refer to a portion of a circuit. This construction is consistent with dictionary definitions for the term. *See, e.g.*, Ex. 1009 at 728 (defining "stage" as "[a] single section of a multisection circuit or device"). This meaning is further reinforced by the claims. Claim 1 specifies that a latching sense amplifier comprises of a "first stage" and an "output stage," and claims 3 and 9 use the terms in the context of particular circuitry found within a "first stage" and an "output stage." *See, e.g.*, Ex.1001 4:8-13, 4:21-23, Reexam Cert. 1:20-21. As the latching sense amplifier is itself a circuit, it follows accordingly that particular "stages" of the circuit reflect a portion of the circuit. My understanding is also consistent with the specification's use of the term "stage." Ex. 1001 3:4-5.

VI. THE PRIOR ART DISCLOSES OR SUGGESTS EVERY FEATURE OF THE CHALLENGED CLAIMS OF THE '130 PATENT

24. I have reviewed several references, discussed further below, that I understand are prior art to the '130 Patent. In my opinion, these references disclose or suggest all features of the challenged claims of the '130 Patent.

A. Brief Description of the Prior Art

25. *Sukegawa* describes "a type of signal transmission circuit wherein the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals." *Sukegawa* 1:11-15. The signal transmission circuit disclosed sought to increase the signal transmission distance as well as increase the speed and lower the power consumption of a transmission. *Id.* 4:52-55. *Sukegawa* discloses that its signal transmission circuit comprises of "a driver circuit, a receiver circuit, an equalizer circuit, and an intermediate amplifier circuit." *Id.* 4:62-65. The intermediate amplifier circuit relies on positive feedback to amplify the signal provided by the driver circuit and transmit the amplified signal to the receiver circuit. *See, e.g.*, *id.* 5:1-4.

26. *Lu* describes a signal transmission system, and in particular, a sense amplifier utilized by DRAMs (Dynamic Random Access Memory). *See, e.g.*, *Lu* Abstract. *Lu* introduces "a sensing scheme for CMOS DRAM's [sic] in which the bit line is precharge to half-V_{DD}." *Id.* 451. Similar to *Sukegawa*, *Lu* discloses the

need to develop signal transmission systems faster in speed and lower in power consumption. *See, e.g.*, *id.* 453-54.

27. *Watanabe* relates to the transmission of signals in electronic circuits. *See, e.g.*, *Watanabe* Abstract, 1:10-13. Specifically, *Watanabe* introduces a "data transfer circuit incorporated in a DRAM." *Id.* 3:38-39. "[T]he data transfer circuit comprises a differential amplifier circuit 10, an equalizing circuit 11, a data latch circuit 12, a pair of first data lines 13, a pair of second data lines 14, and a pair of data output lines 15." *Id.* 3:41-44; *see also, e.g.*, *id.* Fig. 1. Like *Sukegawa* and *Lu*, the circuit disclosed by *Watanabe* was motivated by a need to increase the transmission speed of signals in electronic circuits. *See, e.g.*, *id.* 2:52-56 ("No time is therefore required to equalize either data lines, unlike in the conventional data transfer scheme. Hence, data can be transferred at high speed in DRAM according to the present invention.").

28. *Hardee* is yet another prior art reference relating to signal transmission, and in particular, "integrated circuit memories" and "sense amplifiers for use therein." *See, e.g.*, *Hardee* 1:8-10. *Hardee* introduces a sense amplifier highlighted by three "salient" features:

> (1) the connection of each sense amplifier via transistors or other switching devices to the power supply lines

without directly connecting together power supply lines

for multiple sense amplifiers;

(2) the use of local read amplifiers;

(3) the use of local write circuitry.

See i.d. 5:24-32.

29. All the prior art references mentioned above relate to signal transmission and were motivated to improve the efficiency of such transmissions. As such, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to combine the teachings of these references.

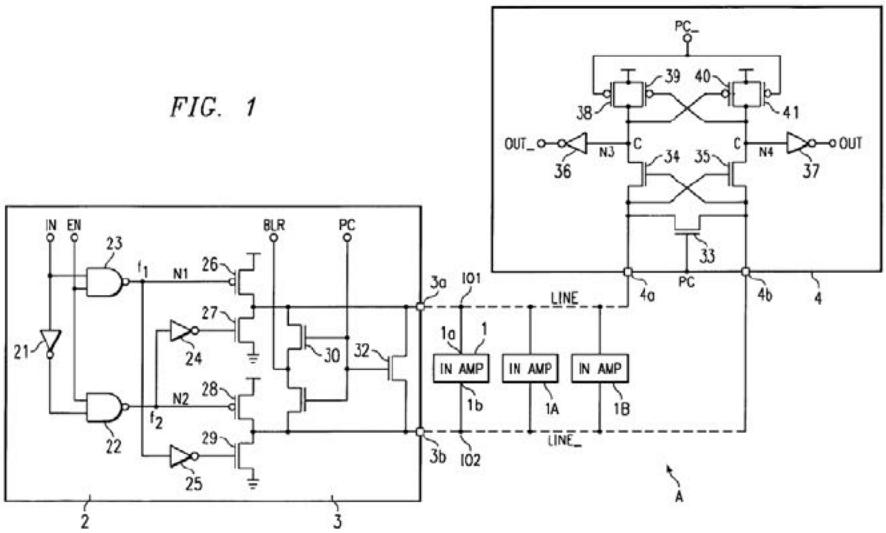
B. *Sukegawa* and *Lu*, Individually or in Combination with Other References, Disclose or Suggest Every Feature of the Challenged Claims of the '130 Patent

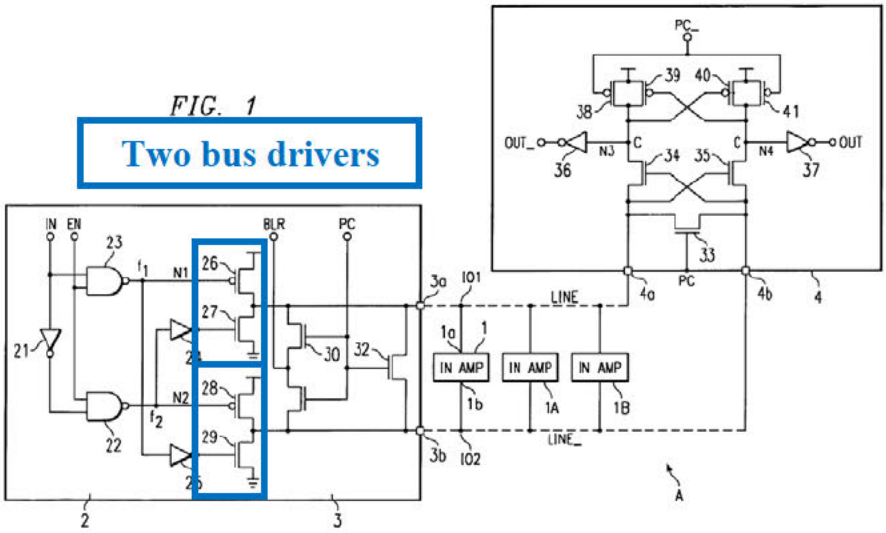
1. *Sukegawa* and *Lu* Disclose or Suggest the Features of Claims 1-2, 5-6, and 9

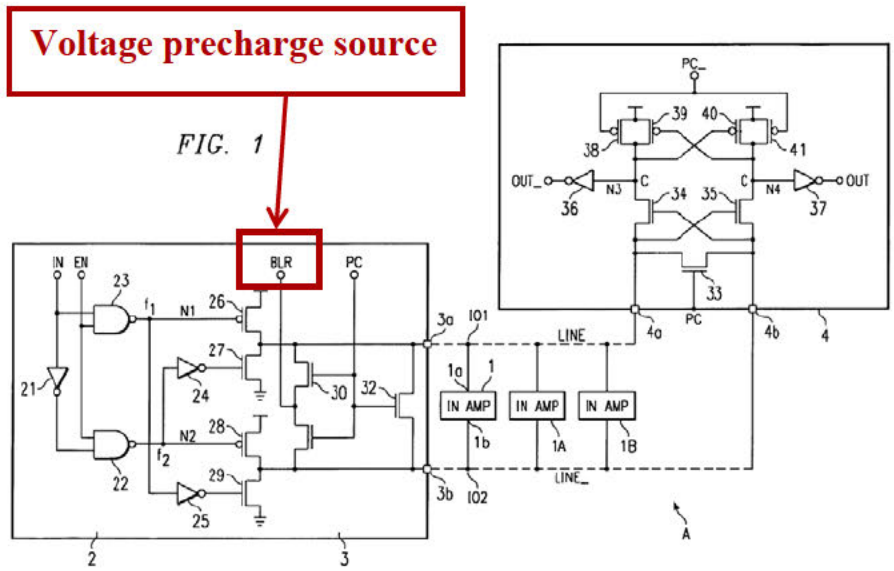
30. In my opinion and as shown in the charts below, *Sukegawa* and *Lu* disclose or suggest each and every feature recited in claims 1-2, 5-6, and 9 of the '130 Patent.

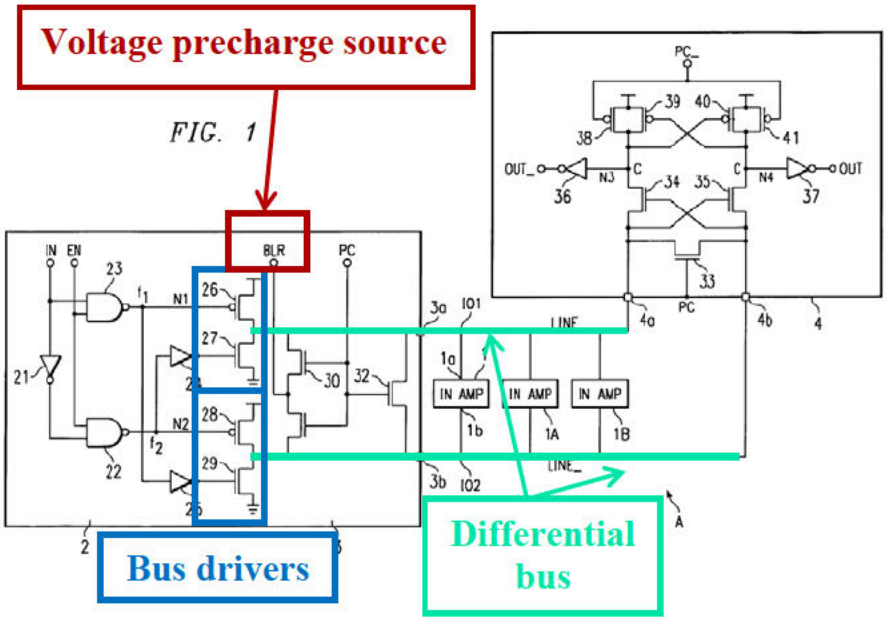
a. Claim 1

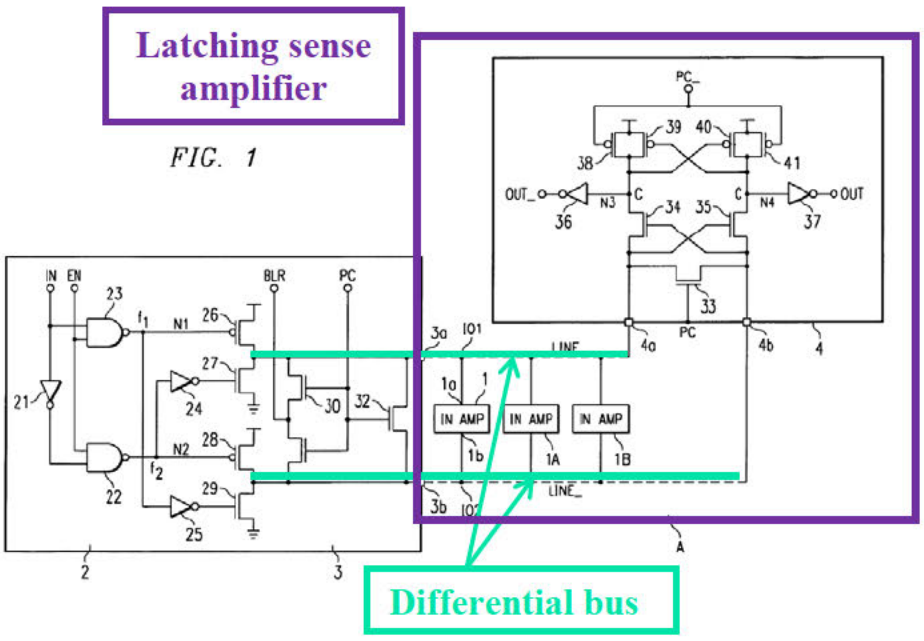
31. In my opinion, *Sukegawa* and *Lu* disclose or suggest each and every feature recited in claim 1.

Claim Language	*Sukegawa* and *Lu*
1. A data transfer arrangement comprising:	*Sukegawa* discloses a data transfer arrangement. For example, *Sukegawa* introduces "[a] signal transmission circuit which enables the distance of signal transmission as measured by the length of the wiring electrically connecting a driver circuit and a receiver circuit of the signal transmission circuit to be increased, while the signal delay and power consumption are reduced." *Sukegawa* Abstract. Fig. 1 of *Sukegawa* "is a circuit diagram illustrating an embodiment of the signal transmission circuit in accordance with the invention." *Sukegawa* 6:37-39. *FIG. 1* 
two bus drivers;	*Sukegawa* discloses two bus drivers (e.g., transistor group 26-27 and transistor group 28-29). *See, e.g.*, *Sukegawa* Fig. 1

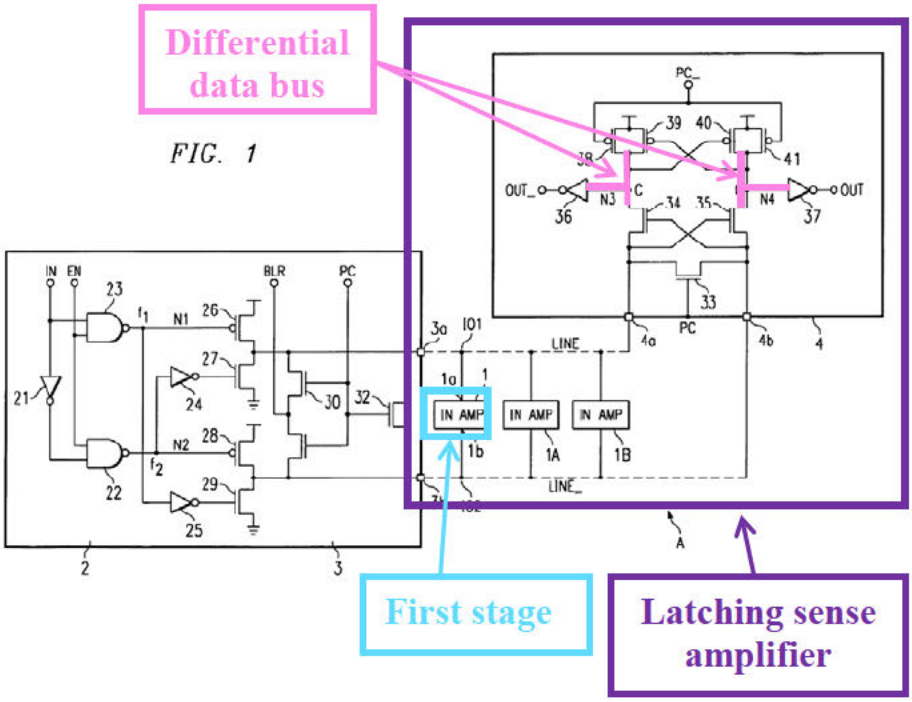
Claim Language	*Sukegawa* and *Lu*
	(annotated below).  *Sukegawa* discloses that "[d]river circuit 2 comprises input terminal IN, enable EN terminal, NAND gates 22, 23, CMOS inverters 21, 24, 25, pMOS transistors 26, 28, and nMOS transistors 27, 29. The input terminal IN of driver circuit 2 is connected through CMOS inverter 21 to one input terminal of NAND gate 22, and the input terminal IN is also connected to one input terminal of NAND gate 23. Enable EN terminal is connected to the other input terminals of NAND gates 22, 23. In the driver circuit 2, in the initial precharge state, the enable EN terminal is at L level, while node N1 and node N2 on the output sides of NAND gates 22, 23 are at H level." *Sukegawa*

Claim Language	*Sukegawa* and *Lu*
	8:11-23; *see also, e.g.*, *id.* 9:14-21.
a voltage precharge source;	*Sukegawa* discloses a voltage precharge source (e.g., BLR). *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).  *See also, e.g.*, *Sukegawa* 8:24-31 ("On the other hand, equalizer circuit 3 comprises BLR node with the balance signal applied to it, precharge (referred to as PC hereinafter) node and nMOS transistors 30-32. The BLR node is connected to the drain of nMOS transistor 30 and the drain of nMOS transistor 31, and the BLR node becomes the power source voltage $V_{DD}/2$ in the initial precharge source."), 7:29-37.
a differential bus coupled to the bus	*Sukegawa* discloses a differential bus (e.g., LINE, LINE_) coupled to the bus drivers (e.g., transistor group 26-27 and

Claim Language	*Sukegawa* and *Lu*
drivers and to the voltage precharge source; aid [sic]	transistor group 28-29) and to the voltage precharge source (e.g., BLR). *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).  "As shown in FIG. 1, in this intermediate amplifier circuit 1, positive line LINE which connects connecting terminal 3a of equalizer circuit 3 and input terminal 4a of receiver circuit 4 is connected to input/output shared terminal 1a at node 101, and negative line N-LINE (where N- represents the negative side) which connects output terminal 3b of equalizing circuit 3 and input terminal 4b of receiver circuit 4 is connected to input/output shared terminal 1b at node 102." *Sukegawa* 6:54-61.

Claim Language	*Sukegawa* and *Lu*
	One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have recognized LINE and LINE_ as the "differential bus" because a voltage differential (i.e., a difference in voltages between the two bus lines) can develop on these two bus lines. *See, e.g.*, *Sukegawa* 7:38-43.
a latching sense amplifier coupled to the differential bus;	*Sukegawa* discloses a latching sense amplifier (shown in purple) coupled to the differential bus (e.g., LINE, LINE_). *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).  The purple box drawn above for the latching sense amplifier is consistent with Petitioner's proposed construction of "latching sense amplifier," as it is a circuit, including a latch, that detects

Claim Language	*Sukegawa* and *Lu*
	and amplifies signals. Each intermediate amplifier 1, 1A, and 1B provides a latch that detects and amplifies the signal on LINE and LINE_. *See, e.g.*, *Sukegawa* Fig. 2, 7:1-8:6. *Sukegawa* further discloses that "[a]s shown in FIG. 1, in this intermediate amplifier circuit 1, positive line LINE which connects connecting terminal 3a of equalizer circuit 3 and input terminal 4a of receiver circuit 4 is connected to input/output shared terminal 1a at node 101, and negative line N-LINE (where N- represents the negative side) which connects output terminal 3b of equalizing circuit 3 and input terminal 4b of receiver circuit 4 is connected to input/output shared terminal 1b at node 102." *Sukegawa* 6:54-61.
wherein the latching sense amplifier comprises: a first stage including a cross-coupled latch coupled to a	*Sukegawa* discloses a latching sense amplifier (shown in purple) wherein a first stage (e.g., IN AMP 1, shown in light blue) includes a cross-coupled latch (e.g., transistors 10, 11, 14, 15) coupled to a differential data bus (pink lines). *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).

Claim Language	*Sukegawa* and *Lu*
differential data bus; and	 The light blue box drawn above for the first stage is consistent with Petitioner's proposed construction of "stage," as it is a "portion of a circuit." Namely, the first stage is a portion of the latching sense amplifier. In particular, intermediate amplifier 1 latches and amplifies voltages received through nodes 1a and 1b, and outputs the amplified voltages through the same nodes. *See, e.g.*, *Sukegawa* 7:1-8:6. Fig. 2 of *Sukegawa* further discloses the first stage and its cross-coupled latch: "a circuit diagram illustrating the specific

Claim Language	*Sukegawa* and *Lu*
	configuration of the first intermediate amplifier circuit 1." *Sukegawa* 6:66-67.

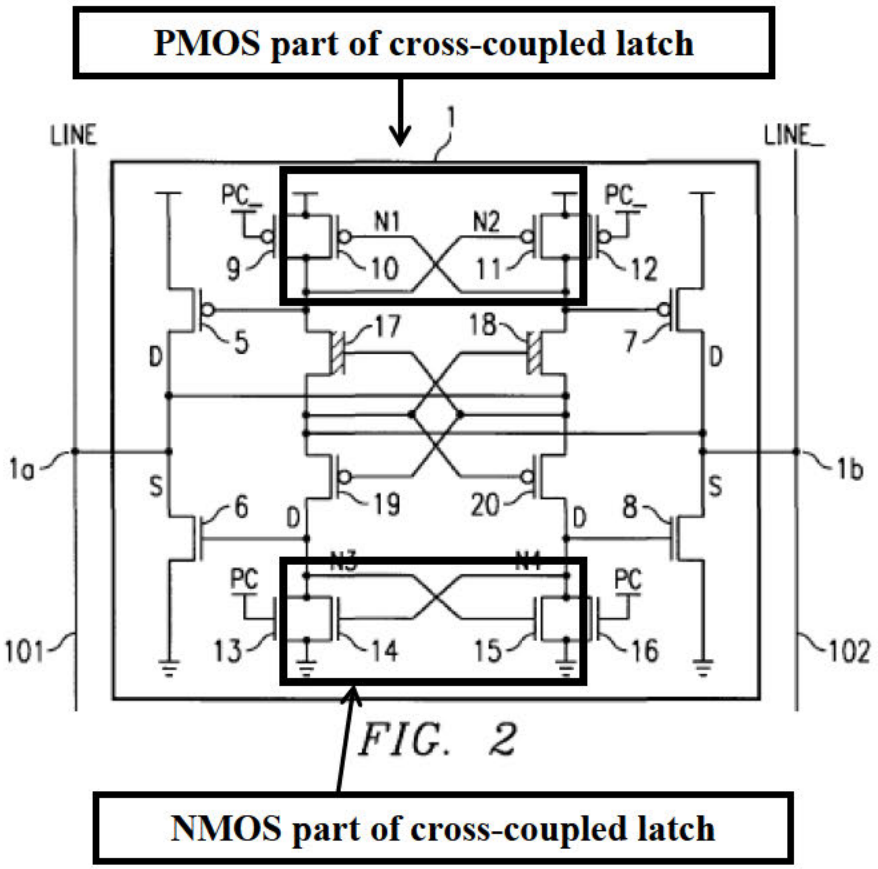
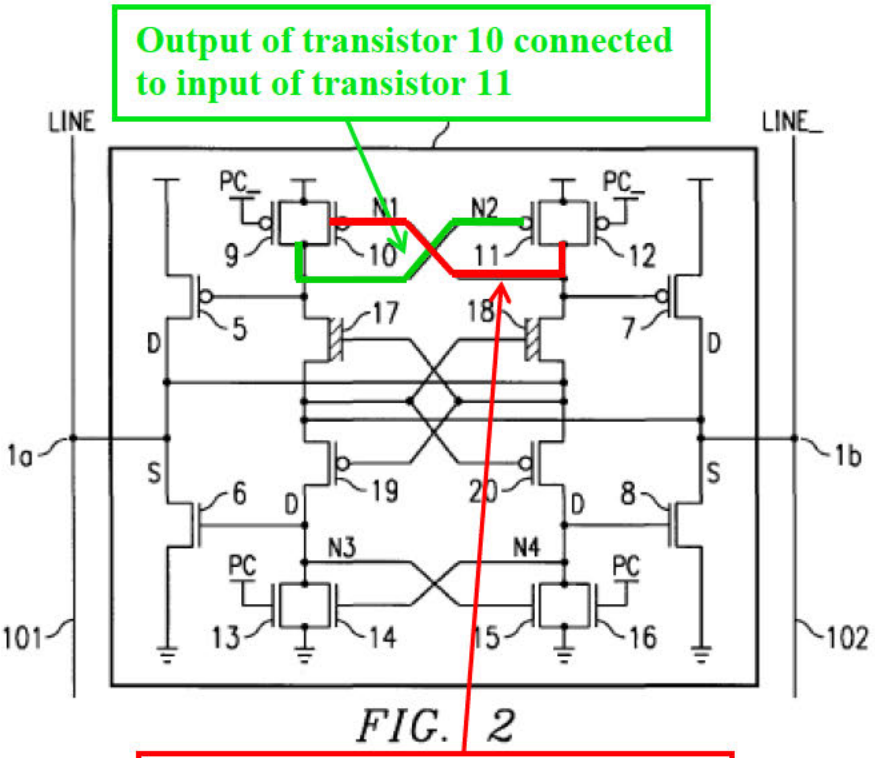
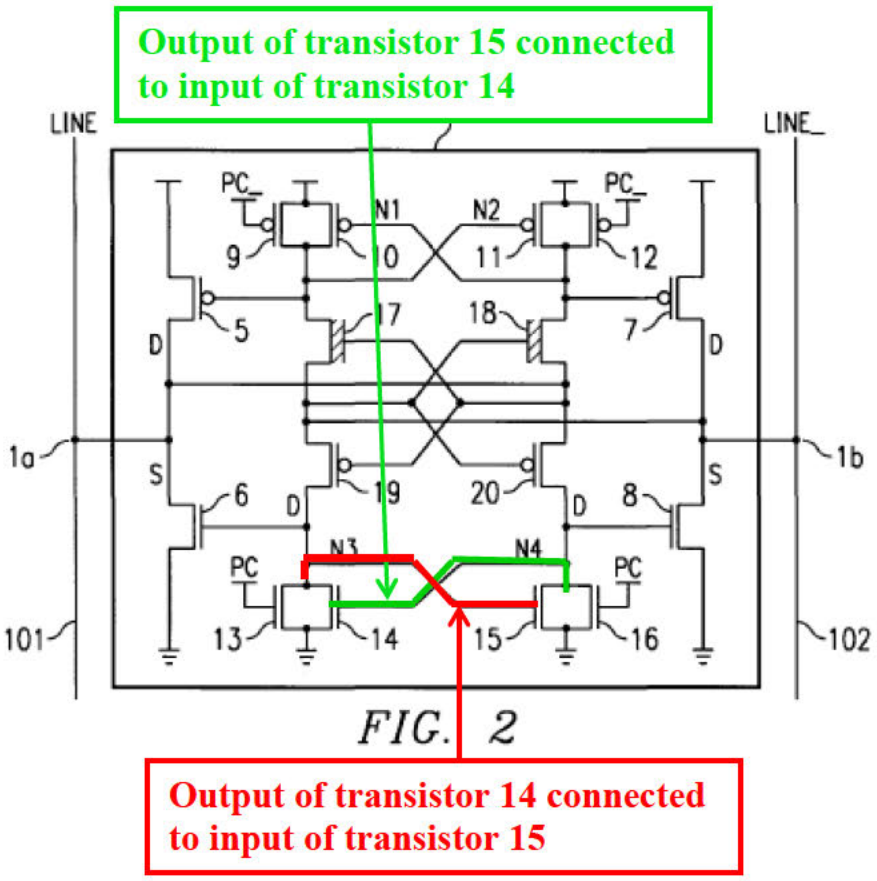


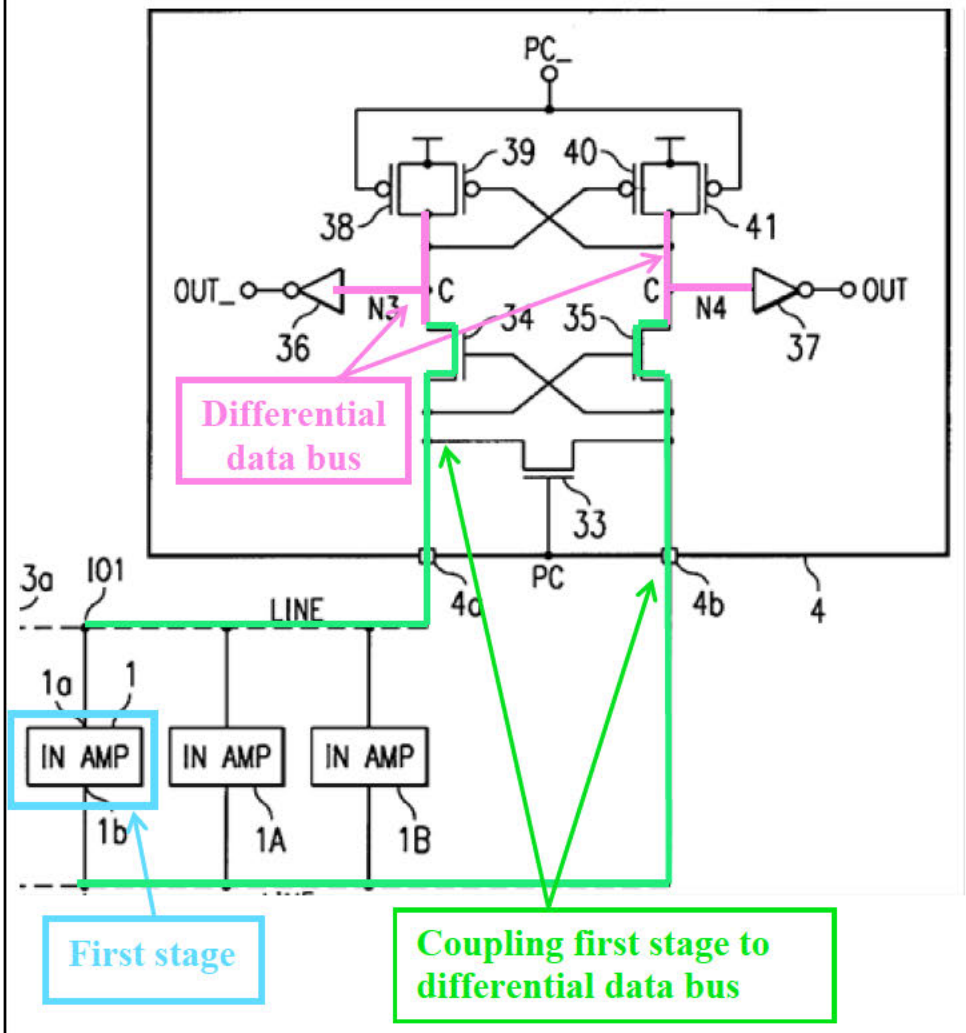
FIG. 2

One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have recognized, based on *Sukegawa*'s disclosure, that the cross-coupled latch comprises of transistors 10, 11, 14, and 15 because these transistors act to regenerate full logic levels (both high and low) on LINE and LINE_. *See, e.g.*, *Sukegawa* 9:14-21.

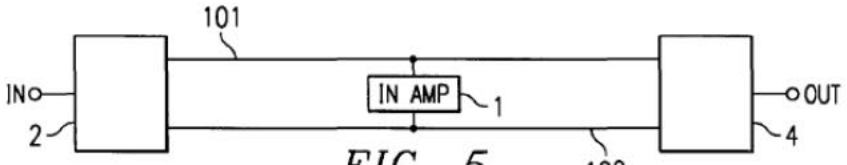
Claim Language	*Sukegawa* and *Lu*
	Moreover, these transistors are cross-coupled because the output of a first transistor (e.g., 10) is tied to the input of a second transistor (e.g., 11), and the output of the second transistor (e.g., 11) is tied to the input of the first transistor (e.g., 10).  *FIG. 2* Likewise, the output of transistor 14 is tied to the input of transistor 15, and vice versa.

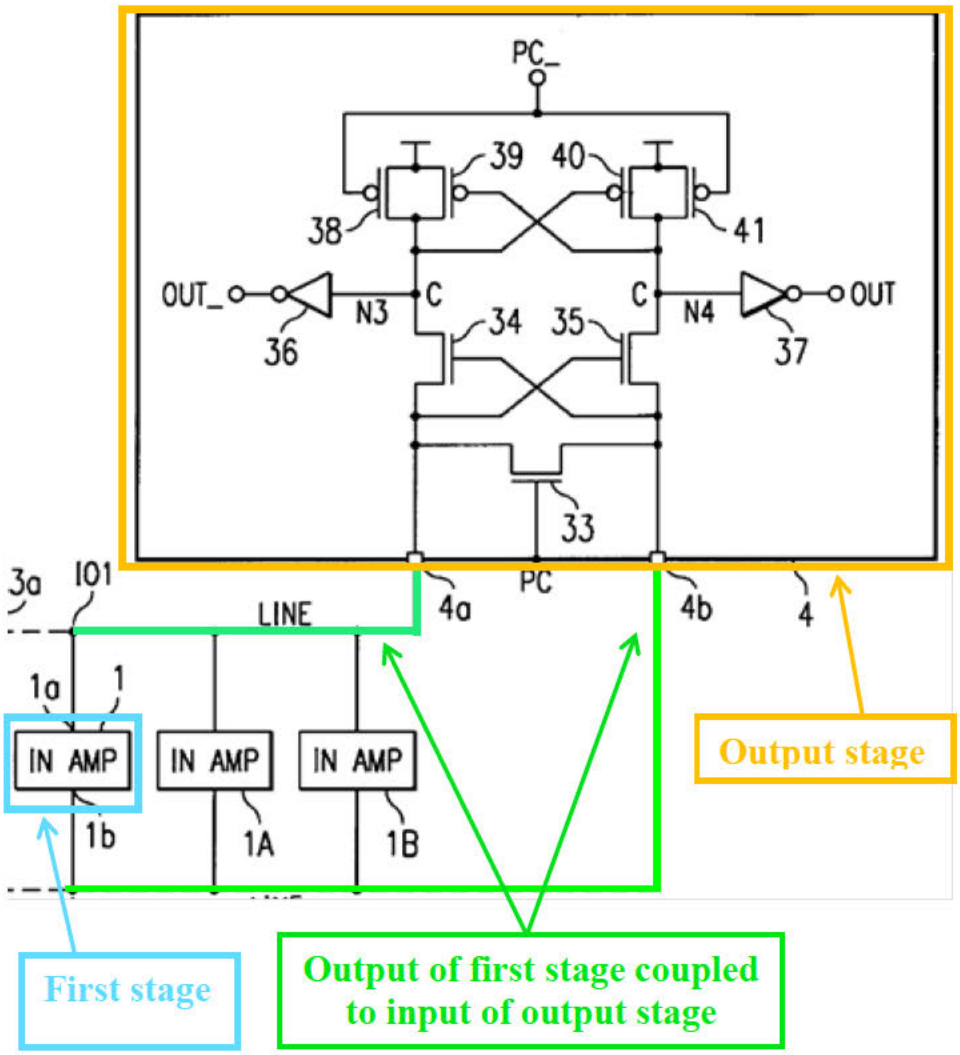
Claim Language	*Sukegawa* and *Lu*
	 *FIG. 2* The first stage is further coupled to the differential data bus via LINE, LINE_ and transistors 34, 35 (*see e.g.*, *Sukegawa* Fig. 1 (annotated below), 6:54-61):

Claim Language	*Sukegawa* and *Lu*

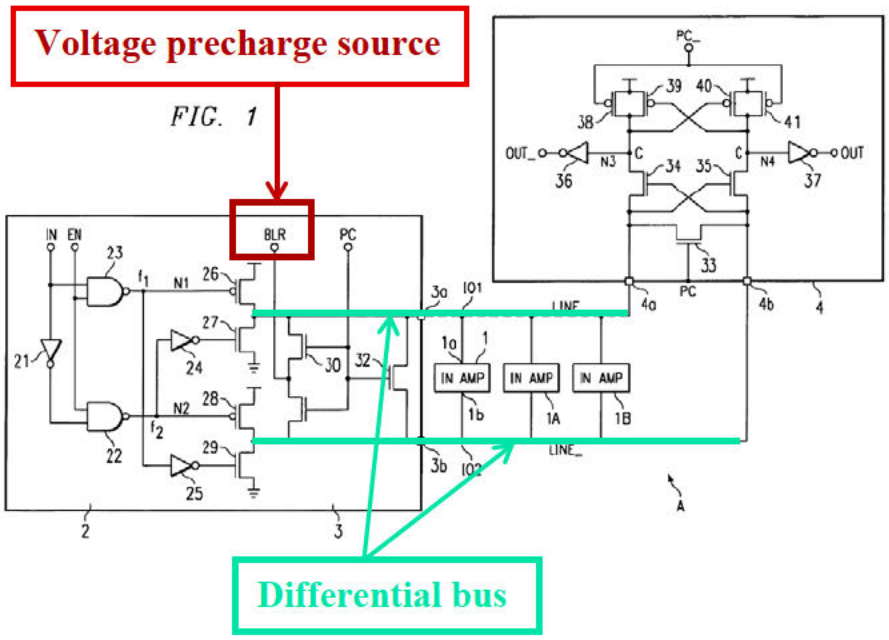
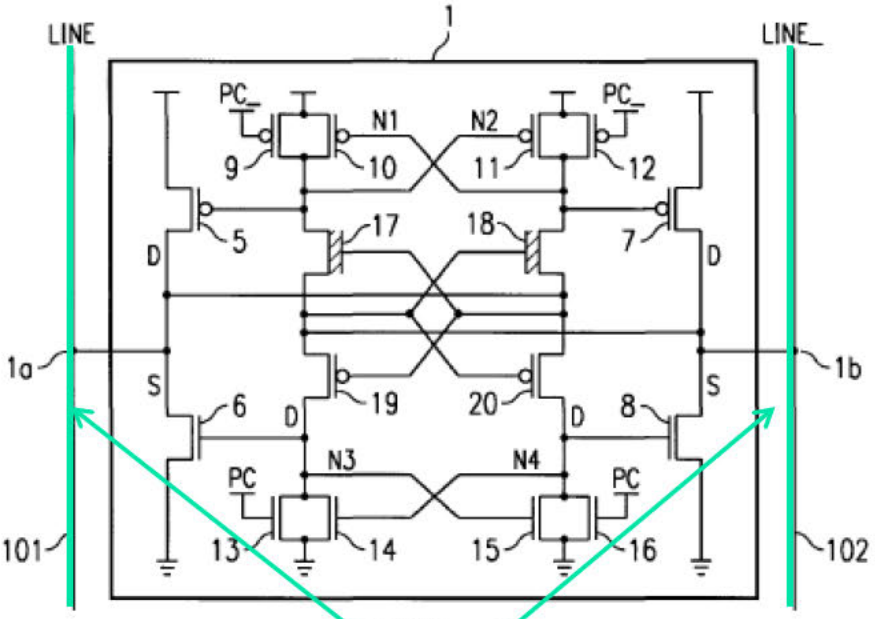


One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have recognized lines associated with nodes C (shown above in pink) as the "differential data bus" because the pink highlighted lines represent an amplified voltage differential representative of the data to be read out by the latching sense amplifier. *See, e.g.*,

Claim Language	*Sukegawa* and *Lu*
	Sukegawa 9:14-24. Indeed, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood the pink highlighted lines to include differential data because of the amplified voltage differential on these lines. Moreover, Fig. 5 of *Sukegawa* also teaches one intermediate amplifier (i.e. first stage) prior to the receiver circuit 4 (as discussed below, the receiver circuit is *Sukegawa*'s "output stage"), and thus the first stage and the differential data bus can be coupled without going through additional intermediate amplifiers:  *FIG. 5*
an output stage coupled to an output of said first stage; wherein the	*Sukegawa* discloses a latching sense amplifier wherein an output stage (e.g., receiver circuit 4, shown in orange) is coupled to an output of the first stage (e.g., IN AMP 1, shown in light blue), and wherein the output of the first stage is coupled to an input of the output stage. *See, e.g.*, *Sukegawa*

Claim Language	*Sukegawa* and *Lu*
output of the first stage is coupled to an input of the output stage;	Fig. 1 (annotated below).  The orange box drawn above for the output stage comprises of receiver circuit 4 and is consistent with Petitioner's proposed construction of "stage," as it is a "portion of a circuit." Namely, the output stage is a portion of the latching sense amplifier circuit. In particular, the identified "output stage"

Claim Language	***Sukegawa* and *Lu***
	performs the function of receiving and driving the output of an amplified voltage differential amplified by *Sukegawa*'s intermediate amplifiers. *See, e.g.*, *Sukegawa* 8:50-9:24. *Sukegawa* further discloses that "[a]s shown in FIG. 1, in this intermediate amplifier circuit 1, *positive line LINE which connects connecting terminal 3a of equalizer circuit 3 and input terminal 4a of receiver circuit 4* is connected to input/output shared terminal 1a at node 101, *and inverted line N-LINE (where N- represents the negative side) which connects output terminal 3b of equalizer circuit 3 and input terminal 4b of receiver circuit 4* is connected to input/output shared terminal 1b at node 102." *Sukegawa* 6:54-61 (emphasis added).
wherein the differential bus and the differential data bus are precharge to a voltage Vpr	*Sukegawa* discloses that the differential bus (e.g., LINE and LINE_) is precharged to Vdd/2, i.e., a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor. *See, e.g.*, *Sukegawa* Figs. 1, 2 (annotated below).

Claim Language	*Sukegawa* and *Lu*
between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor.	  FIG. 2 Differential bus *Sukegawa* discloses, for example, that "[w]hen intermediate

Claim Language	*Sukegawa* and *Lu*
	amplifier circuit 1 is in the initial precharge state, pMOS transistors 5, 7 and nMOS transistors 6, 8 are all in OFF (nonconductive) state. In this case, *the voltage at nodes 101 and 102 becomes the intermediate voltage VDD/2*; gate node N1 of pMOS transistor 10 and gate node N2 of pMOS transistor 11 become the high level (referred to as 'H level' hereinafter); and gate node N3 of nMOS transistor 15 and gate node N4 of nMOS transistor 14 become the low level (referred to as 'L level' hereinafter). This is because, in the initial precharge state, the PC terminal becomes the H level, while the N-PC terminal becomes the L level." *Sukegawa* 7:26-37 (emphasis added); *see also id.* Figs. 1 (identifying nodes 101 and 102), 2 (same). Further, "[t]he BLR node is connected to the drain of the nMOS transistor 30 and the drain of nMOS transistor 31, and the BLR node becomes the power source voltage VDD/2 in the initial precharge state." *Sukegawa* 8:28-31; *see also, e.g., id.* 9:14-21. While *Sukegawa* discloses that the differential data bus is

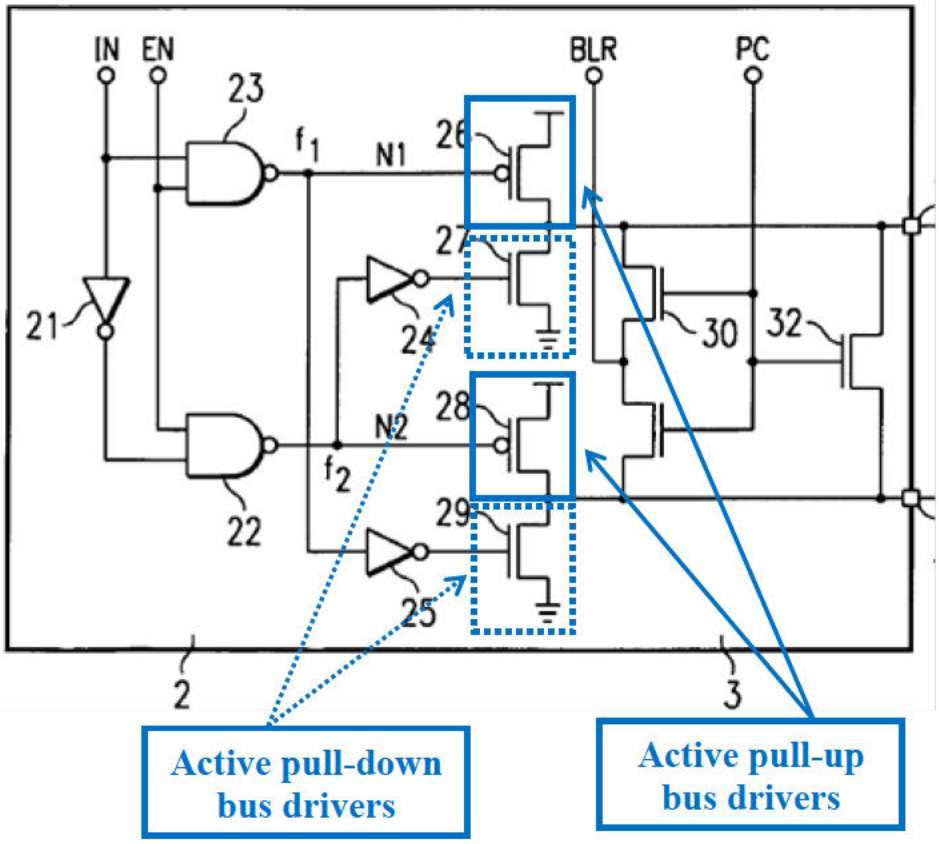
Claim Language	*Sukegawa* and *Lu*
	precharged to a voltage Vdd (*see, e.g.*, *Sukegawa* 9:4-7), one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to modify *Sukegawa* so that the differential data bus is precharged to an intermediate voltage rather than Vdd. One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that precharging to an intermediate voltage would have been desirable to speed up operation of the circuit because pulling up or pulling down a node precharged to an intermediate voltage to full logic levels would require a smaller voltage swing (and thus be faster) when compared to a full Vdd voltage swing when pulling down a node precharged to Vdd. For example, when the intermediate precharge voltage is Vdd/2, pulling up or down a node precharged to Vdd/2 would merely require half the voltage change when compared to pulling down a node precharged to Vdd. This reasoning is disclosed by, for example, *Lu*: "At sensing and bit-line precharge in half-V_{DD} sensing, the pullup and pulldown of bitlines are balanced and have only half-V_{DD} swing." *Lu* 453.

Claim Language	***Sukegawa* and *Lu***
	Given the overlapping subject matter between *Sukegawa* and *Lu* and the apparent benefit of precharging to Vdd/2, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to apply the teachings of one reference to the other. In fact, modifying *Sukegawa* to precharge its differential data bus to the intermediate voltage Vdd/2, as taught by *Lu*, would have amounted to nothing more than applying known techniques to improve similar devices in the same way to yield predictable results.

b. Claim 2

32. In my opinion, *Sukegawa* and *Lu* disclose or suggest each and every feature recited in claim 2.

Claim Language	***Sukegawa* and *Lu***
2. The data transfer arrangement in accordance with claim 1 wherein	*Sukegawa* discloses a data transfer arrangement wherein the bus drivers (e.g., transistor group 26-27 and transistor group 28-29) comprise active pull-up (transistors 26, 28) and active pull-down (transistors 27, 29) bus drivers. *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).

Claim Language	*Sukegawa* and *Lu*
the bus drivers comprise active pull-up and active pull-down bus drivers.	 *Sukegawa* teaches that the bus drivers comprise of active pull-up drivers because PMOS transistors 26 and 28 may couple LINE or LINE_ to Vdd (indicated by the flat line to the top of transistors 26 and 28) and thus pull up the output. *See, e.g.*, *Sukegawa* Fig. 1, 9:14-21. Similarly, *Sukegawa* teaches that the bus drivers comprise of active pull-down drivers as NMOS transistors 27 and 29 may couple LINE or LINE_ to ground (indicated by the dashed lines in the shape of a triangle to the

Claim Language	***Sukegawa* and *Lu***
	bottom of transistors 27 and 29) and thus pull down the outputs. *See, e.g.*, *Sukegawa* Fig. 1, 9:14-21.

c. Claim 5

33. In my opinion, *Sukegawa* and *Lu* disclose or suggest each and every feature recited in claim 5.

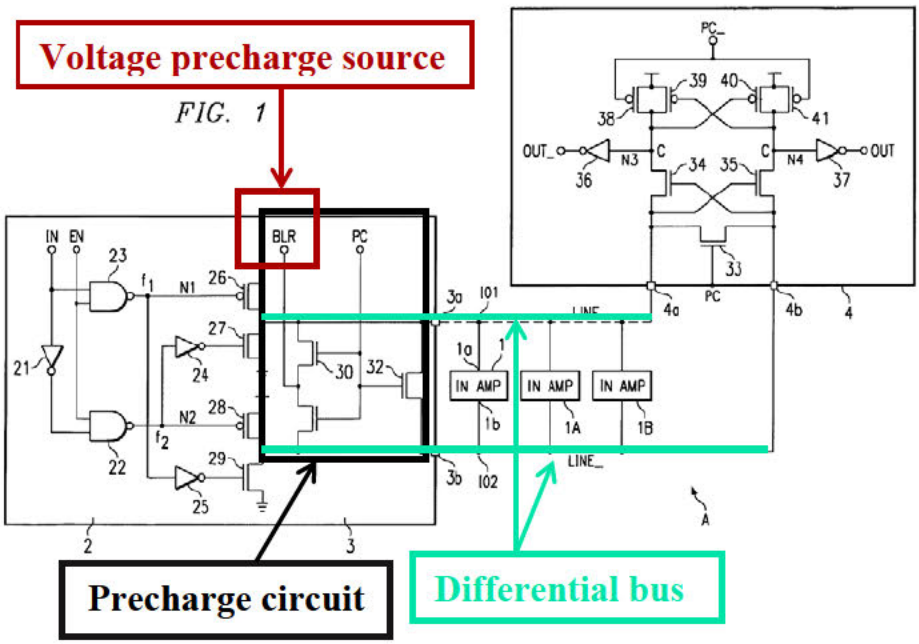
Claim Language	***Sukegawa* and *Lu***
5. The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic	*Sukegawa* discloses a data transfer arrangement wherein the voltage precharge source (e.g., BLR) is configured to precharge the differential bus (e.g., LINE, LINE_) to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage. *Sukegawa* discloses that "[w]hen intermediate amplifier circuit 1 is in the initial precharge state, pMOS transistors 5, 7 and nMOS transistors 6, 8 are all in OFF (nonconductive) state. In this case, *the voltage at nodes 101 and 102 becomes the intermediate voltage VDD/2*; gate node N1 of pMOS transistor 10 and gate node N2 of pMOS transistor 11 become the high level (referred to as 'H level' hereinafter); and gate node N3 of nMOS transistor 15 and gate node N4 of nMOS transistor 14

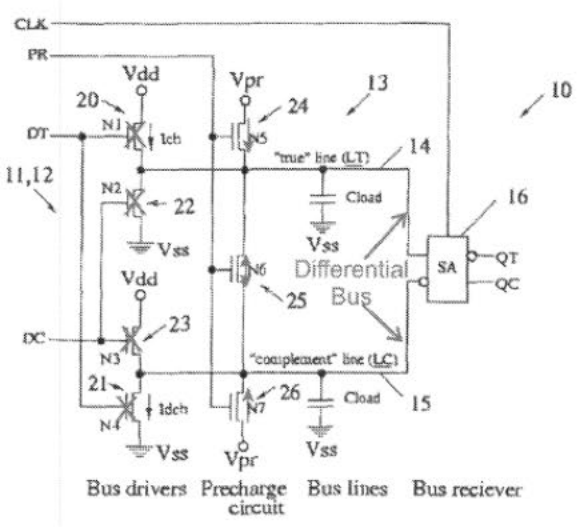
Claim Language	*Sukegawa* and *Lu*
high voltage and greater than a logic low voltage.	become the low level (referred to as 'L level' hereinafter). This is because, in the initial precharge state, the PC terminal becomes the H level, while the N-PC terminal becomes the L level." *Sukegawa* 7:26-37 (emphasis added). *Sukegawa* further discloses that "[t]he BLR node is connected to the drain of the nMOS transistor 30 and the drain of nMOS transistor 31, and the BLR node becomes the power source voltage VDD/2 in the initial precharge state." *Sukegawa* 8:28-31; *see also, e.g.*, *id.* 9:14-21.

d. Claim 6

34. In my opinion, *Sukegawa* and *Lu* disclose or suggest each and every feature recited in claim 6.

Claim Language	*Sukegawa* and *Lu*
6. The data transfer arrangement in accordance with claim 1 further comprising a	*Sukegawa* discloses a data transfer arrangement further comprising a precharge circuit coupled between the precharge source (e.g., BLR) and the differential bus (e.g., LINE, LINE_). *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).

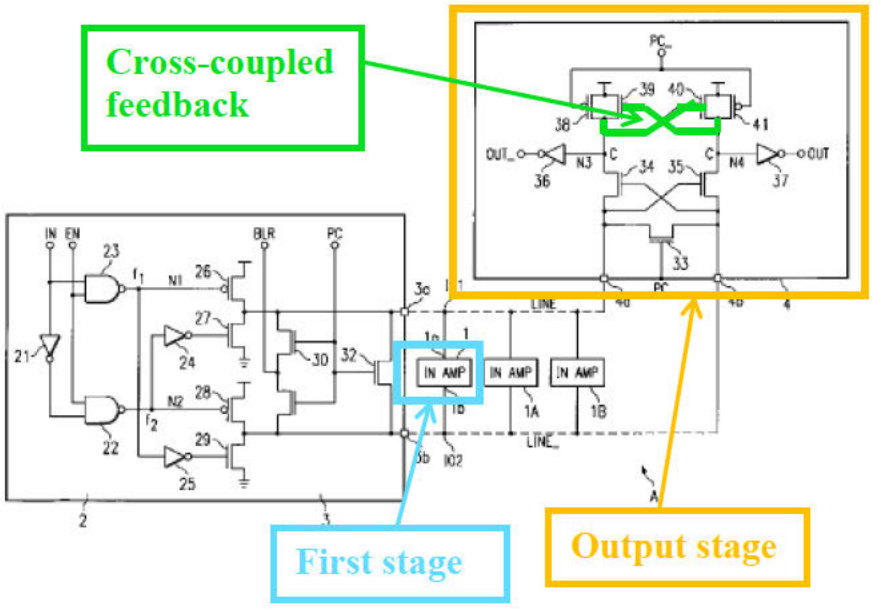
Claim Language	*Sukegawa* and *Lu*
precharge circuit coupled between the precharge source and the differential bus.	 *Sukegawa* discloses that "[t]he PC node is connected to the gates of nMOS transistors 30, 31, and 32. In the initial precharge state, the PC node enters the H level; in the drive state, the PC node changes from H level to L level; in the precharge state, it changes from L level to H level. The BLR node is connected to the drain of the nMOS transistor 30 and the drain of nMOS transistor 31, and the BLR node becomes the power source voltage VDD/2 in the initial precharge state." *Sukegawa* 8:28-36. The precharge circuit is between the voltage precharge source

Claim Language	*Sukegawa* and *Lu*
	and the differential bus because the transistors within the precharge circuit connect the voltage precharge source to the differential bus. *Sukegawa* 8:28-36. This is consistent with the '130 Patent's disclosure and the Patent Owner's characterization of the disclosure during reexamination:  Ex. 1004, p. 68 (declaration of Dr. Philip Koopman disclosing precharge circuit 13 and the "differential bus").

e. Claim 9

35. In my opinion, *Sukegawa* and *Lu* disclose or suggest each and every feature recited in claim 9.

Claim Language	*Sukegawa* and *Lu*
9. The data	*Sukegawa* discloses a data transfer arrangement wherein the

Claim Language	*Sukegawa* and *Lu*
transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback.	output stage (e.g., receiver circuit 4) includes cross-coupled feedback. *See, e.g.*, *Sukegawa* Fig. 1 (annotated below).  *See also, e.g.*, *Sukegawa* 5:5-12. The cross-coupled feedback identified above is consistent with the "cross-coupled feedback" identified by the Patent Owner during *inter partes* reexamination. Specifically, Patent Owner argued that "cross-coupled feedback" was demonstrated by Fig. 2 of the '130 Patent, which is nearly (if not entirely) identical with Petitioner's mapping of *Sukegawa*:

Claim Language	*Sukegawa* and *Lu*

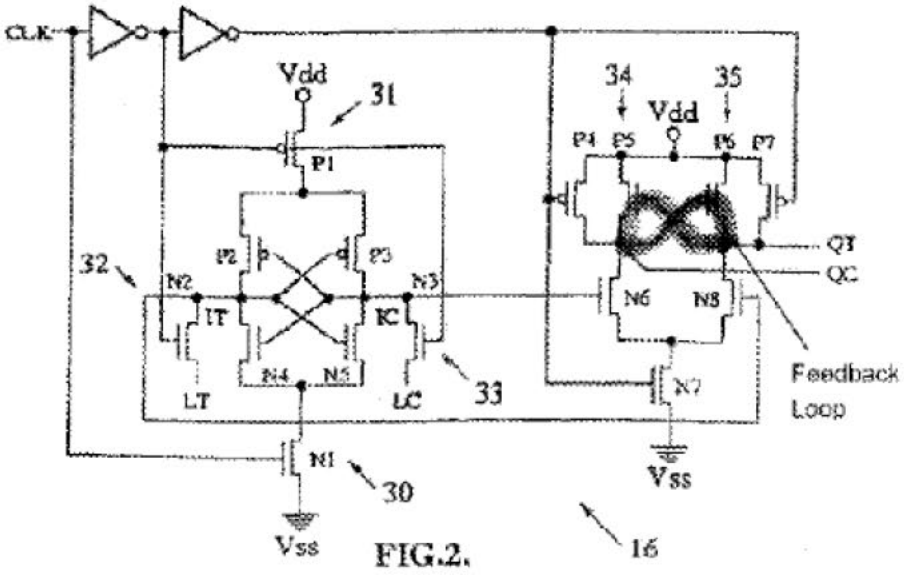


FIG.2.

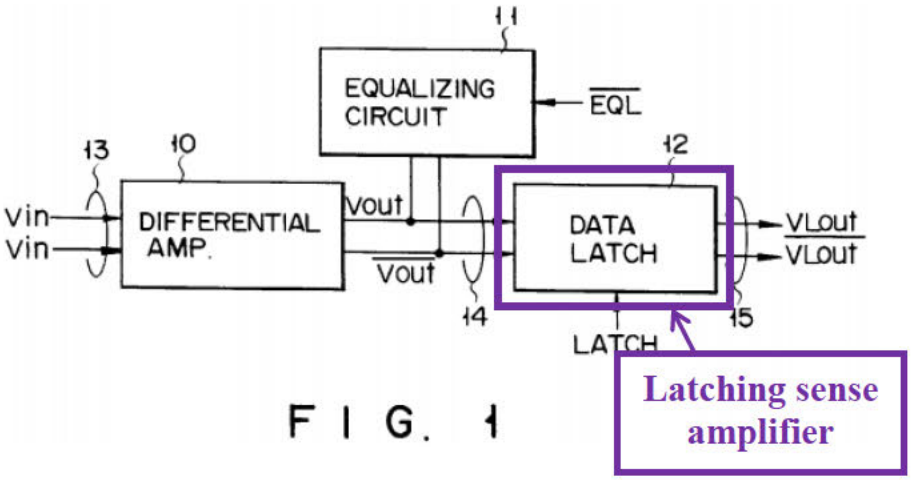
Ex. 1004, p. 127. Patent Owner argued that "feedback' should be construed to mean "a loop in the topography of a circuit where, in addition to its input being connected to its output, its output is also connected to its input via a different path." *Id.*, p. 126. The circuit in *Sukegawa* meets this definition as the output C above transistor 34 is tied to the input gate of transistor 40 and the output C above transistor 35 is tied to the input gate of transistor 30. *See, e.g.*, *Sukegawa* 8:59-64, Fig. 1. Indeed, this identical circuitry disclosed by Fig. 2 of the '130 Patent was not only sufficient to satisfy the "feedback" limitation of claim 9, but also the additional limitation that the feedback must be "cross-coupled." Ex. 1004, pp. 126-27, 139-

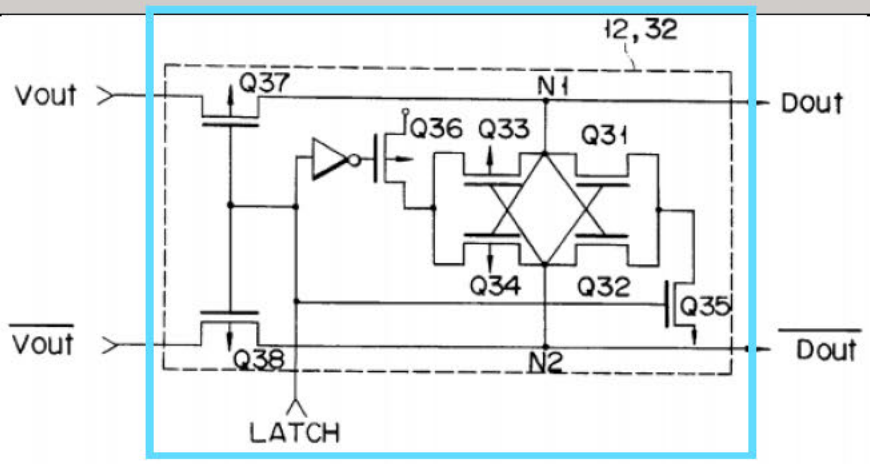
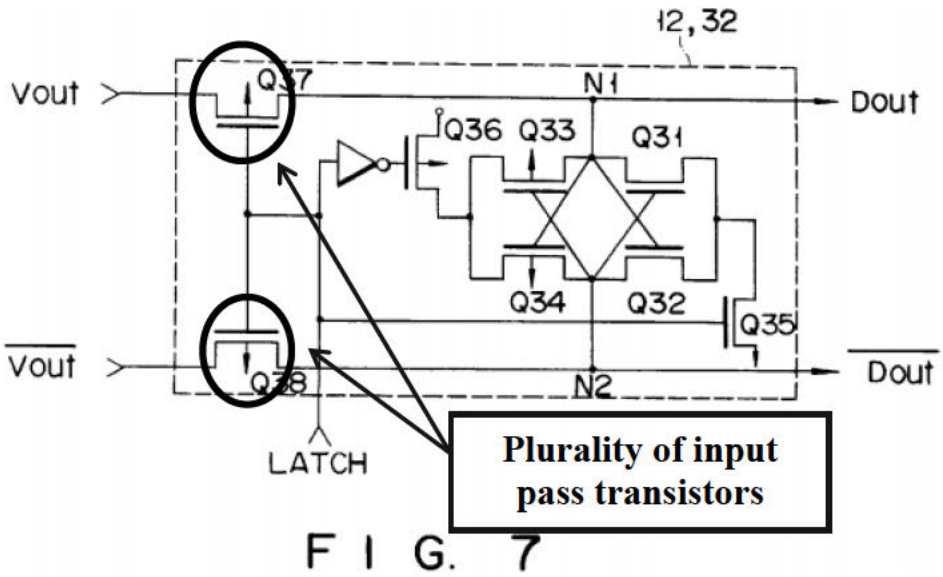
Claim Language	***Sukegawa* and *Lu***
	40. Accordingly, in my view, *Sukegawa* discloses cross-coupled feedback.

2. *Sukegawa*, *Lu*, and *Watanabe* Disclose or Suggest the Features of Claim 3

36. In my opinion, *Sukegawa*, *Lu*, and *Watanabe* disclose or suggest each and every feature recited in claim 3. One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to combine the teachings of *Sukegawa* and *Lu* with *Watanabe* as all three references cover the same field of technology – transmission of data through electronic circuits. *See supra* Section VI.A. Furthermore, one would have been motivated to modify the first stage of the latching sense amplifier of *Sukegawa* with the first stage of *Watanabe*'s latching sense amplifier as *Watanabe*'s first stage comprises fewer transistors, and thus would speed up the operation of the circuit. Fewer control signals and a smaller circuit layout are also used in the first stage of *Watanabe*. Both of these benefits allow more circuitry to be placed into a fixed area on the chip, and therefore, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would additionally have been motivated to modify *Sukegawa*'s first stage with *Watanabe*'s first stage. In fact, this change would have amounted to nothing more than applying known techniques to improve similar devices in the same way to yield predictable results.

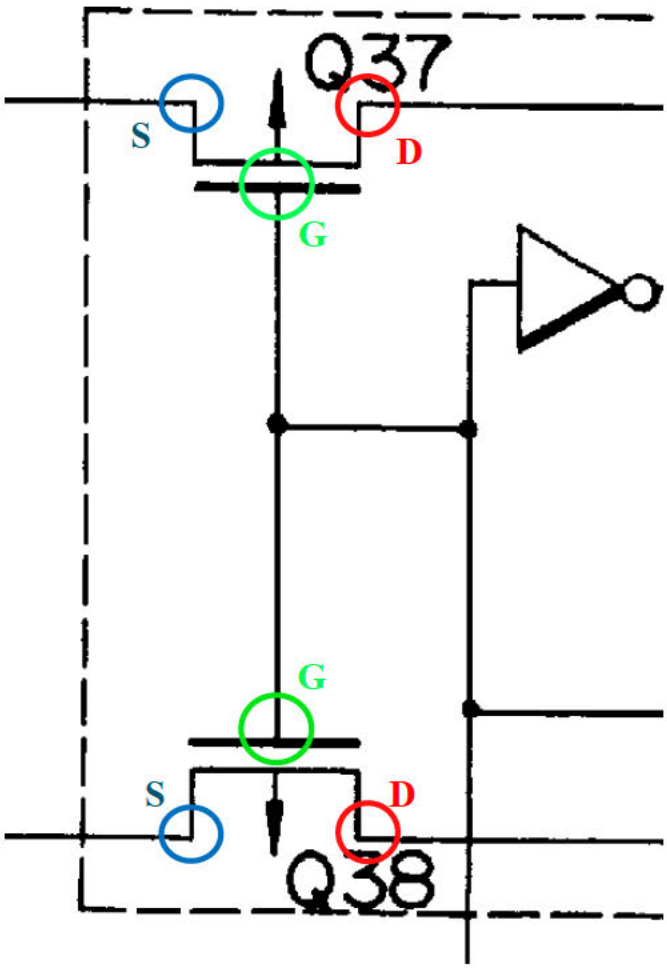
37. Further, as demonstrated in the exemplary disclosures below, *Sukegawa*, *Lu*, and *Watanabe* disclose or suggest each and every feature recited in claim 3.

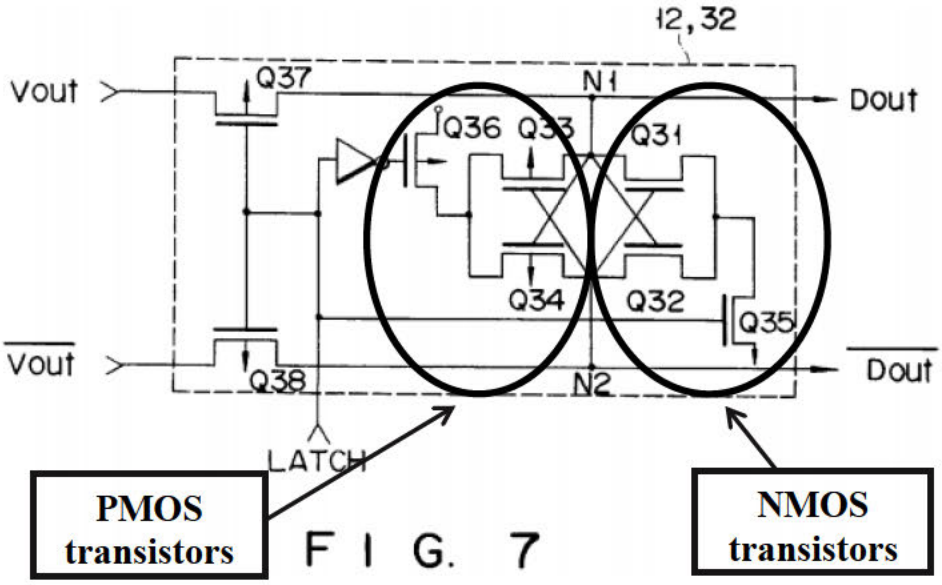
Claim Language	***Sukegawa*, *Lu*, and *Watanabe***
3. The data transfer arrangement in accordance with claim 1,	As illustrated with claim 1, *Sukegawa* and *Lu* discloses a data transfer arrangement including a latching sense amplifier with a first stage. *Watanabe* also discloses a data transfer arrangement including a latching sense amplifier (e.g., data latch 12) with a first stage. *See, e.g., Watanabe* Fig. 1 (annotated below).  FIG. 1 Data latch 12 of *Watanabe*, which includes a first stage, is further detailed in Fig. 7. *See, e.g.*, *Watanabe* Fig. 7 (annotated below), 4:13-16.

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	 F I G. 7
wherein the first stage of the latching sense amplifier comprises: a plurality of input pass transistors each having a gate, a source terminal, and a drain; and	*Watanabe* discloses a first stage of a latching sense amplifier comprising a plurality of input pass transistors (e.g., transistors Q37, Q38) each having a gate, a source terminal, and a drain. *See, e.g.*, *Watanabe* Fig. 7 (annotated below).  F I G. 7 One of ordinary skill in the art at the time of the alleged

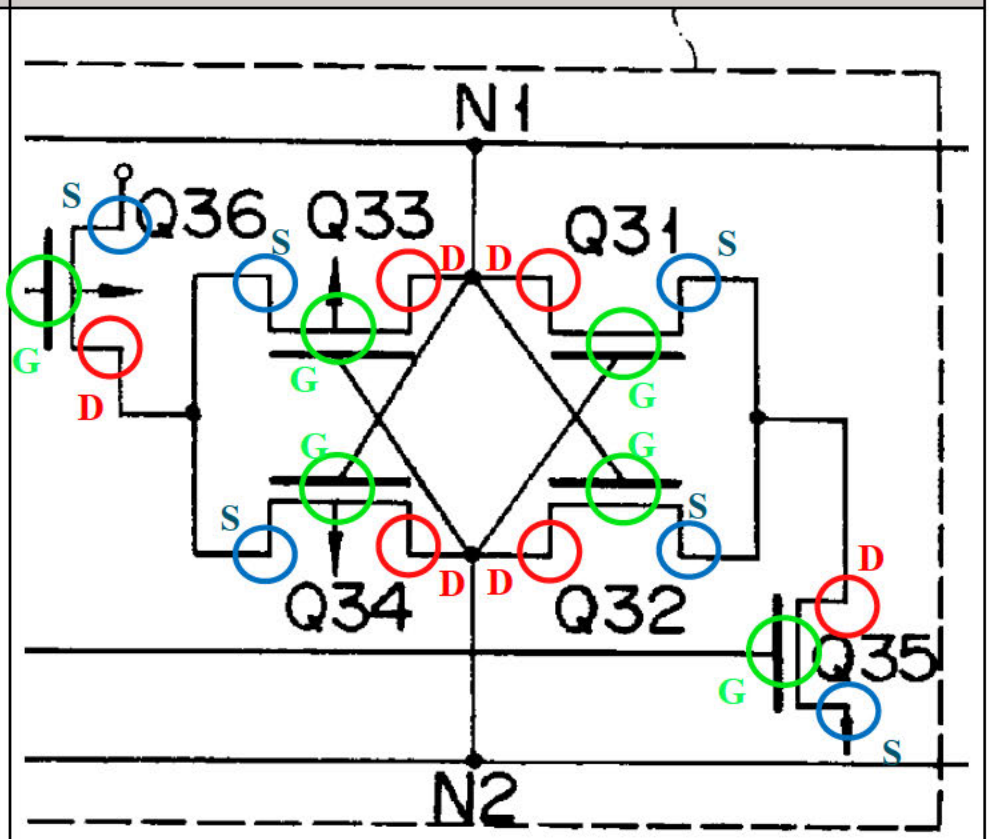
Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	invention of the '130 Patent would have understood that the gate, source, and drain of the input pass transistors are indicated as follows in annotated Fig. 7 of *Watanabe* (sources in blue circles; drains in red circles; gates in green circles)[1]:

[1] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the sources and drains for the input pass transistors is dependent on the voltage provided to the transistors from vout and $\overline{\text{vout}}$. Nonetheless, the identification of the sources and drains in annotated Fig. 7 of *Watanabe* is consistent with the '130 Patent's specification and identification of sources and drains for the claimed input pass transistors.

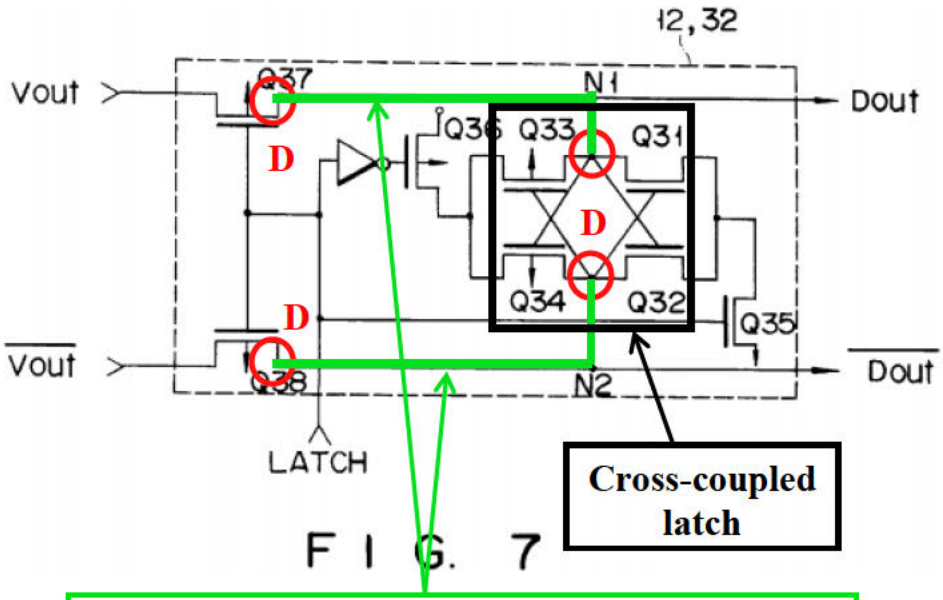
Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	 *Watanabe* discloses that Q37 and Q38 are pass transistors as "[t]he MOS transistors Q37 and Q38 are latch control elements. In operation, the p-channel MOS transistors Q37 and Q38 are turned on when the latch control signal LATCH falls to a low level, whereby the input data is transferred to the nodes N1 and N2 of the flip-flop. When the control signal

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	LATCH rises to a high level, the transistors Q37 and Q38 are turned off, whereby the nodes N1 and N2 are disconnected from the input lines, and the flip-flop is activated at the same to hold the data." *Watanabe* 4:22-30. In particular, Q37 and Q38 are pass transistors since they pass the voltages from vout and $\overline{\text{vout}}$ to nodes N1 and N2, respectively.
a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain;	*Watanabe* discloses a first stage of a latching sense amplifier comprising of a plurality of NMOS (e.g., NMOS transistors Q31, Q32, Q35) and PMOS transistors (e.g., PMOS transistors Q33, Q34, Q36) each having a gate, a source terminal, and a drain. *See, e.g.*, *Watanabe* Fig. 7 (annotated below).  FIG. 7 *Watanabe* discloses that "[t]he data latch circuit shown in FIG.

Claim Language	***Sukegawa*, *Lu*, and *Watanabe***
	7 comprises a pair of *three n-channel MOS transistors Q31, Q32 and Q35 and five p-channel MOS transistors Q33, Q34, Q36, Q37 and Q38*. The MOS transistors Q31, Q32, Q33 and Q34 constitute a flip-flop. The MOS transistors Q35 and Q36 are used to activate the flip-flop. The MOS transistors Q37 and Q38 are latch control elements." *Watanabe* 4:16-22 (emphasis added). One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the gate, source, and drain of the plurality of NMOS and PMOS transistors are indicated as follows in annotated Fig. 7 of *Watanabe* (sources in blue circles; drains in red circles; gates in green circles):

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	
wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled	*Watanabe* discloses a first stage of a latching sense amplifier wherein the drains of the input pass transistors (e.g., Q37, Q38) are coupled to the drains of the cross-coupled latch amplifier NMOS (e.g., NMOS transistors Q31, Q32) and PMOS transistors (e.g., PMOS transistors Q33, Q34). *See*, e.g., *Watanabe* Fig. 5 (annotated below; drains in red circles)[2]:

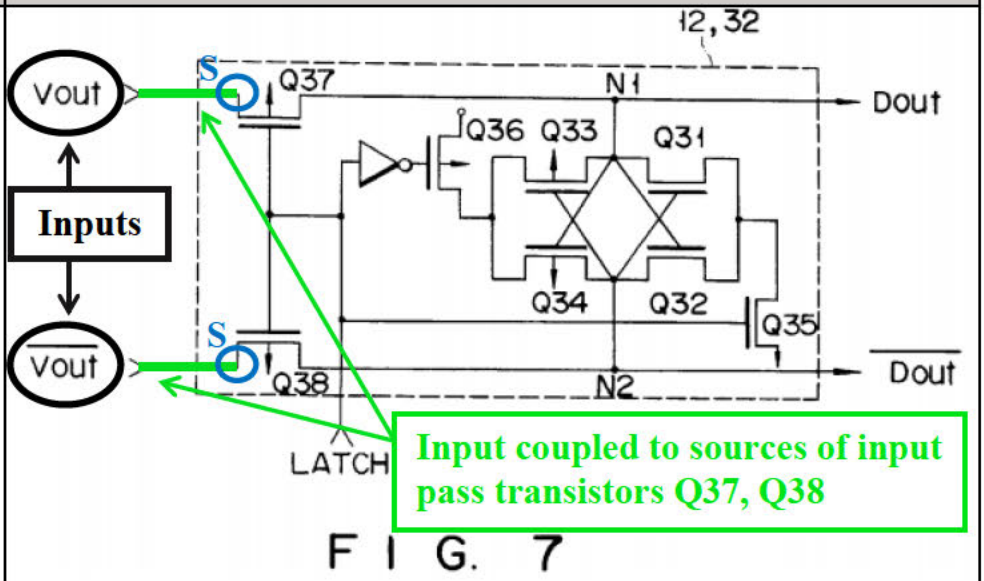
[2] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the drains for the input pass

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
latch amplifier NMOS and PMOS transistors,	 FIG. 7 *Watanabe* discloses that "[t]he MOS transistors Q37 and Q38 are latch control elements. In operation, the p-channel MOS transistors Q37 and Q38 are turned on when the latch control signal LATCH falls to a low level, whereby the input data is transferred to the nodes N1 and N2 of the flip-flop. When the

transistors is dependent on the voltage provided to the transistors from vout and $\overline{\text{vout}}$. Nonetheless, the identification of the drains in annotated Fig. 7 of *Watanabe* is consistent with the '130 Patent's specification and identification of drains for the claimed input pass transistors.

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	control signal LATCH rises to a high level, the transistors Q37 and Q38 are turned off, whereby the nodes N1 and N2 are disconnected from the input lines, and the flip-flop is activated at the same to hold the data." *Watanabe* 4:21-30. Transistors Q31, Q32, Q33, and Q34 are cross-coupled because the output of a first transistor (e.g., Q31) is tied to the input of a second transistor (e.g., Q32), and the output of the second transistor (e.g., Q32) is tied to the input of the first transistor (e.g., Q31). Likewise, the output of transistor Q33 is tied to the input of transistor Q34 and the output of transistor Q34 is tied to the input of transistor Q33.
each source terminal of the input pass transistors is	*Watanabe* discloses a first stage of a latching sense amplifier wherein each source terminal of the input pass transistors (e.g., Q37, Q38) is coupled to an input. *See, e.g.*, *Watanabe* Fig. 7 (annotated below; sources in blue circles), 4:13-16.[3]

[3] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the sources for the input pass transistors is dependent on the voltage provided to the transistors from vout

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
coupled to an input,	 F I G. 7
the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor	*Watanabe* discloses a first stage of a latching sense amplifier wherein the sources of the cross-coupled latch amplifier NMOS transistors (e.g., NMOS transistors Q31, Q32) are coupled to the drain of the NMOS transistor (e.g., NMOS transistor Q35) coupled to a clock signal input (e.g., LATCH). *See*, e.g., *Watanabe* Fig. 7 (annotated below; sources in blue circles; drains in red circles):

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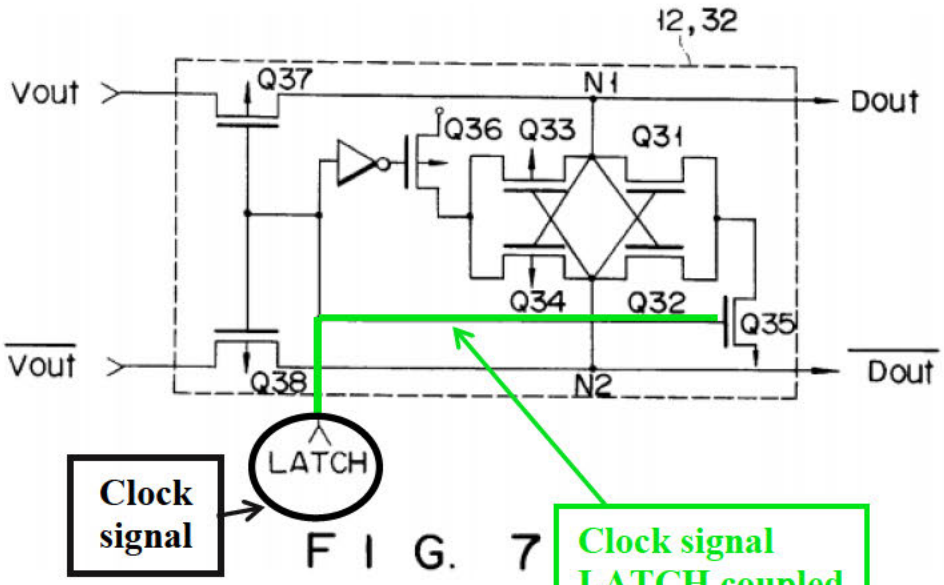
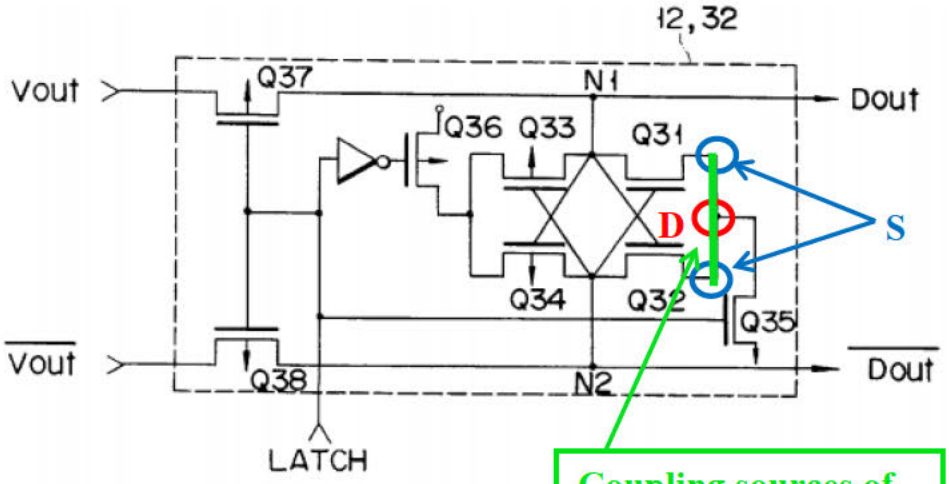
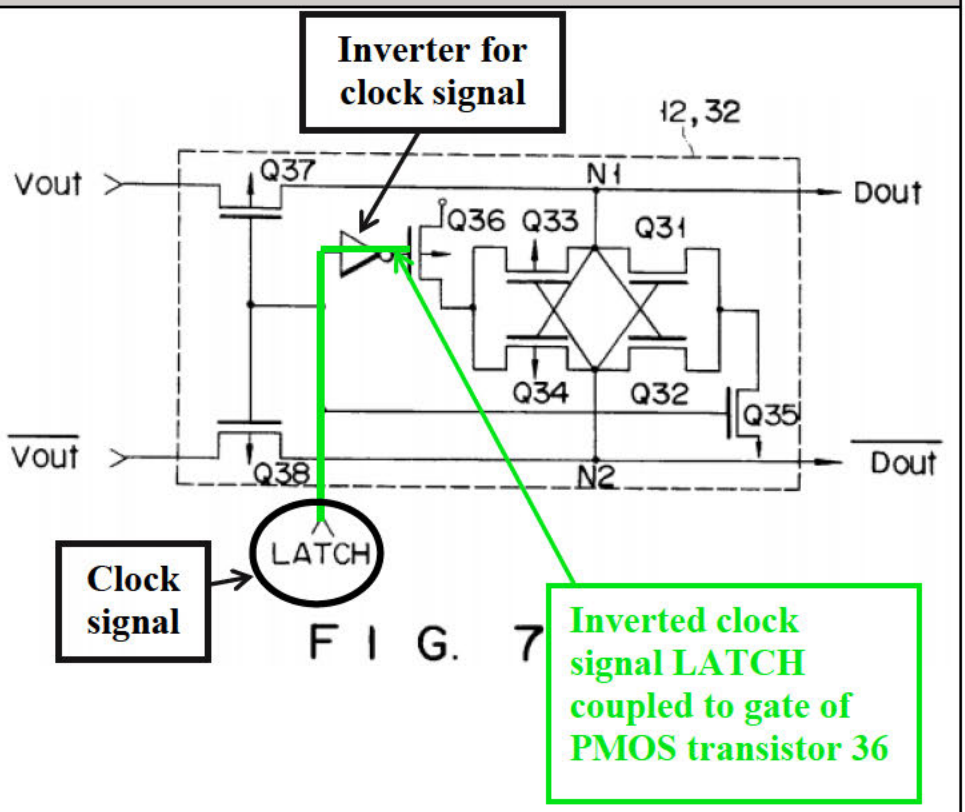
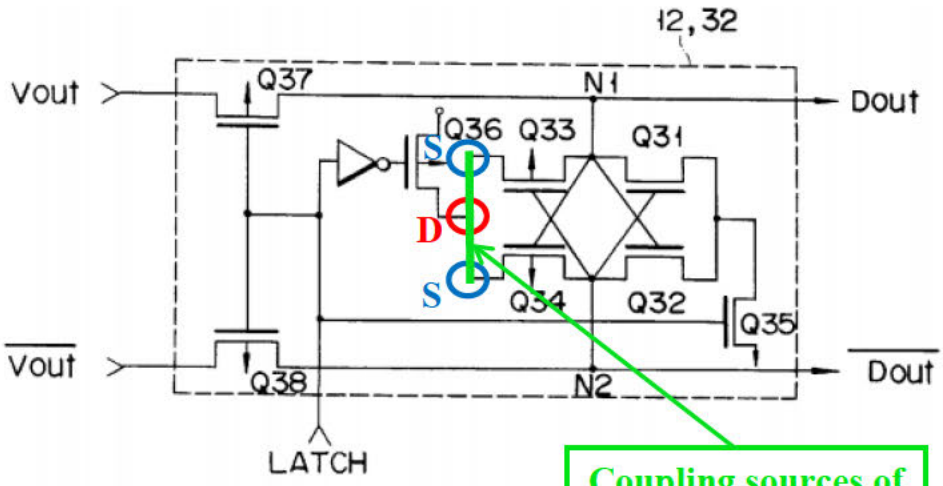
and $\overline{\text{vout}}$. Nonetheless, the identification of the sources in annotated Fig. 7 of *Watanabe* is consistent with the '130 Patent's specification and identification of sources for the claimed input pass transistors.

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
coupled to a clock signal input, and	 F I G. 7  F I G. 7 *Watanabe* further discloses that "[i]n operation, the p-channel

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	MOS transistors Q37 and Q38 are turned on when the latch control signal LATCH falls to a low level, where by the input data is transferred to the nodes N1 and N2 of the flip-flop. When the control signal LATCH rises to a high level, the transistors Q37 and Q38 are turned off, whereby the nodes N1 and N2 are disconnected from the input lines, and the flip-flop is activated at the same to hold the data." *Watanabe* 4:23-30.
the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input.	*Watanabe* discloses a first stage of a latching sense amplifier wherein the sources of the PMOS transistors (e.g., PMOS transistors Q33, Q34) are coupled to the drain of the PMOS transistor (e.g., PMOS transistor Q36) having a gate coupled to an inverted clock signal input. *See*, e.g., *Watanabe* Fig. 7 (annotated below; sources in blue circles; drains in red circles): circles):

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*
	 F I G. 7

Claim Language	*Sukegawa*, *Lu*, and *Watanabe*



F I G. 7

Coupling sources of PMOS transistors in cross-coupled latch amplifier with drain of PMOS transistor Q36

Watanabe further discloses that "[i]n operation, the p-channel MOS transistors Q37 and Q38 are turned on when the latch control signal LATCH falls to a low level, where by the input data is transferred to the nodes N1 and N2 of the flip-flop. When the control signal LATCH rises to a high level, the transistors Q37 and Q38 are turned off, whereby the nodes N1 and N2 are disconnected from the input lines, and the flip-flop is activated at the same to hold the data." *Watanabe* 4:23-30.

3. *Sukegawa, Lu,* and *Hardee* Disclose or Suggest the Features of Claim 7

38. In my opinion, *Sukegawa*, *Lu*, and *Hardee* disclose or suggest each and every feature recited in claim 7, which is reproduced below:

> ***The data transfer arrangement in accordance with claim 2 wherein the active pull up and pull down bus drivers are NMOS transistors.***

39. As I discussed above in connection with claim 2, *Sukegawa* and *Lu* disclose a data transfer arrangement with active pull up and active pull down bus drivers. *See, e.g., Sukegawa* Fig. 1, 8:11-23; *supra* Section VI.B.1.b. *Sukegawa* and *Lu* disclose that the active pull up and pull down bus drivers comprise of both NMOS and PMOS transistors. *See, e.g.*, *Sukegawa* Fig. 1, 8:11-23; *supra* Section VI.B.1.b. However, one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have modified *Sukegawa* and *Lu* so that the active pull up and pull down bus drivers comprised entirely of NMOS transistors.

40. It was well known at the time of the alleged invention of the ’130 Patent that active pull up and active pull down bus drivers could be designed with solely NMOS transistors. For example, Fig. 5 of *Hardee* discloses NMOS active pull up and pull down drivers:

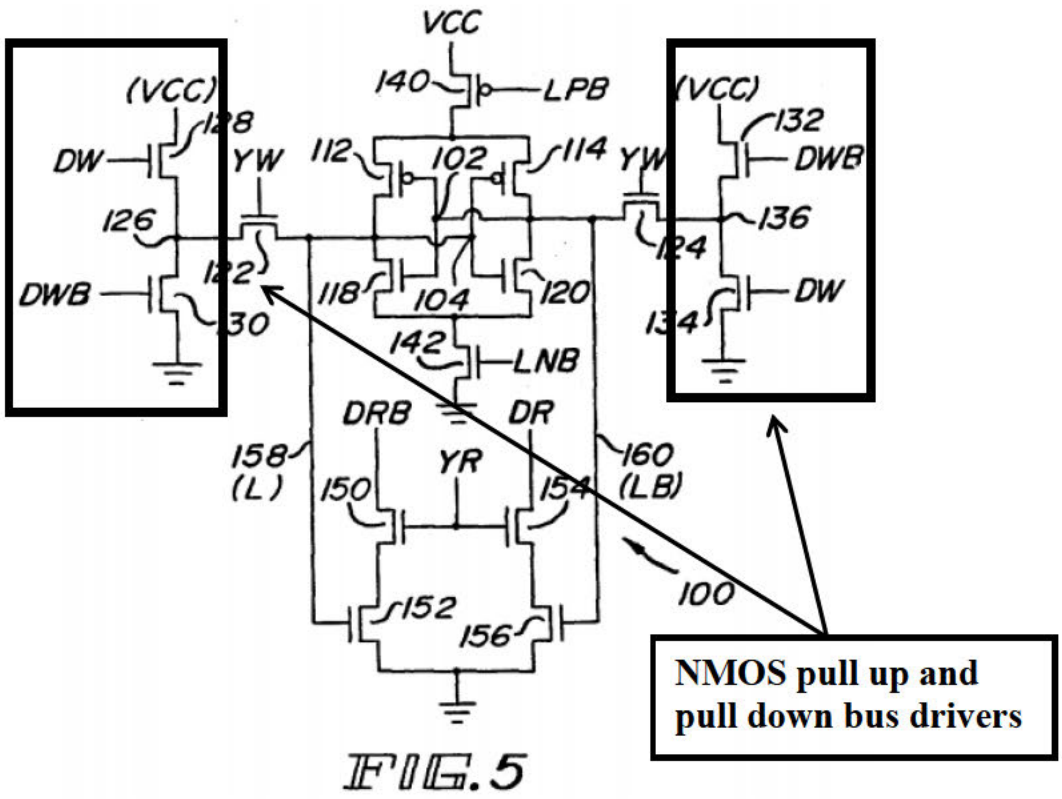


FIG. 5

Hardee discloses:

> *Transistors 128 and 130 are N channel devices* having their source-drain paths coupled in series. The drain of transistor 128 is coupled to VCC and the source of transistor 130 is coupled to ground. A data write signal DW is coupled to the gate electrode of transistor 128 and its complement DWB is coupled to the gate electrode of transistor 130. A similar configuration exists on the right side of sense amplifier 100 where transistors 132 and 134 are coupled between VCC and ground and have a node 136 there between which is coupled to transistor 124. Note, however, that the data write signal DW is coupled to control transistor 134 whereas its complement DWB is

> coupled to the gate electrode of transistor 132. That is to say, the data write signal DW turns on a *pull-up transistor 128* on the left side of the sense amplifier 100, but turns on a *pull down transistor 134* on the right side of sense amplifier 100. Its complementary signal DWB likewise has reciprocal effects on the left and right sides."

Hardee 6:28-46 (emphasis added).

41. Given the teachings of *Hardee*, which like *Sukegawa* and *Lu* is also concerned with signal transmission and improving the efficiency of such transmissions, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to reconfigure the circuit of *Sukegawa* and *Lu* to include NMOS pull up and pull down bus drivers. One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have done so in order to reduce the layout area and avoid latch-up. The use of only NMOS transistors in the driver eliminates the need for the n-well used in the construction of PMOS transistors and thus reduces the layout size. Small layout size can be important when connecting the drivers up to an array of transistors, as used in a memory, or driving a parallel data bus where the data signals are laid out directly adjacent to each other. Further, by eliminating the PMOS device, the driver becomes immune to latch-up. Latch-up causes a wire to short to the power supply Vdd (or Vcc) or ground. Avoiding latch-up is especially important when driving a

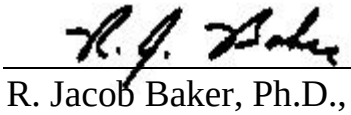
signal off-chip where the driver is connected to a bonding wire which is inductive and thus can produce ringing voltages.

42. Further, in my opinion, implementing pull up and pull down bus drivers using solely NMOS transistors in *Sukegawa* and *Lu* is simply a design choice that one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have certainly understood. This follows from the fact that there were a small finite number of MOSFET configurations for implementing pull up and pull down bus drivers (e.g., NMOS, PMOS, or CMOS – both NMOS and PMOS). In fact, this change would have amounted to nothing more than applying known techniques to improve similar devices in the same way to yield predictable results.

VII. CONCLUSION

43. In summary, it is my opinion that certain references disclose or suggest all of the features recited in the challenged claims of the '130 Patent.

44. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 26, 2015 By: 

R. Jacob Baker, Ph.D., P.E.

DECLARATION OF DR. R. JACOB BAKER

APPENDIX A

R. JACOB (JAKE) BAKER, PH.D., P.E.

Professor of Electrical and Computer Engineering
University of Nevada, Las Vegas
Department of Electrical and Computer Engineering
Box 454026 • 4505 S. Maryland Parkway
Las Vegas, Nevada 89154-4026

(702) 895-4125 (office)

Email: rjacobbaker@gmail.com
Website: http://CMOSedu.com/jbaker/jbaker.htm

SUMMARY

- Extensive leadership experience including:
  - Chair, Electrical and Computer Engineering Department, Boise State University;
  - Dealing with conflict, problems, and limited resources;
  - Leading the department through ABET accreditation;
  - Creation and implementation of both Master and Doctoral programs in ECE.
- Active scholar (h-index > 30 and an i10-index > 90) whose research is focused on:
  - High-speed interfaces for electro-optic, mixed-signal, and analog integrated circuits;
  - Design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide);
  - Analog and mixed-signal circuit techniques for nanometer CMOS; 3D packaging techniques
  - The design of instrumentation for scientific research
  - Delivery of circuit design education to off-campus students/engineers via the Internet.
- Mentor to:
  - Approximately 75 graduate students (major professor), http://CMOSedu.com/jbaker/students/students.htm
  - Electrical and Computer Engineering Department faculty;
  - Engineers locally, nationally, and internationally;
  - New and established companies.
- Inventor with 137 granted US patents
- Experienced integrated circuit designer and educator with significant industry experience. See additional information at http://cmosedu.com/jbaker/projects/fund.htm
- Textbook authorship and Internet contributions (see http://CMOSedu.com), that have helped tens of thousands of engineers around the world.
- Recognized by the IEEE Power Electronics Society with the Best Paper Award in 2000 (*IEEE Transactions on Power Electronics*) from PhD dissertation work.
- International known in the field of integrated circuit design, recipient of many honors including the Terman Award, the IEEE CAS Education Award, and IEEE Fellow.

EDUCATION

Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*

M.S. and B.S. in Electrical Engineering: May 1986 and 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

ACADEMIC EXPERIENCE

January 1991 - Present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, and the Air Force Research Lab.
- Current research interests are:
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories
  - Analog and mixed-signal circuit design for communication systems, synchronization, energy storage, and data conversion
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
  - Reconfigurable electronics design using nascent memory technologies
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Methods to deliver circuit design education to industry and off-campus students, see videos here
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

INDUSTRIAL EXPERIENCE

2013 - present: Working with Freedom Photonics and Attolo Engineering in the Santa Barbara area on the integration of optics with CMOS integrated circuits including Avalanche Photodiodes. Work has resulted, and should continue to result in, support via the SBIR and STTR programs.

2013 - present: Working with National Security Technologies, LLC,) on the Design of Integrated electrical/photonic application specific integrated circuit (ASIC) design.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors with memory for very high-speed consumer imager products.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (now Oracle) VLSI research group. Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power and 3D packaging.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project between Micron and HP labs in magnetic memory using the MJT memory cell. Worked on numerous projects (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line.

Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging.

Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing (35 nm technology node).

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1998: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns risetime and 8 ns falltime for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble shooting electric motors on mining equipment.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services are listed below. I have been deposed eight times and given testimony at one trial.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for *SK hynix*, Inc. on matters relating to investigation of certain patents owned by Longitude Licensing Ltd.
Case Subject Matter – Semiconductor random access memory and communication interfaces.
Work Performed – Provided expert consulting services in 2015.

Ropes & Gray LLP (New York City, NY)

Case – *Samsung, Inc.* v. Imperium IP Holdings (Cayman), Ltd.
Case Number – IPR2015-01233. Filed on May 21, 2015.
Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – *Silergy Corporation* v. Monolithic Power Systems, Inc.
Case Numbers – IPR2015-00803 and IPR2015-00804. Filed on February 24, 2015.
Case Subject Matter – Microelectronic packaging.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Jones Day LLP (San Diego, CA)

Case – *Micron Technology, Inc.* v. eDigital Corp.
Case Number - IPR2015-00519. Filed on December 31, 2014.
Case Subject Matter – Methods for memory management in non-volatile flash memories.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (Atlanta, GA and Washington, DC)

Case – *Micron Technology, Inc.* v. MLC Intellectual Properties and BTG USA/International Inc.
Case Number - IPR2015-00504. Filed on December 24, 2014.
Case Subject Matter – Multi-level non-volatile floating gate memory, e.g. EPROM, EEPROM, and flash technologies.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Skadden, Arps, Slate, Meagher & Flom LLP & Affiliates (Palo Alto, CA)

Case – ALFRED T. GIULIANO, Chapter 7 Trustee of the Ritz Estate; CPM ELECTRONICS INC.; E.S.E. ELECTRONICS, INC. and MFLASH, INC., on Behalf of Themselves and All Others Similarly Situated v. *SanDisk Corp.*
Case Number – California, ND (Oakland) 4:10-cv-02787. Fourth amended complaint filed on September 24, 2014.
Case Subject Matter – Non-volatile semiconductor flash memory.
Work Performed – Provided expert consulting services.

Ropes & Gray LLP (East Palo Alto, CA, New York City, NY, and Washington, DC)

Case – Macronix International Co., Ltd. v. *Spansion, Inc.*, *Aerohive Networks*, *Allied Telesis*, *Ciena*, *Delphi Automotive*, *Polycom*, *Ruckus Wireless*, *ShoreTel*, *Tellabs*, and *TiVo*
Case Number – ITC Investigation No. 337-TA-922. Complaint filed on June 27, 2014.
Case Subject Matter – Devices containing non-volatile memory and products containing the same.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, Markman tutorial, and expert report.

Quinn Emanuel Urquhart & Sullivan, LLP (San Francisco, CA and Washington, DC)

Case – Freescale Semiconductor, Inc. v. *MediaTek, Inc.*, et. al.
Case Number – ITC Investigation No. 337-TA-920. Amended complaint filed on May 27, 2014.
Case Subject Matter – Semiconductor integrated circuits and devices containing the same.
Work Performed – Provided expert consulting services.

DLA Piper (East Palo Alto and San Diego, CA)

Case – *GSI Technology, Inc.* v. Cypress Semiconductor Corporation
Case Number – IPR2014-00419. Filed on February 7, 2014.
Case Subject Matter – Semiconductor static random access memory (SRAM) circuit design.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Ropes & Gray LLP (Washington, DC)

Case – Macronix International Co., Ltd. v. *Spansion, Inc.*, et al.
Case Number – Virginia, ED 3:13-cv-00679. Complaint filed on November 20, 2013.
Case Subject Matter – Non-volatile semiconductor flash memory.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Cooley LLP (San Diego, CA)

Case – HSM Portfolio LLC and Technology Properties Limited LLC v. Fujitsu, AMD, *Qualcomm, Inc.*, Elpida, SK Hynix, Micron, ProMOS, SanDisk, Sony, ST Micro, Toshiba, ON, and Zoran
Case Number – Delaware, 1:11-cv-00770. Third amended complaint filed on June 28, 2013.
Case Subject Matter – Semiconductor sensing circuits.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto and San Diego, CA)

Case – Cypress Semiconductor Corporation v. *GSI Technology, Inc.*
Case Number – California, ND 3:13-cv-02013. Complaint filed on May 1, 2013.
Case Subject Matter – Semiconductor static random access memory (SRAM) circuit design.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, and invalidity analysis.

Montgomery McCracken Walker & Rhoads LLP (Philadelphia, PA)

Case – Simon Nicholas Richmond v. Winchance Solar Fujian Technology, *Target*, *Creative Industries*, et. al.
Case Number – New Jersey, 3:13-cv-01954. Amended complaint filed on March 27, 2013.
Case Subject Matter – Circuitry including solar cells, re-chargeable batteries, energy conversion for solar lighting.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto, CA)

Case – Intellectual Ventures I/II LLC v. *Toshiba, Inc.*
Case Number – Delaware, 1:13-cv-00453. Complaint filed on March 20, 2013.
Case Subject Matter – Semiconductor memory and interface circuits.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Alston & Bird, DLA Piper, Gibson Dunn, Katten, O'Melveny, Orrick, and WilmerHale (various locations in the USA)

Case – Freescale v. *Funai*, *CSR*, *Zoran*, *MediaTek*, *Vizio*, *Sanyo*, *TPF*, *Top Victory Electronics*, *Envision Peripherals*, *AmTRAN*, and *Marvell*
Case Number – Texas, WD 1:12-cv-00644. Amended complaint filed on January 14, 2013.
Case Subject Matter – Semiconductor circuitry for voltage regulators, bus terminations, packaging, and signal processing.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, and Markman tutorial.

Amin, Turocy & Watson LLP (San Jose and San Francisco, CA)

Case – *InvenSense, Inc.* v. Robert Bosch GmbH
Case Subject Matter – Microelectromechanical systems (MEMS) sensor design and manufacture.
Work Performed – Provided expert consulting services in 2013.

Morrison & Foerster LLP (Los Angeles, Palo Alto, and San Francisco, CA)

Case – STMicroelectronics, Inc. v. *InvenSense, Inc.*
Case Number – California, ND 3:12-cv-02475. Complaint filed on May 16, 2012.
Case Subject Matter – Microelectromechanical systems (MEMS) sensors including Gyroscopes and accelerometers.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for *SK hynix*, Inc. on matters relating to investigation of certain patents owned by Round Rock Research LLC
Case Subject Matter – Semiconductor random access memory.
Work Performed – Provided expert consulting services in 2012.

Keker & Van Nest LLP (San Francisco, CA)

Case – Round Rock Research LLC v. *SanDisk Corp.*
Case Number – Delaware, 1:12-cv-00569. Complaint filed on May 3, 2012.

Case Subject Matter – Semiconductor non-volatile flash memory.
Work Performed – Provided expert consulting including: invalidity analysis, non-infringement analysis, expert reports, and was deposed.

Perkins Coie LLP (San Diego, CA)
Case – *ASUS Computer International* v. Round Rock Research LLC
Case Number – California, ND 3:12-cv-02099. Complaint filed on April 26, 2012.
Case Subject Matter – Semiconductor memory and image sensors.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, expert reports, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)
Case – Dr. Michael Jaffe' as insolvency administrator for Qimonda AG v. LSI, *Atmel Corp*, Cypress, MagnaChip, and ON Semiconductor
Case Number – California, ND 3:12-cv-03166. Complaint filed on January 10, 2012.
Case Subject Matter – Semiconductor processing and manufacturing.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Useful Arts IP (Cupertino, CA)
Case – Tezzaron (formerly Tachyon Semiconductor) v. *Elm Technology Corporation*
Case Number – Patent Interference No. 105,859. Declared on December 1, 2011.
Case Subject Matter – Packaging of semiconductors and through semiconductor vias.
Work Performed – Patent interference, wrote declaration, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)
Case – Nanya Technology Corporation v. *Elpida Memory, Inc. and Kingston Technology Company, Inc.*
Case Number – ITC Investigation No. 337-TA-821. Complaint filed on November 21, 2011.
Case Subject Matter – Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting and reports on validity, infringement, and domestic industry. Also provided declarations and was deposed.

Morgan, Lewis & Bockius LLP (Washington, DC)
Case – *Elpida Memory, Inc.* v. Nanya Technology Corporation
Case Number – ITC Investigation No. 337-TA-819. Complaint filed on November 15, 2011.
Case Subject Matter – Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting and reports on infringement, domestic industry, and validity. Also provided Markman tutorial, declarations, deposition, and testimony at the trial.

Ropes & Gray LLP (New York City, NY)
Case – Intellectual Ventures v. *Sendai Nikon Corporation*
Case Number – Delaware, 1:11-cv-01025. Complaint filed on October 26. 2011.
Case Subject Matter – Image sensor design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Farella Braun + Martel LLP (San Francisco, CA)
Case – Round Rock Research LLC v. *Dell, Inc.*
Case Number – Delaware, 1:11-cv-00976. Complaint filed on October 14, 2011.
Case Subject Matter – Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Latham & Watkins LLP (San Francisco, CA)

Case – Altera Corp. v. *LSI Corp. and Agere Systems, Inc.*
Case Number – California, ND 4:11-cv-03139. Complaint filed on June 24, 2011.
Case Subject Matter – Semiconductor devices including phase-locked loops and clock recovery circuits.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Fish & Richardson P.C. (Washington, DC)

Case – Spansion LLC v. *Samsung Electronics Co., Ltd.*, Apple, Inc., Nokia Corp., PNY Technologies, Inc. Research In Motion Corporation, Transcend Information Inc.
Case Number – ITC Investigation No. 337-TA-735. Complaint filed on August 6, 2010.
Case Subject Matter – Semiconductor flash memory manufacture and design.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Jones Day LLP (Palo Alto, CA)

Case – LSI and Agere, Inc. v. *Xilinx, Inc.*
Case Number – New York, SD 1:09-cv-09719. Complaint filed on November 23, 2009.
Case Subject Matter – Semiconductor digital design and clocking.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Morrison & Foerster LLP (New York City, NY)

Case – Innurvation, Inc. et al v. *Fujitsu Microelectronics America, Inc.*, Sony Corporation of America, Toshiba America Electronics Components, Inc., and Freescale Semiconductor, Inc.
Case Number – Maryland, 1:09-cv-01416. Complaint filed on May 29, 2009.
Case Subject Matter – Semiconductor circuit layout.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Wilson Sonsini Goodrich & Rosati P.C. (Palo Alto, CA)

Case – Panavision Imaging, LLC, v. *OmniVision Technologies, Inc.*, Canon U.S.A., Inc., Micron Technology, Inc., Aptina Imaging Corporation, and Aptina, LLC.
Case Number – California, CD 2:09-cv-01577. Complaint filed on March 6, 2009.
Case Subject Matter – CMOS image sensor design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and wrote declaration.

McDermott Will & Emery (Menlo Park, CA)

Case – Volterra Semiconductor Corp. v. Primarion *& Infineon Technologies North America & Infineon Technologies, A.G.*
Case Number – California, ND 3:08-cv-05129. Complaint filed on November 12, 2008.
Case Subject Matter – High-performance analog and mixed-signal power management semiconductors.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and was deposed.

pre-2008 Miscellaneous minor expert witness work, was deposed twice.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013 - 2015
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2013 - 2014
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- Elevated to Senior member of the IEEE, 1997
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Masters graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-present), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as the Technology Editor (2012-2014) and Editor-in-Chief (2015 - present) for the *IEEE Solid-State Circuits Magazine*, as a Distinguished Lecturer for the SSCS (2013-2014), and as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015.

ARMED FORCES

6 years United States Marine Corps reserves (Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge, October 23, 1987

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition" *Wiley-IEEE*, 1174 pages. ISBN 978-0470881323 (2010) **Over 50,000 copies of this book's three editions in print.**

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 978-0471227540 (first edition, 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 978-0-470-18475-2

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0-7803-6014-1

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 978-0780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 1999. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 1999. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

INVITED TALKS AND SEMINARS

Have given invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICySSS keynote, IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2015) "Radiation Hardened Optoelectronics for Optical Interconnects," Electronics Defense Threat Reduction Agency (DTRA), $45,000 **submitted for funding**
- Baker, R. Jacob, (2015) "Low Light Short Wave Infrared Focal Plane Arrays," Missile Defense Agency (MDA), $44,999 **submitted for funding**
- Baker, R. Jacob, (2015) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665 **submitted for funding**
- Baker, R. Jacob, (2015-2016) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $45,000
- Baker, R. Jacob, (2015) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $45,000
- Baker, R. Jacob, (2014-2015) "NSTec ASIC Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, $90,000
- Baker, R. J., (2014-2015) "Silicon Photonic-Electronic System Level Integration," U.S. Air Force/DOD, $54,607
- Baker, R. Jacob, (2013-2014) "NSTec ASIC Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, $162,074
- Baker, R. Jacob, (2013) "Design Software Setup," Department of Energy, National Security Technologies, LLC, $10,999
- Campbell, K. A. and Baker, R. J., (2009-2012) "Reconfigurable Electronics and Non-Volatile Memory Research" funded by the Air Force Research Laboratory, $2,790,081
- Baker, R. J., (2010-2012) "Dual Well Focal Plane Array (FPA) Sensor," U.S. Navy, $31,500
- Baker, R. J., (2011) "Readout-Integrated Circuit (ROIC) Development in Support of Corrugated Quantum Well Infrared Photo-detector (C-QWIP) Focal Plane Arrays (FPA) for Tactical Applications," U.S. Army, $27,000
- Baker, R. J., (2011) "Monolithic CMOS LADAR Focal Plane Array (FPA) with a Photonic High-Speed Output Interface," U.S. Air Force/DOD, $50,002
- Campbell, K. A., Baker, R. J., Peloquin, J., and Teasdale, J. (2008-2010) "Radiation Resistant Phase Change Memory and Reconfigurable Electronics," NASA. $1,500,000
- Campbell, K. A., Baker, R. J., Peloquin, J., and Teasdale, J. (2007) "Reliability Investigations of Radiation Resistant, Multi-State Phase-Change Memory," NASA. $726,768
- Baker, R. J., et. al., (2006-2010) "Establishment of a Doctoral Degree Program in Electrical and Computer Engineering in Electrical and Computer Engineering," Micron Foundation. $5,000,000
- Baker, R. J., (2005-2006) "Advanced Processing Techniques for Fabrication of 3-D Microstructures for Future Electronic Devices," DARPA, N66001-01-C-8034, $125,000
- Baker, R. J., (2004-2005) "Multi-Purpose Sensors for Detection and Analysis of Contaminants" EPA, X-97031102, $75,000
- Baker, R. J., (2001-2006) Multi-University Research Initiative (MURI), "The effects of radio frequency pulses on electronic circuits and systems," Air Force Research Laboratory, $350,000.

GRANTED US PATENTS

137. Baker, R. J., "Reference current sources," **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,878,274**, November 4, 2014.
135. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,854,899**, October 7, 2014.
134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.

132. Baker, R. J., “Methods of quantizing signals using variable reference signals,” **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **8,712,249**, April 29, 2014.
130. Baker, R. J., “Resistive memory element sensing using averaging,” **8,711,605**, April 29, 2014.
129. Baker, R. J., “Memory with correlated resistance,” **8,681,557**, March 25, 2014.
128. Baker, R. J., “Reference current sources,” **8,675,413**, March 18, 2014.
127. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougal, M., Geske, J., and Baker, R. J., “Dual well read-out integrated circuit (ROIC),” **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, “Resistive memory element sensing using averaging,” **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, “Memory with correlated resistance,” **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, “Phase splitter using digital delay locked loops,” **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, “Subtraction circuits and digital-to-analog converters for semiconductor devices,” **8,194,477**, June 5, 2012.
119. Baker, R. J., “Digital Filters for Semiconductor Devices,” **8,149,646**, April 3, 2012.
118. Baker, R. J., “Error detection for multi-bit memory,” **8,117,520**, February 14, 2012.
117. Baker, R. J., “Integrators for delta-sigma modulators,” **8,102,295**, January 24, 2012.
116. Baker, R. J., “Devices including analog-to-digital converters for internal storage locations,” **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., “Multi-resistive integrated circuit memory,” **8,093,643**, January 10, 2012.
114. Baker, R. J., “Quantizing circuits with variable parameters,” **8,089,387**, January 3, 2012.
113. Baker, R. J., “Reference current sources,” **8,068,367**, November 29, 2011.
112. Baker, R. J., “Methods of quantizing signals using variable reference signals,” **8,068,046**, November 29, 2011.
111. Baker, R. J., “Systems and devices including memory with built-in self test and methods of making using the same,” **8,042,012**, October 18, 2011.
110. Baker, R. J., “Memory with correlated resistance,” **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **7,941,056**, May 10, 2011.
108. Baker, R. J., “K-delta-1-sigma modulator,” **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., “Phase splitter using digital delay locked loops,” **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., “Complementary bit PCRAM sense amplifier and method of operation,” **7,869,249**, January 11, 2011.
104. Baker, R. J., “Subtraction circuits and digital-to-analog converters for semiconductor devices,” **7,839,703**, November 23, 2010.
103. Baker, R. J., “Digital Filters with Memory” **7,830,729**, November 9, 2010.
102. Baker, R. J., “Systems and devices including memory with built-in self test and methods of making using the same,” **7,818,638**, October 19, 2010.

101. Baker, R. J., “Integrators for delta-sigma modulators,” **7,817,073**, October 19, 2010.
100. Baker, R. J., “Digital filters for semiconductor devices,” **7,768,868**, August 3, 2010.
99. Baker, R. J., “Quantizing circuits with variable reference signals,” **7,733,262**, June 8, 2010.
98. Baker, R. J., “Quantizing circuits for semiconductor devices,” **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., “Multi-resistive integrated circuit memory,” **7,642,591**, January 5, 2010.
96. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **7,616,474**, November 10, 2009.
95. Baker, R. J., “Resistive memory element sensing using averaging,” **7,577,044**, Aug. 18, 2009.
94. Baker, R. J., “Quantizing circuits with variable parameters,” **7,538,702**, May 26, 2009.
93. Baker, R. J., “Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors,” **7,528,877**, May 5, 2009.
92. Baker, R. J., “Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors,” **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., “Method and apparatus for sensing flash memory using delta-sigma modulation,” **7,495,964**, February 24, 2009.
90. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **7,489,575**, February 10, 2009.
89. Baker, R. J., “Per column one-bit ADC for image sensors,” **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., “Input buffer design using common-mode feedback,” **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **7,421,607**, September 2, 2008.
86. Baker, R. J., “Methods for resistive memory element sensing using averaging,” **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., “Method and apparatus for sensing flash memory using delta-sigma modulation,” **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., “Method of operating a complementary bit resistance memory sensor and method of operation,” **7,366,003**, April 29, 2008.
83. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **7,330,390**, February 12, 2008.
82. Baker, R. J., “Input and output buffers having symmetrical operating characteristics and immunity from voltage variations,” **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., “Method and apparatus providing input buffer design using common-mode feedback,” **7,310,018**, December 18, 2007.
80. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., “Method and apparatus for reducing duty cycle distortion of an output signal,” **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., “Method and apparatus for reducing duty cycle distortion of an output signal,” **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., “Skewed sense AMP for variable resistance memory sensing,” **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., “Method of operating a complementary bit resistance memory sensor,” **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., “Rewrite prevention in a variable resistance memory,” **7,224,632**, May 29, 2007.

73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.
66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.
62. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **6,985,375**, January 10, 2006.
61. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,954,392**, October 11, 2005.
60. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,391**, October 11, 2005.
59. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **6,950,487**, September 27, 2005.
57. Baker, R. J., "Method and apparatus for measuring current as in sensing a memory cell," **6,930,942**, August 16, 2005.
56. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,917,534**, July 12, 2005.
55. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,914,838**, July 5, 2005.
54. Baker, R. J., "High speed low power input buffer," **6,914,454**, July 5, 2005.
53. Baker, R. J., and Beigel, K. D., "Method for stabilizing or offsetting voltage in an integrated circuit," **6,913,966**, July 5, 2005.
52. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,909,656**, June 21, 2005.
51. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,901,020**, May 31, 2005.
50. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **6,888,771**, May 3, 2005.
49. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory,"**6,885,580**, April 26, 2005.
48. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,882,578**, April 19, 2005.
47. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,870,784**, March 22, 2005.

46. Baker, R. J., “Sensing method and apparatus for a resistive memory device,” **6,859,383**, February 22, 2005.
45. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,856,564**, February 15, 2005.
44. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **6,856,532**, February 15, 2005.
43. Baker, R. J., “Dual loop sensing scheme for resistive memory elements,” **6,829,188**, Dec. 7, 2004.
42. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,826,102**, Nov. 30, 2004.
41. Baker, R. J., “Resistive memory element sensing using averaging,” **6,822,892**, Nov. 23, 2004.
40. Baker, R. J., “System and method for sensing data stored in a resistive memory element using one bit of a digital count,” **6,813,208**, Nov. 2, 2004.
39. Baker, R. J., “Wordline driven method for sensing data in a resistive memory array,” **6,809,981**, Oct. 26, 2004.
38. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,798,705**, Sept. 28, 2004.
37. Baker, R. J., “Methods and apparatus for measuring current as in sensing a memory cell,” **6,795,359**, Sept. 21, 2004.
36. Hush, G. and Baker, R. J., “Complementary bit PCRAM sense amplifier and method of operation,” **6,791,859**, Sept. 14, 2004.
35. Baker, R. J., “Method and apparatus for sensing resistance values of memory cells,” **6,785,156**, August 31, 2004.
34. Lin, F. and Baker, R. J., “Phase detector for all-digital phase locked and delay locked loops,” **6,779,126**, August 17, 2004.
33. Baker, R. J., and Lin, F. "Digital dual-loop DLL design using coarse and fine loops," **6,774,690**, August 10, 2004.
32. Hush, G., Baker, R. J., and Voshell, T., “Producing walking one pattern in shift register,” **6,771,249**, August 3, 2004.
31. Baker, R. J., “Sensing method and apparatus for resistance memory device,” **6,741,490**, May 25, 2004.
30. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **6,704,881**, March 9, 2004.
29. Baker, R. J., “Method and system for writing data in an MRAM memory device,” **6,687,179**, February 3, 2004.
28. Baker, R. J., “High speed digital signal buffer and method,” **6,683,475**, January 27, 2004.
27. Baker, R. J., “High speed low power input buffer,” **6,600,343**, July 29, 2003.
26. Baker, R. J., “Offset compensated sensing for magnetic random access memory,” **6,597,600**, July 22, 2003.
25. Baker, R. J., “Sensing method and apparatus for resistive memory device,” **6,577,525**, June 10, 2003.
24. Baker, R. J., “Method and apparatus for sensing resistance values of memory cells,” **6,567,297**, May 20, 2003.
23. Baker, R. J., “High-speed digital signal buffer and method,” **6,538,473**, March 25, 2003.
22. Baker, R. J. and Beigel, K. D., "Electronic device with interleaved portions for use in integrated circuits," **6,509,245**, January 21, 2003.
21. Baker, R. J., "Resistive memory element sensing using averaging," **6,504,750**, January 7, 2003.
20. Baker, R. J., "High-speed digital signal buffer and method," **6,483,347**, November 19, 2002.
19. Baker, R. J., and Lin, F., "Digital dual-loop DLL design using coarse and fine loops," **6,445,231**, September 3, 2002.

18. Baker, R. J., "Method and apparatus for receiving synchronous data," **6,424,684**, July 23, 2002.
17. Baker, R. J. and Beigel, K. D., "Comb-shaped capacitor for use in integrated circuits," **6,410,955**, June 25, 2002.
16. Baker, R. J., "High-speed, low-power input buffer," **6,407,588**, June 18, 2002.
15. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,316,976**, Nov. 13, 2001.
14. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,256,234**, July 3, 2001.
13. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,104,209**, August 15, 2000.
12. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,069,506**, May 30, 2000.
11. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,026,051**, February 15, 2000.
10. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **6,026,050**, February 15, 2000.
9. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **5,953,284**, September 14, 1999.
8. Baker, R. J., "Fully-differential amplifier," **5,953,276**, September 14, 1999.
7. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array". **5,909,201**, June 1, 1999.
6. Hush, G. and Baker, R. J., "Field emission display having pulsed capacitance current control," **5,894,293**, April 13, 1999.
5. Baker, R. J., "Adaptively biased voltage regulator and operating method," **5,874,830**, February 23, 1999.
4. Hush, G. Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a Phase-Locked Loop," **5,818,365**, October 1, 1998.
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