

Case No. IPR2015-01524
U.S. Patent No. 6,366,130

Attorney Docket No.
ELBRUS-IPR2

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.

Petitioner

v.

ELBRUS INTERNATIONAL LIMITED

Patent Owner

Case: IPR2015-01524

U.S. Patent No. 6,366,130

PATENT OWNER'S RESPONSE

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Statutes

35 U.S.C. § 103

35 U.S.C. § 316(a)(8)

Rules

37 C.F.R. § 42.100(b)

37 C.F.R. § 42.120

Other Authorities

Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48764
(Aug. 14,2012)

Manual of Patent Examining Procedure (M.P.E.P.)

LIST OF EXHIBITS RELIED UPON

- Exhibit 1001 - U.S. Patent No. 6,366,130 ("the `130 patent").
- Exhibit 1002 - Declaration of Dr. Baker.
- Exhibit 1005 - U.S. Patent No. 5,828,241 (Sukegawa).
- Exhibit 1006 - U.S. Patent No. 6,108,254 (Watanabe et al.).
- Exhibit 1007 - U.S. Patent No. 6,249,469 (Hardee).
- Exhibit 1008 - Nicky Chau-Chun Lu and Hu H. Chao, *Half-VDD Bit-Line Sensing Scheme in CMOS DRAM's*, IEEE Journal of Solid State Circuits, Vol. SC-19, No. 4, August 1984.
- Exhibit 2001 - "Action Closing Prosecution" - Reexamination Control No. 95/000,657.
- Exhibit 2002 - Brent Keeth and R. Jacob Baker, *DRAM Circuit Design - A Tutorial*, IEEE Press Series on Microelectronic Systems, 2001, pp. 26-29.
- Exhibit 2003 - Deposition of R. Jacob Baker Ph.D., Las Vegas, NV, April 1, 2016.
- Exhibit 2004 - Declaration of William R. Huber D.Sc., P.E. in Support of Patent Owner's Response to Petition.
- Exhibit 2005- JEDEC *Dictionary of Terms for Solid State Technology*, JESD88E.
- Exhibit 2006- JEDEC Standard No. 8-1, Addendum No. 1 to JEDEC Standard No. 8, *Interface Standard for Low Voltage TTL-Compatible (LVTTL) VLSI Digital Circuits*, Electronic Industries Association, Washington, D.C., December 1984. (Ex. 2006).
- Exhibit 2007 - JEDEC Standard JESD79E (Revision of JESD79D), *Double Data Rate (DDR) SDRAM Specification*, JEDEC Solid State

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