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Paper No. 9
Entered: January 19, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ELBRUS INTERNATIONAL LIMITED,
Patent Owner.

Case IPR2015-01524
Patent 6,366,130

Before JUSTIN T. ARBES, JEFFREY W. ABRAHAM, and DANIEL J. GALLIGAN, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition seeking *inter partes* review of claims 1–3, 5–7, and 9 of U.S. Patent No. 6,366,130 B1 (Ex. 1001, "the '130 patent"), as amended by *Inter Partes* Reexamination Certificate No. US 6,366,130 C1 ("Reexam. Cert."). Paper 1 ("Pet."). Elbrus International Limited ("Patent Owner") filed a Preliminary Response to the Petition. Paper 8 ("Prelim. Resp."). Applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we institute an *inter partes* review of claims 1–3, 5–7, and 9 as discussed below.

Our determinations at this stage of the proceeding are based on the record developed thus far, prior to the Patent Owner's Response. This is not a final decision as to the patentability of any challenged claim. Any final decision will be based on the full record developed during trial.

II. BACKGROUND

A. Related Proceedings

The parties identify *Cascades Computer Innovation, LLC. v. Samsung Electronics Co., Ltd.*, Case No. 1-14-cv-05691 (N.D. Ill.), currently pending, as well as pending *inter partes* review petition in Case IPR2015-01523, also pertaining to the '130 patent. Pet. 1–2; Paper 4, 3.

B. The '130 Patent

The '130 patent, titled "High Speed Low Power Data Transfer Scheme," issued on April 2, 2002, with a reexamination certificate issuing on August 4, 2014. The '130 patent is directed to a "high speed and low power [complementary metal-oxide semiconductor (CMOS)] data transfer

arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver." Ex. 1001, 1:24–28, Fig. 1. In one embodiment, the latching sense amplifier is arranged as a "cross coupled latched amplifier." *Id.* at 1:36–38, Fig. 2. The '130 patent explains that its data transfer scheme can operate at increased speeds due to, *inter alia*, precharging the buses to a specific level (V_{pr}) between ground and V_{dd}. *Id.* at 2:23–38, 3:17–55.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5–7, and 9. Claim 1 is the only independent claim challenged, and is reproduced below:

> 1. A data transfer arrangement comprising:
>
> two bus drivers;
>
> a voltage precharge source;
>
> a differential bus coupled to the bus drivers and to the voltage precharge source; aid
>
> a latching sense amplifier coupled to the differential bus;
>
> wherein the latching sense amplifier comprises:
>
> a first stage including a cross-coupled latch coupled to a differential data bus; and
>
> an output stage coupled to an output of said first stage;
>
> wherein the output of the first stage is coupled to an input of the output stage;
>
> wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.

Id. at 4:2–17.

D. References

Petitioner relies on the following references:

Sukegawa, U.S. Patent No. 5,828,241, issued Oct. 27, 1998 ("Sukegawa," Ex. 1005).

Watanabe et al., U.S. Patent No. 6,108,254, filed Nov. 12, 1993, issued Aug. 22, 2000 ("Watanabe," Ex. 1006).

Hardee, U.S. Patent No. 6,249,469 B1, filed July 1, 1996, issued June 19, 2001 ("Hardee," Ex. 1007).

Nicky Chau-Chun Lu & Hu H. Chao, *Half-V_{DD} Bit-Line Sensing Scheme in CMOS DRAM's*, SC-19:4 IEEE JOURNAL OF SOLID STATE CIRCUITS 451–454 (1984) ("Lu," Ex. 1008).

E. The Asserted Grounds

Petitioner asserts the following grounds of unpatentability:

References	Statutory Basis	Claim(s) Challenged
Sukegawa and Lu	§103	1, 2, 5, 6, and 9
Sukegawa, Lu, and Watanabe	§103	3
Sukegawa, Lu, and Hardee	§103	7

III. ANALYSIS

A. Claim Construction

Petitioner offers constructions for two terms, "latching sense amplifier" and "stage." Pet. 9–11. Petitioner contends that "latching sense amplifier" should be construed to mean "a circuit, including a latch, that detects and amplifies signals." *Id.* at 9. Petitioner contends that "stage" should be construed to mean "portion of a circuit." *Id.* at 10.

Patent Owner argues that these terms are commonly used and well-known in the art, and should be given their plain and ordinary meaning. Prelim. Resp. 4–6.

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1275–79 (Fed. Cir. 2015). We determine that no express claim construction is required for purposes of this Decision.

B. References

1. Sukegawa

Sukegawa discloses a "signal transmission circuit which enables the distance of signal transmission . . . to be increased, while the signal delay and power consumption are reduced." Ex. 1005, Abstract. Sukegawa teaches that "the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals." *Id.* at 1:12–15. Sukegawa provides circuit diagrams illustrating, and corresponding descriptions in the specification describing, the specific configuration of the various components of its transmission circuit. *See id.* at 6:35–9:50, Figs. 1–7.

2. Watanabe

Watanabe discloses a "[dynamic random access memory (DRAM)] having means which can transfer data at a sufficiently high speed." Ex. 1006, 1:64–65. Watanabe's data transfer circuit contains differential amplifier circuit 10, equalizing circuit 11, data latch circuit 12, pairs of first data lines 13 and second data lines 14, and pair of data output lines 15. *Id.* at

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