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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD,
Petitioner,

v.

ELBRUS INTERNATIONAL LIMITED,
Patent Owner.

Case IPR2015-01524
Patent 6,366,130

Before JUSTIN T. ARBES, JEFFREY W. ABRAHAM, and DANIEL J. GALLIGAN, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition seeking *inter partes* review of claims 1–3, 5–7, and 9 of U.S. Patent No. 6,366,130 B1 (Ex. 1001, "the '130 patent"), as amended by *Inter Partes* Reexamination Certificate No. US 6,366,130 C1 ("Reexam. Cert."). Paper 1 ("Pet."). Elbrus International Limited ("Patent Owner") filed a Preliminary Response to the Petition. Paper 8. On January 19, 2016, we instituted an *inter partes* review of claims 1–3, 5–7, and 9. Paper 9 ("Dec. on Inst.").

After institution, Patent Owner filed a Patent Owner Response (Paper 12, "PO Resp."), and Petitioner filed a Reply (Paper 16, "Reply"). An oral hearing was held on October 18, 2016, and a transcript of the hearing has been entered into the record of the proceeding as Paper 25 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1, 2, 5–7, and 9 are unpatentable.

II. BACKGROUND

A. Related Proceedings

The parties identify *Cascades Computer Innovation, LLC. v. Samsung Electronics Co., Ltd.*, Case No. 1-14-cv-05691 (N.D. Ill). Pet. 1–2; Paper 4, 3.

B. The '130 Patent

The '130 patent, titled "High Speed Low Power Data Transfer Scheme," issued on April 2, 2002, with a reexamination certificate issuing on August 4, 2014. The '130 patent is directed to a "high speed and low power [complementary metal-oxide semiconductor (CMOS)] data transfer

arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver." Ex. 1001, 1:24–28, Fig. 1. In one embodiment, the latching sense amplifier is arranged as a "cross coupled latched amplifier." *Id.* at 1:36–38, Fig. 2. The '130 patent explains that its data transfer scheme can operate at increased speeds due to, *inter alia*, precharging the buses to a specific level (Vpr) between ground and Vdd. *Id.* at 2:23–38, 3:17–55.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5–7, and 9. Claim 1 is the only independent claim challenged and is reproduced below.

> 1. A data transfer arrangement comprising:
>
> two bus drivers;
>
> a voltage precharge source;
>
> a differential bus coupled to the bus drivers and to the voltage precharge source; aid
>
> a latching sense amplifier coupled to the differential bus;
>
> wherein the latching sense amplifier comprises:
>
> a first stage including a cross-coupled latch coupled to a differential data bus; and
>
> an output stage coupled to an output of said first stage;
>
> wherein the output of the first stage is coupled to an input of the output stage;
>
> wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.

Id. at 4:2–17.

D. References

Petitioner relies on the following references:

Sukegawa, U.S. Patent No. 5,828,241, issued Oct. 27, 1998 ("Sukegawa," Ex. 1005).

Watanabe et al., U.S. Patent No. 6,108,254, filed Nov. 12, 1993, issued Aug. 22, 2000 ("Watanabe," Ex. 1006).

Hardee, U.S. Patent No. 6,249,469 B1, filed July 1, 1996, issued June 19, 2001 ("Hardee," Ex. 1007).

Nicky Chau-Chun Lu & Hu H. Chao, *Half-V_{DD} Bit-Line Sensing Scheme in CMOS DRAM's*, SC-19:4 IEEE JOURNAL OF SOLID STATE CIRCUITS 451–454 (1984) ("Lu," Ex. 1008).

E. Reviewed Grounds of Unpatentability

The Board instituted trial to review the patentability of the challenged claims on the following grounds (Dec. on Inst. 19):

References	Statutory Basis	Claim(s) Challenged
Sukegawa and Lu	§103	1, 2, 5, 6, and 9
Sukegawa, Lu, and Watanabe	§103	3
Sukegawa, Lu, and Hardee	§103	7

F. Level of Ordinary Skill in the Art

Petitioner's declarant, R. Jacob Baker, Ph.D., testified that "a person of ordinary skill in the art related to the technology of the '130 Patent would have had an undergraduate degree in Electrical Engineering or equivalent and at least two to three years of experience in the design and/or analysis of data transfer circuits or the equivalent." Ex. 1002 ¶ 15. Patent Owner's declarant, William R. Huber, D.Sc., similarly testified that a person of ordinary skill in the art would have had "a Bachelor of Science degree in

Electrical Engineering or an equivalent field, as well as at least 2 years of experience designing and analyzing data transfer or equivalent circuits." Ex. 2004 ¶ 27.

We credit the testimony provided by the declarants for both parties and hold that one of ordinary skill in the art would have possessed an undergraduate degree in electrical engineering or equivalent field and at least two years of experience in the design and/or analysis of data transfer or equivalent circuits. This level of ordinary skill is reflected not only by the information presented by the parties, but also by the prior art of record. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of ordinary skill in the art).

III. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). In applying a broadest reasonable construction, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Based on the parties' post-issuance arguments (Reply 2–6; PO Resp. 20–24; Tr. 33:25–34:6), we address the proper interpretation of the claim term "bus," which we discuss below. No other express claim construction is

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