United States Patent [19]

Ternullo, Jr. et al.

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[54] **HIGH-SPEED SYNCHRONOUS WRITE CONTROL SCHEME**

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[51] Int. Cl.[7] **G11C 8/00**

[52] U.S. Cl. **365/233**; 365/189.05; 365/202; 365/190

[58] Field of Search 365/233, 189.05, 365/202, 190

[56] **References Cited**

U.S. PATENT DOCUMENTS

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[57] **ABSTRACT**

The present invention provides a method and apparatus that accomplishes a high performance, random read/write SDRAM design by synchronizing the read and write operations at the data line sense amplifier. This enables the design to perform random read and write operations without varying cycle time issues or unbalanced margin issues. The data lines are used as bi-directional lines to accomplish high performance reads and writes with minimal additional wiring overhead required. During a read operation, read data is transferred from the memory cells of the device across a series of consecutive pairs of data lines to an input/output port of the memory device. The first pair of data lines is coupled to a data line sense amplifier. The additional pairs of data lines are coupled to additional amplifiers. During a read operation, data is transferred across the consecutive pairs of data lines according to the timing cycles of the respective amplifiers. In order to quickly drive the data signals during a write operation up the series of consecutive pairs of data lines, the timing signals for each of the pairs of data lines except the first pair of data lines are disabled so that the data lines are allowed to float, and then the data lines are overdriven with the write data so that the write data quickly transitions up the series of data lines to the selected data line sense amplifier, where it arrives at approximately the same time that read data normally arrives during the timing cycle for the data line sense amplifier.
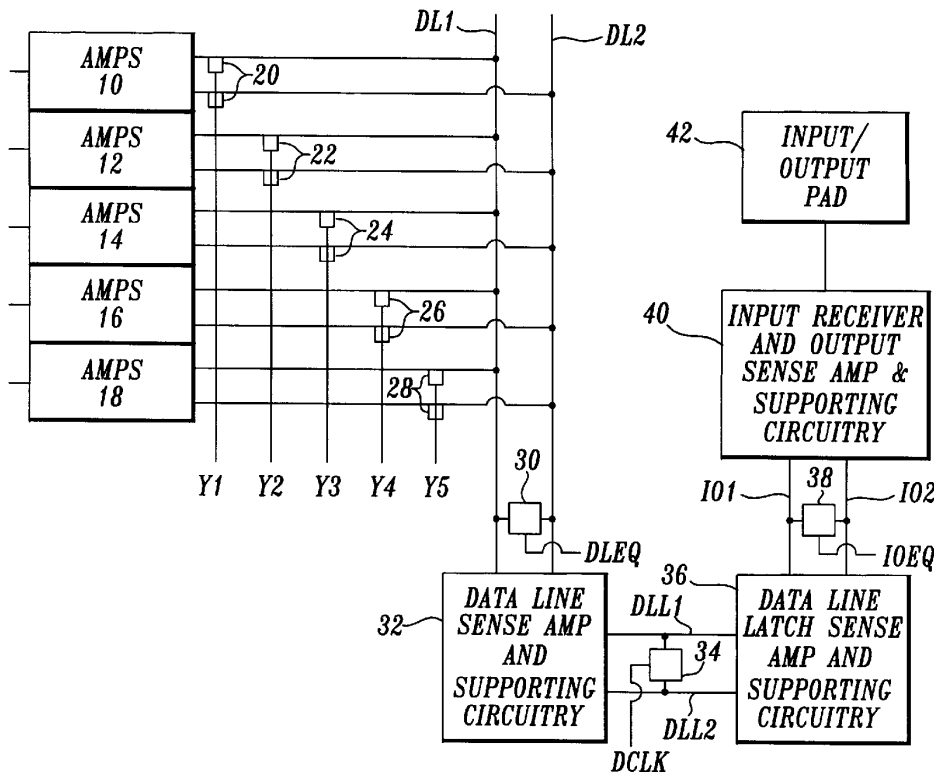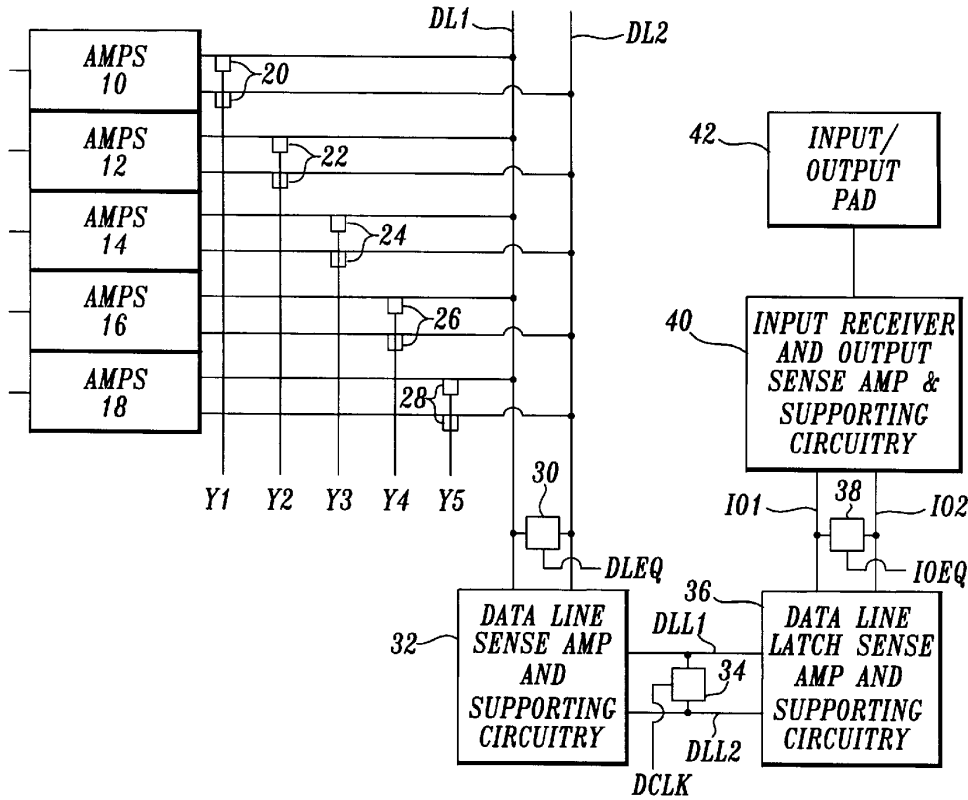
26 Claims, 12 Drawing Sheets

Fig. 1.

32A

DL1   DL2

120   60

DLEQ → EQUALIZING LOGIC

DLEQB

DLEQD

EQUALIZING CIRCUIT

ISOLATION CIRCUIT — 70

110

LAT1

DCLK   ISOLATION AND LATCH LOGIC

SEL

DCLKT

80

DATA LINE LATCH

LAT2

DCLKTN

100

READBM

READ LOGIC

READM

READ DRIVERS — 90
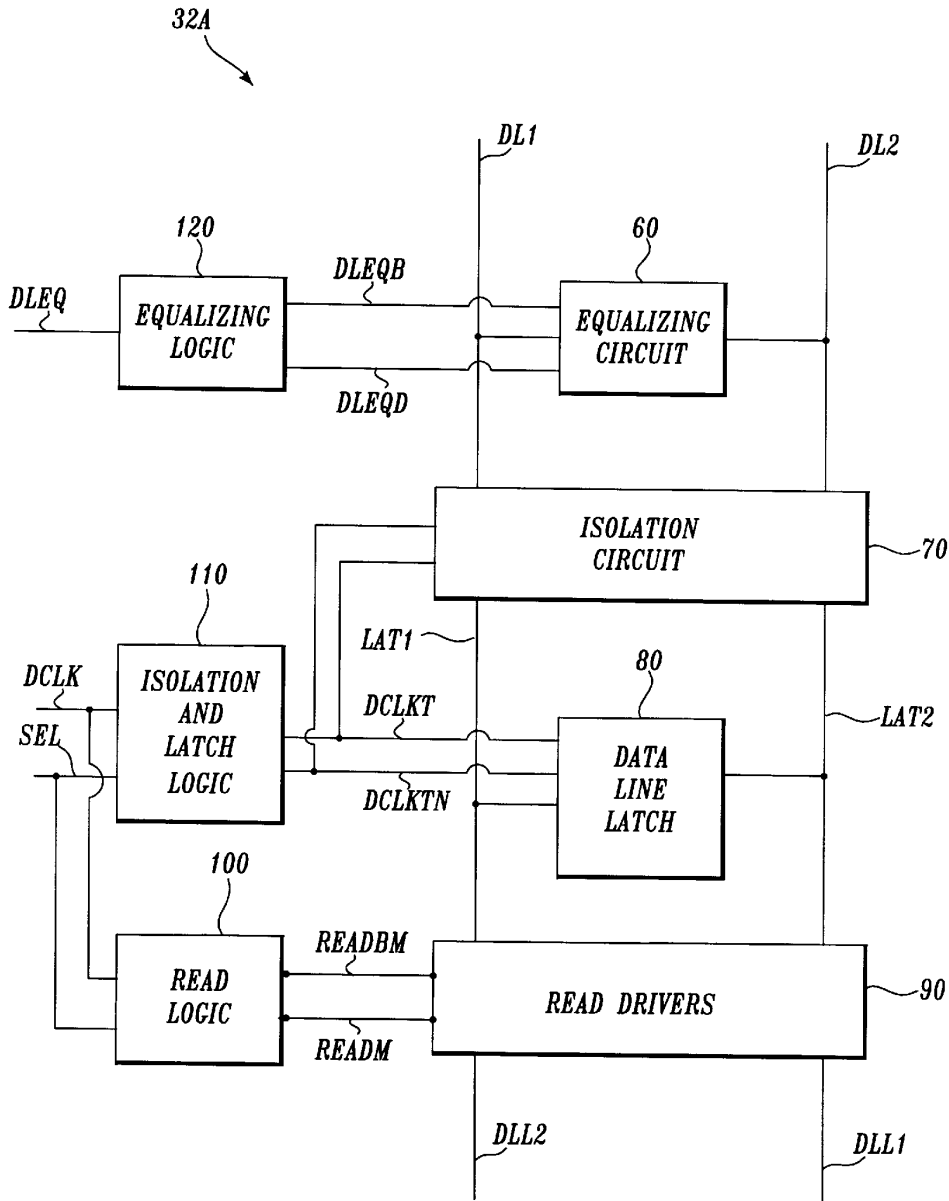
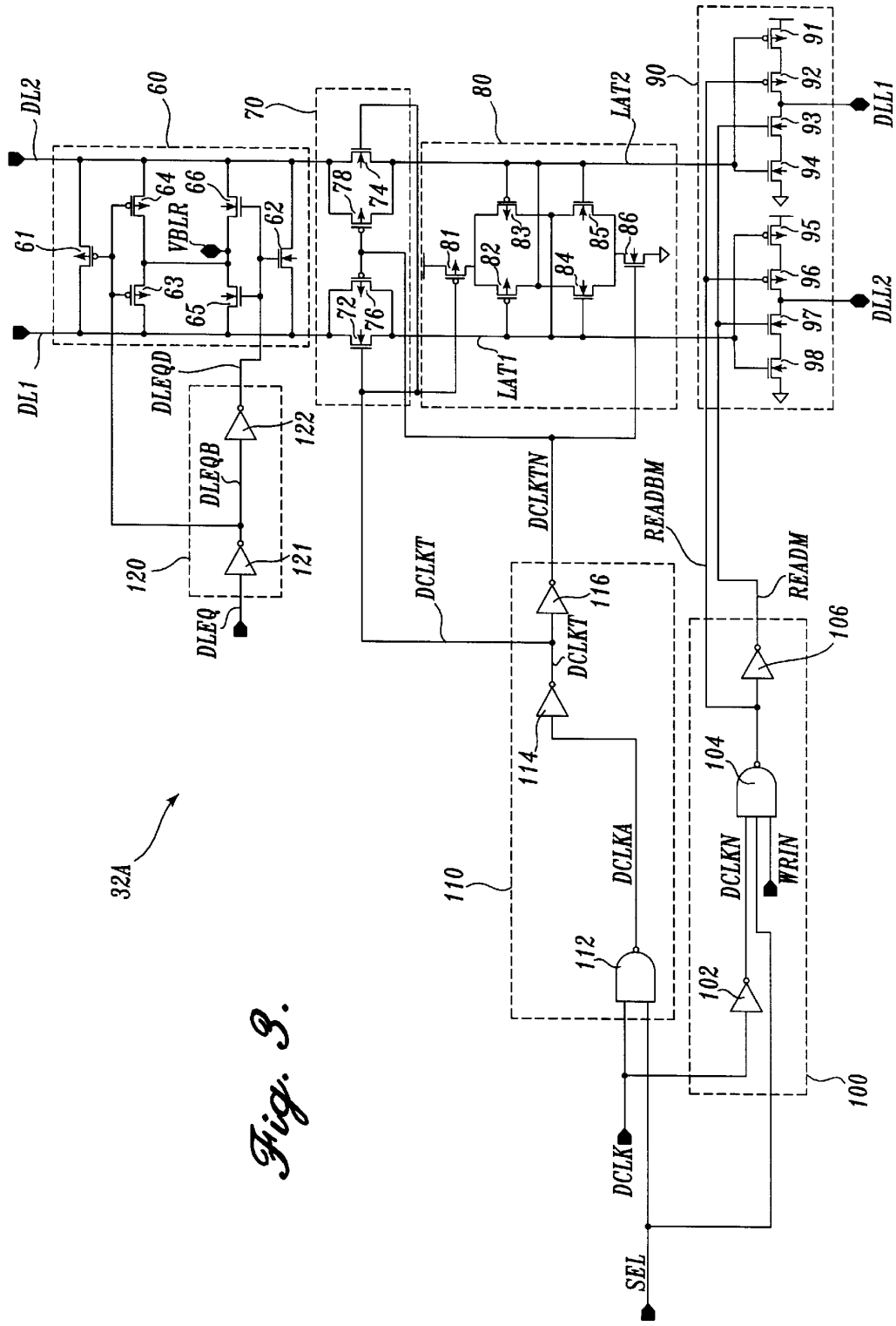DLL2   DLL1

Fig. 2.

Fig. 3.

Fig. 4.

DOCKET ALARM
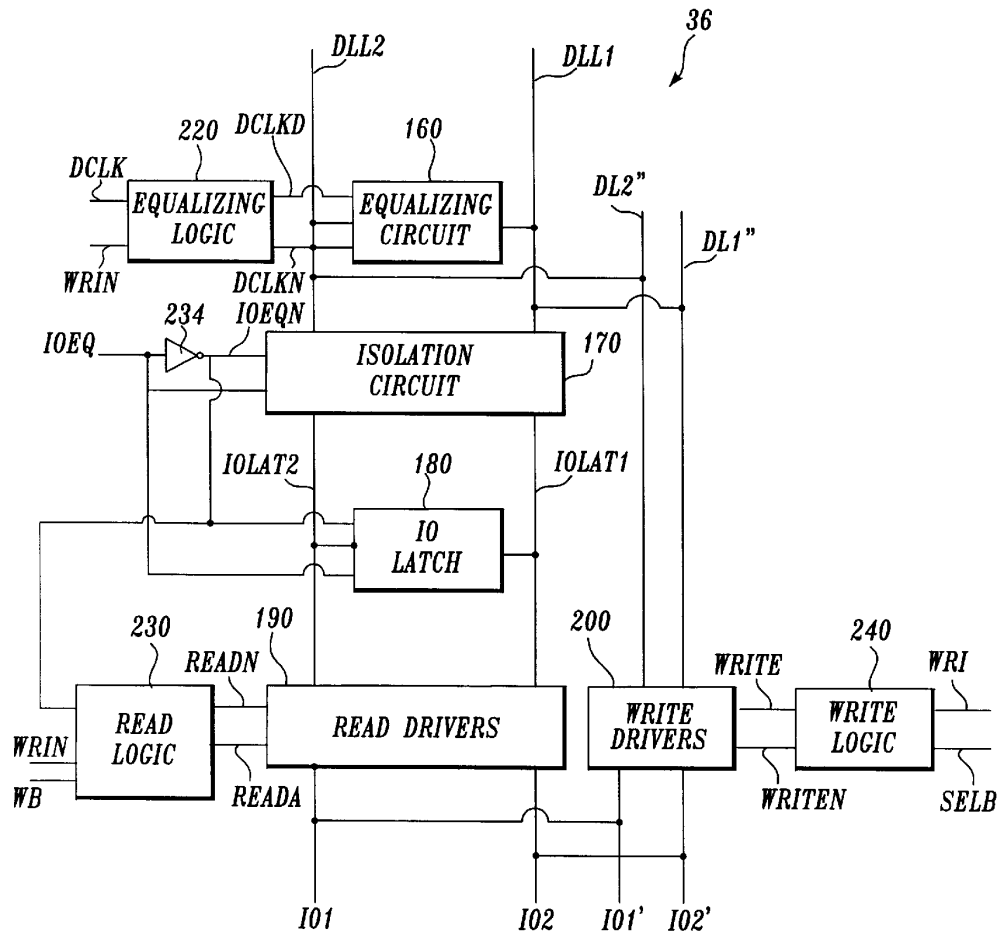
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