[redacted]

17

Customer No. 20350
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

02.22.00

Attorney Docket No. 20181-5US
Client Ref No. PPA-5

ASSISTANT COMMISSIONER FOR PATENTS
BOX PATENT APPLICATION
Washington, D.C. 20231

"Express Mail" Label No. EL394877883US
Date of Deposit: February 17, 2000

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

By: Sunil Dutt

jc600 U.S. PTO 02/17/00

jc678 U.S. PTO 09/505656 02/17/00

Transmitted herewith for filing is the
[**X**] patent application of

Inventor(s)/Applicant Identifier: Andrew V. Podlesny et al.

For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

[**X**] This application claims priority from each of the following Application Nos./filing dates:
60/120,531/Filed 2/17/99
the disclosure(s) of which is (are) incorporated by reference.

Enclosed are:

[**X**] 1 sheet(s) of [ ] formal [**X**] informal drawing(s).

[**X**] A [ ] signed [**X**] unsigned Declaration.

[**X**] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [**X**] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

Kevin T. LeMond
Reg No.: 35,933
Attorneys for Applicant

Telephone:
(415) 576-0200

Facsimile:
(415) 576-0300

SF 1036480 v1

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov
Application or Patent No.:
Filed or Issued:
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

[ ] the owner of the small business concern identified below
[X] an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Elbrus International Limited
Address of Small Business Concern: P.O. Box 265
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov described in:

[X] the specification filed herewith;
[ ] Application No. _____, filed _____;
[ ] Patent No. _____, issued _____.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim
Title of Person if Other than Owner: President
Address of Person Signing: 14 Bolshoy Savvinsky per.
Moscow 119435, Russia

Signature _____ Date 02/4/2000

SF 1058186 v1

Attorney Docket No.: 20181-5US
Client Reference No.: PPA-5

PATENT APPLICATION

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

Inventor(s):

Andrew V. Podlesny
38/2 Menzinsky Street, Apt. 192
Moscow, Russia 129281
a citizen of Russia

Valery V. Lozovoy
108 Ac.Chelomey Street, Apt. 6
Moscow, Russia 117630
a citizen of Russia

Alexander V. Malshin
50 Frunzenskaya Nabergnaya, Apt. 608
Moscow, Russia 119270
a citizen of Russia

Assignee:

ELBRUS INTERNATIONAL LIMITED
14, Bolshoi Savvinski Per.
Moscow, Russia 119435

Entity: Small business concern

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

PATENT
Attorney Docket No.: 20181-5US
Client Reference No.: PPA-5

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

This application claims priority from U.S. Provisional Patent Application No. 60/120,531, filed February 17, 1999, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to a data transfer scheme, and more particularly, to a high speed and low power CMOS data transfer scheme.

2. Description Of The Prior Art

Today's requirements for electronic circuits require high speed. Additionally, the circuits should be as small and simple as possible due to the ever increasing number of circuits that are crowding today's chip devices. Furthermore, circuits for data transfer should not be sensitive to circuit parameter mismatches, noise, and deviations in various applied voltages.

SUMMARY OF THE INVENTION

The present invention provides a high speed and low power CMOS data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver.

In accordance with one embodiment of the present invention, a data transfer arrangement includes two bus drivers, a voltage precharge source, a differential bus coupled to the bus drivers and to the voltage precharge source, and a latching sense amplifier coupled to the differential bus.

In accordance with another embodiment of the present invention, the latching sense amplifier is arranged as a cross coupled latched amplifier.

In accordance with a further embodiment of the present invention, the two bus drivers consist of active pull up/pull down bus drivers.

Thus, the present invention provides a data transfer arrangement that operates at a high speed and uses low power. The data transfer arrangement is faster because the bus voltage swing passes directly to high gain nodes of the cross-coupled latched amplifier. Additionally, the data transfer arrangement uses a lower number of stacked transistors coupled between the supply voltage and the high gain nodes when compared to the prior art. Additionally, the arrangement according to the present invention is less sensitive to deviations in voltage sources and the deviation of threshold voltage concerns of the input transistors. Additionally, the arrangement is less sensitive to circuit parameter mismatches, data bus common mode noise and power bus noises.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred embodiments below, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a differential data transfer arrangement in accordance with the present invention; and

Figure 2 is a schematic of a circuit for a sense amplifying latch for use in the data transfer arrangement illustrated in Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a data transfer arrangement circuit 10 that includes two bus drivers 11, 12, a precharge circuit 13, and two complementary bus lines 14, 15. The bus lines are inputs to a bus receiver 16 that is arranged as a latching sense amplifier.

The two bus drivers are complementary and consist, preferably, of two active pull up/active pull down bus drivers.

Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

During the bus precharge phase, the control input PR (control signal for bus precharge circuit 13) is high and signal inputs DT (true phase of dual-rail data function) and DC (complement phase of dual-rail data function) are low. The true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23

are in high impedance state and both bus lines are equalized and precharged to a potential V_{pr} (buses precharging voltage level) through the turned on transistors 24, 25 and 26.

During the data transfer phase, the control input PR is low. The signal inputs become differential: DT is high and DC is low, and vise versa. One of the drivers is pulled up and charges the appropriate bus line from the precharged level V_{pr} toward a more positive $V_{dd} - V_t$ (where V_t is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged level V_{pr} towards a more negative level V_{ss} (ground). This provides a differential voltage: +dV and – dV from the precharging level V_{pr} between true and complement bus lines. To provide proper operation of the bus receiver (the sensing amplifier), the minimum voltage difference 2* dV_{min} (swing) between the lines may be about 0.05-- 0.20V. This low voltage swing is a basis to obtain high frequency of data transfer through the bus.

Figure 2 illustrates sensing amplifier 16. Preferably, the sensing amplifier is a cross-coupled latched amplifier.

The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode. The cross-coupled latched amplifier is isolated from the power buses (transistors 30 and 31 are turned off). Transistors 32 and 33 are turned on and thus, the bus voltage swing passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to V_{dd} and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high.

When the control input CLK is high and the bus driver is in the precharge mode, the sensing amplifier is in the data transfer mode. Transistors 32 and 33 are turned of and isolate the internal nodes IT and IC of the latched amplifier from the bus lines. The cross-coupled latched amplifier is connected to power buses (transistors 30 and 31 are turned on) and it begins to amplify the low voltage swings of the internal nodes IT

and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low.

The use of domino output stages in accordance with the present invention instead of static inverters is necessary to avoid leakage currents and output glitches, which may appear because potentials of nodes IT and IC are approximately equal to V_{pr} during the operating cycle of the bus driver. Weak PMOS transistors 34 and 35 are preferably included in the sensing amplifier to help prevent output glitches.

The data transfer arrangement in accordance with the present invention provides an increase in speed due to the differential low voltage swing bus driver in combination with the use of the latched differential sense amplifier as the bus receiver.

A further increase in speed is attained with the data transfer arrangement due to the pull up/pull down bus drivers, which provide equal low differential voltage swings +dV/ - dV in both bus lines. This allows both bus lines to be active during the data transfer phase, eliminates the necessity to use special circuits for holding the precharged level and leads to a reduction in the capacitance load of the driver.

The buses precharging to the specific level between ground and V_d ($V_{pr} = K*V_{dd}$, where K = 1/3 for the ideal MOS model) also provides: equal charge and discharge driver currents $I_{ch} = Id_{ch}$, provided by the NMOS pull up follower and the NMOS pull down switch, respectively, and therefore, equal differential voltage swings dV in both charged and discharged bus during the data transfer phase Pdtf: $+ dV = I_{ch}*D_{dtf}/C_{LOAD}$; and $-dV = I_{dch} *T_{dtf}/C_{LOAD}$. I_{ch} represents the driver pull up output current (which provides the C_{LOAD} charging from V_{pr} up to V_{dd}); I_{dch} represents the driver pull down output current (providing the C_{LOAD} discharging from V_{pr} up to V_{ss}); C_{LOAD} represents the bus lines' compacitances; +dV represents the bus voltage change up from V_{pr} during data transfer phase; -dV represents the bus voltage change down from V_{pr} during data transfer phase; and T_{dtf} represents the data transfer phase duration. The buses precharging to the specific level between ground and V_{dd} also provides high noise immunity due to active mode for both buses that equal low output resistances of the drivers in pull up and pull down mode and; low total power consumed by drivers during the cycle of operation (transfer plus precharge).

The latched sense amplifier is faster due to the bus voltage swing passing directly to the high-gain nodes IT and IC of the cross- coupled latched amplifier, the lower number of stacked transistors that are connected between the supply voltage V_{dd} (or

V_{cc}) and nodes IT and IC, the fact that during latching of the IT and IC nodes, the nodes are charged by $K*V_{dd}$ and $(1-K)*V_{dd}$ instead of simply V_{dd}. Additionally, the speed of the latched sensing amplifier is effected little by the deviation of voltage V_{pr} and the deviation of the threshold voltage of the input transistors.

In addition to the higher speed and low power consumption of the data transfer arrangement in accordance with the present invention, the arrangement is also less sensitive to circuit parameters mismatching, data bus common mode noise and power buses' noises since both drivers are active during data transfer phase. During the appropriate bus precharge phase, the bus receiver is isolated from the bus lines.

Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus.

2. A data transfer arrangement in accordance with claim 1 wherein the latching sense amplifier comprises a cross coupled latched amplifier.

3. A data transfer arrangement in accordance with claim 1 wherein the bus drivers consist of active pull up/pull down bus drivers.

HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

ABSTRACT OF THE DISCLOSURE

A data transfer arrangement. The data transfer arrangement includes two active pull up/active pull down bus drivers and a voltage precharge source. A differential bus is coupled to the bus drivers and to the voltage precharge source. A latching sense amplifier is coupled to the differential bus and serves as the bus receiver. The bus drivers operate in a precharge phase and a data transfer phase. The bus receiver operates in an analogous but opposite manner, i.e., when the bus drivers are in the precharge phase, the bus receiver is in the data transfer phase and when the bus drivers are in the data transfer phase, the bus receiver is in a precharge phase

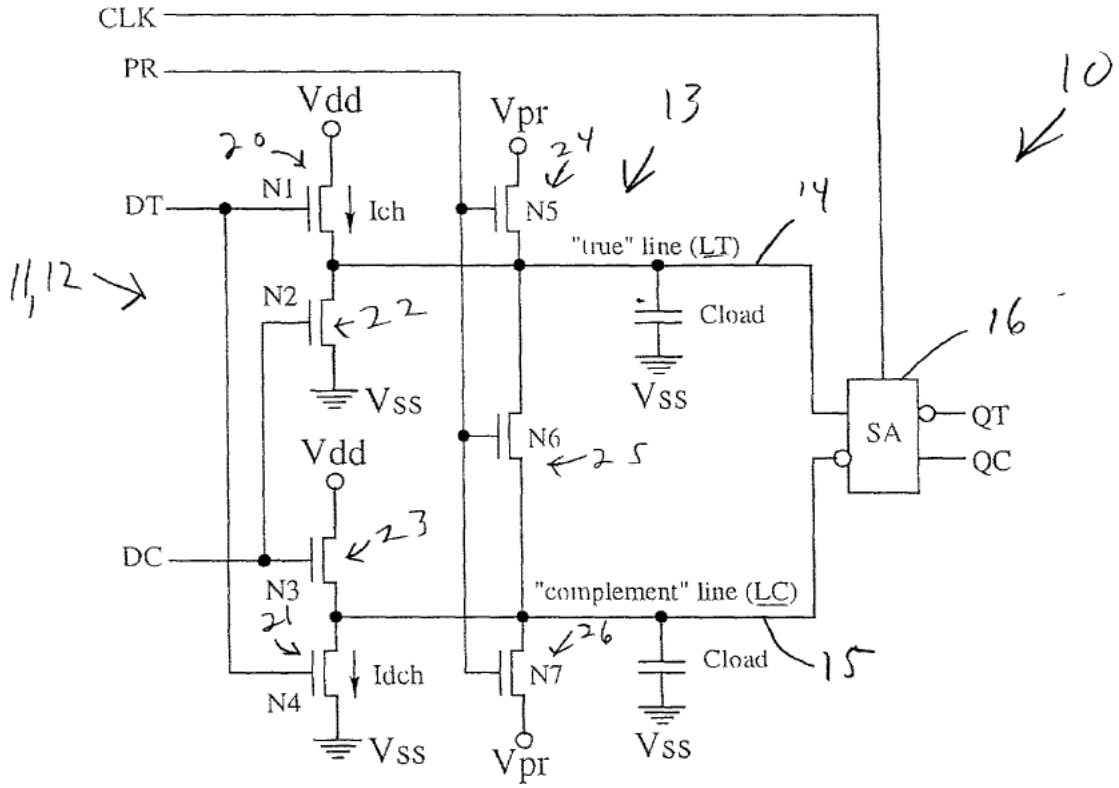

CLK
PR
Vdd
Vpr
10
13
20
24
N1
Ich
N5
DT
14
"true" line (LT)
11, 12
N2
22
Cload
16
Vss
Vss
SA
QT
N6
25
QC
Vdd
23
DC
N3
"complement" line (LC)
21
26
Cload
15
Idch
N7
N4
Vss
Vpr
Vss
Bus drivers
Precharge circuit
Bus lines
Bus reciever

Fig.1.

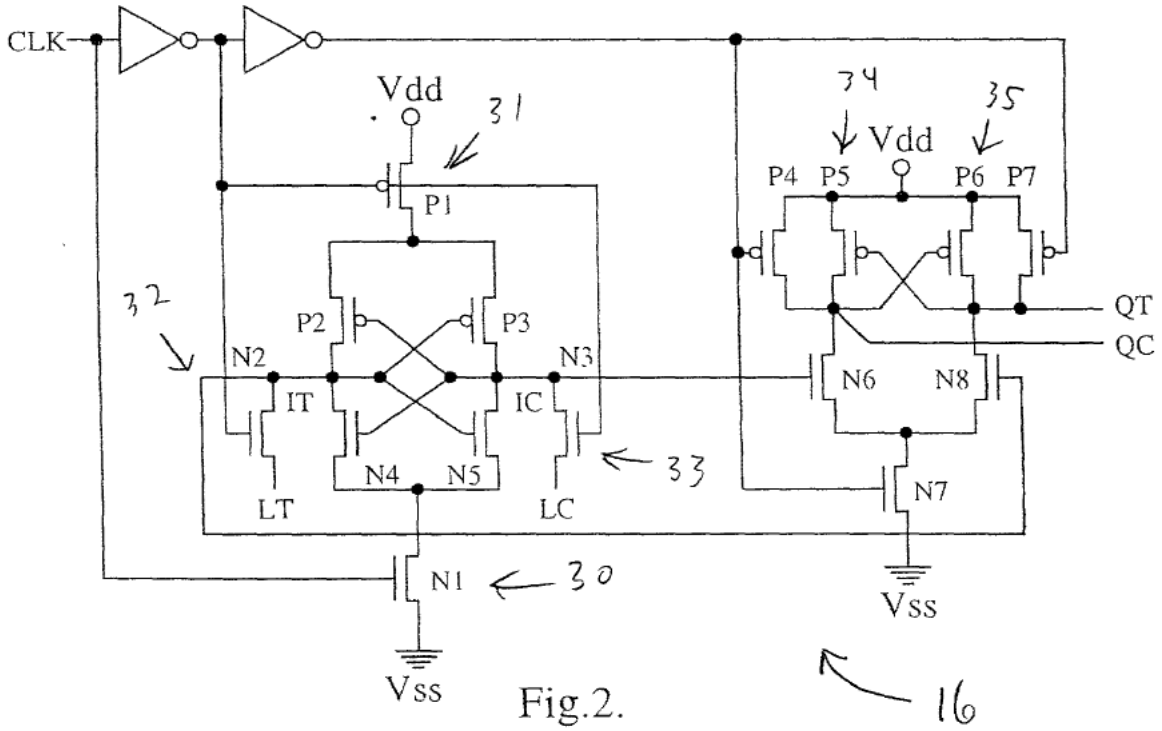

CLK
Vdd
31
34
35
Vdd
P4
P5
P6
P7
P1
32
P2
P3
QT
QC
N2
N3
N6
N8
IT
IC
33
N4
N5
N7
LT
LC
N1
30
Vss
Vss
16

Fig.2.

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which _X_ is attached hereto or ___ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

J. Georg Seka, Reg. No. 24,491
Robert J. Bennett, Reg. No. 27,533
Charles E. Krueger, Reg. No. 30,077
Charles J. Kulas, Reg. No. 35,809
Kevin T. LeMond, Reg. No. 35,933
George B.F. Yee, Reg. No. 37,478
Chad S. Hilyard, Reg. No. 40,647
Gerald T. Gray, Reg. No. 41,797
Daniel D. Tagliaferri, Reg. No. 43,178
Thomas D. Franklin, Reg. No. 43,616
Patrick M. Boucher, Reg. No. 44,037

Send Correspondence to:	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)
Kevin T. LeMond **TOWNSEND and TOWNSEND and CREW LLP** **Two Embarcadero Center, 8th Floor** **San Francisco, California 94111-3834**	Name: Kevin T. LeMond Reg. No.: 35933 Telephone: 415-576-0200

Full Name of Inventor 1:	Last Name: **Podlesny**	First Name: **Andrew**	Middle Name or Initial: **V.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **Apt. 192, 38/2 Menzinsky St.**	City: **Moscow**	State/Country: **Russia**	Postal Code: **129281**
Full Name of Inventor 2:	Last Name: **Malshin**	First Name: **Alexander**	Middle Name or Initial: **V.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **Apt. 608, 50 Frunzenskaya Nabergnaya**	City: **Moscow**	State/Country: **Russia**	Postal Code: **119270**
Full Name of Inventor 3:	Last Name: **Solomatnikov**	First Name: **Alexander**	Middle Name or Initial: **Y.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **14, Bolshoi Savvinski Per.**	City: **Moscow**	State/Country: **Russia**	Postal Code: **119435**

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Andrew V. Podlesny	Alexander V. Malshin	Alexander Y. Solomatnikov
Date	Date	Date

SF 1060790 v1

Customer No. 20350
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

Attorney Docket No. 20181-5US
Client Ref No. PPA-5

ASSISTANT COMMISSIONER FOR PATENTS
BOX PATENT APPLICATION
Washington, D.C. 20231

"Express Mail" Label No. EL394877883US
Date of Deposit: February 17, 2000

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

By: _____

Sir:

Transmitted herewith for filing is the
[X] patent application of

Inventor(s)/Applicant Identifier: Andrew V. Podlesny et al.

For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

[X] This application claims priority from each of the following Application Nos./filing dates:
60/120,531/Filed 2/17/99
the disclosure(s) of which is (are) incorporated by reference.

Enclosed are:
[X] 1 sheet(s) of [ ] formal [X] informal drawing(s).
[X] A [ ] signed [X] unsigned Declaration.
[X] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [X] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

Kevin T. LeMond
Reg No.: 35,933
Attorneys for Applicant

Telephone: (415) 576-0200
Facsimile: (415) 576-0300

SF 1068480 v1

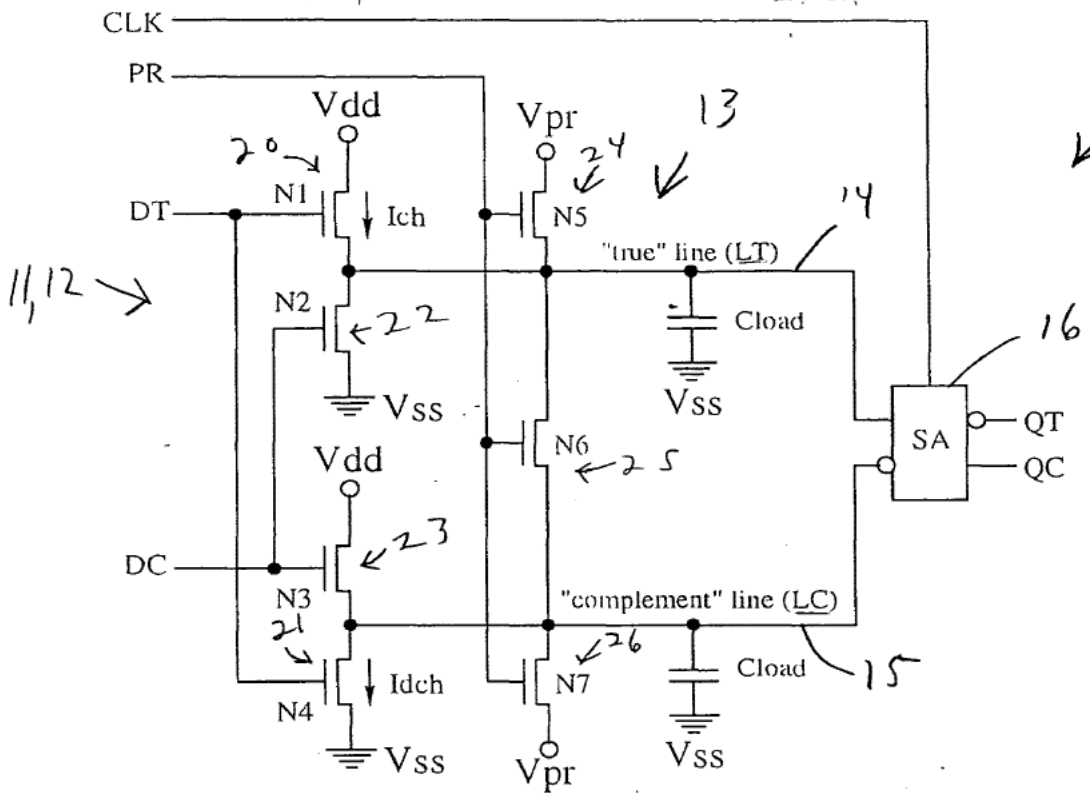

CLK
PR
Vdd
Vpr
10
13
20
24
N1
Ich
N5
DT
14
"true" line (LT)
11,12
N2
22
Cload
16
Vss
Vss
SA
QT
QC
N6
25
Vdd
DC
23
N3
"complement" line (LC)
21
26
Idch
N7
Cload
15
N4
Vss
Vpr
Vss
Bus drivers
Precharge circuit
Bus lines
Bus reciever

Fig.1.

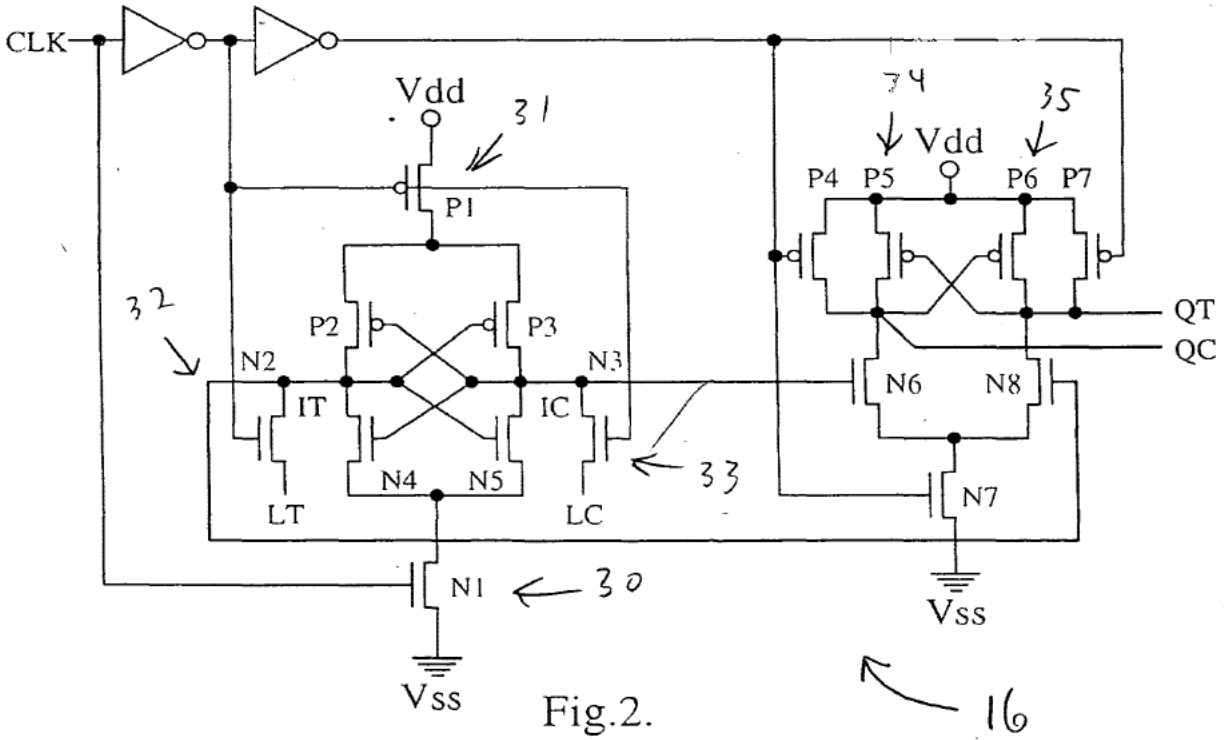

CLK
Vdd
31
34
35
Vdd
P4
P5
P6
P7
P1
32
P2
P3
QT
QC
N2
N3
N6
N8
IT
IC
N4
N5
33
N7
LT
LC
N1
30
Vss
Vss
16

Fig.2.

2

Attorney Docket No.: 20181-5US
Client Reference No.: PPA-5

PATENT APPLICATION

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

Inventor(s):

Andrew V. Podlesny
38/2 Menzinsky Street, Apt. 192
Moscow, Russia 129281
a citizen of Russia

Valery V. Lozovoy
108 Ac.Chelomey Street, Apt. 6
Moscow, Russia 117630
a citizen of Russia

Alexander V. Malshin
50 Frunzenskaya Nabergnaya, Apt. 608
Moscow, Russia 119270
a citizen of Russia

Assignee:

ELBRUS INTERNATIONAL LIMITED
14, Bolshoi Savvinski Per.
Moscow, Russia 119435

Entity: Small business concern

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

PATENT

Attorney Docket No.: 20181-5US

Client Reference No.: PPA-5

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

This application claims priority from U.S. Provisional Patent Application No. 60/120,531, filed February 17, 1999, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to a data transfer scheme, and more particularly, to a high speed and low power CMOS data transfer scheme.

2. Description Of The Prior Art

Today's requirements for electronic circuits require high speed. Additionally, the circuits should be as small and simple as possible due to the ever increasing number of circuits that are crowding today's chip devices. Furthermore, circuits for data transfer should not be sensitive to circuit parameter mismatches, noise, and deviations in various applied voltages.

SUMMARY OF THE INVENTION

The present invention provides a high speed and low power CMOS data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver.

In accordance with one embodiment of the present invention, a data transfer arrangement includes two bus drivers, a voltage precharge source, a differential bus coupled to the bus drivers and to the voltage precharge source, and a latching sense amplifier coupled to the differential bus.

In accordance with another embodiment of the present invention, the latching sense amplifier is arranged as a cross coupled latched amplifier.

In accordance with a further embodiment of the present invention, the two bus drivers consist of active pull up/pull down bus drivers.

Thus, the present invention provides a data transfer arrangement that operates at a high speed and uses low power. The data transfer arrangement is faster because the bus voltage swing passes directly to high gain nodes of the cross-coupled latched amplifier. Additionally, the data transfer arrangement uses a lower number of stacked transistors coupled between the supply voltage and the high gain nodes when compared to the prior art. Additionally, the arrangement according to the present invention is less sensitive to deviations in voltage sources and the deviation of threshold voltage concerns of the input transistors. Additionally, the arrangement is less sensitive to circuit parameter mismatches, data bus common mode noise and power bus noises.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred embodiments below, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a differential data transfer arrangement in accordance with the present invention; and

Figure 2 is a schematic of a circuit for a sense amplifying latch for use in the data transfer arrangement illustrated in Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a data transfer arrangement circuit 10 that includes two bus drivers 11, 12, a precharge circuit 13, and two complementary bus lines 14, 15. The bus lines are inputs to a bus receiver 16 that is arranged as a latching sense amplifier.

The two bus drivers are complementary and consist, preferably, of two active pull up/active pull down bus drivers.

Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

During the bus precharge phase, the control input PR (control signal for bus precharge circuit 13) is high and signal inputs DT (true phase of dual-rail data function) and DC (complement phase of dual-rail data function) are low. The true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23

are in high impedance state and both bus lines are equalized and precharged to a potential V_{pr} (buses precharging voltage level) through the turned on transistors 24, 25 and 26.

During the data transfer phase, the control input PR is low. The signal inputs become differential: DT is high and DC is low, and vise versa. One of the drivers is pulled up and charges the appropriate bus line from the precharged level V_{pr} toward a more positive $V_{dd} - V_t$ (where V_t is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged level V_{pr} towards a more negative level V_{ss} (ground). This provides a differential voltage: +dV and – dV from the precharging level V_{pr} between true and complement bus lines. To provide proper operation of the bus receiver (the sensing amplifier), the minimum voltage difference $2^* dV_{min}$ (swing) between the lines may be about 0.05-- 0.20V. This low voltage swing is a basis to obtain high frequency of data transfer through the bus.

Figure 2 illustrates sensing amplifier 16. Preferably, the sensing amplifier is a cross-coupled latched amplifier.

The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode. The cross-coupled latched amplifier is isolated from the power buses (transistors 30 and 31 are turned off). Transistors 32 and 33 are turned on and thus, the bus voltage swing passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to V_{dd} and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high.

When the control input CLK is high and the bus driver is in the precharge mode, the sensing amplifier is in the data transfer mode. Transistors 32 and 33 are turned of and isolate the internal nodes IT and IC of the latched amplifier from the bus lines. The cross-coupled latched amplifier is connected to power buses (transistors 30 and 31 are turned on) and it begins to amplify the low voltage swings of the internal nodes IT

and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low.

The use of domino output stages in accordance with the present invention instead of static inverters is necessary to avoid leakage currents and output glitches, which may appear because potentials of nodes IT and IC are approximately equal to V_{pr} during the operating cycle of the bus driver. Weak PMOS transistors 34 and 35 are preferably included in the sensing amplifier to help prevent output glitches.

The data transfer arrangement in accordance with the present invention provides an increase in speed due to the differential low voltage swing bus driver in combination with the use of the latched differential sense amplifier as the bus receiver.

A further increase in speed is attained with the data transfer arrangement due to the pull up/pull down bus drivers, which provide equal low differential voltage swings +dV/ - dV in both bus lines. This allows both bus lines to be active during the data transfer phase, eliminates the necessity to use special circuits for holding the precharged level and leads to a reduction in the capacitance load of the driver.

The buses precharging to the specific level between ground and V_d ($V_{pr} = K*V_{dd}$, where K = 1/3 for the ideal MOS model) also provides: equal charge and discharge driver currents $I_{ch} = Id_{ch}$, provided by the NMOS pull up follower and the NMOS pull down switch, respectively, and therefore, equal differential voltage swings dV in both charged and discharged bus during the data transfer phase Pdtf: + dV = $I_{ch}*D_{dtf}/C_{LOAD}$; and -dV = $I_{dch}*T_{dtf}/C_{LOAD}$. I_{ch} represents the driver pull up output current (which provides the C_{LOAD} charging from V_{pr} up to V_{dd}); I_{dch} represents the driver pull down output current (providing the C_{LOAD} discharging from V_{pr} up to V_{ss}); C_{LOAD} represents the bus lines' compacitances; +dV represents the bus voltage change up from V_{pr} during data transfer phase; -dV represents the bus voltage change down from V_{pr} during data transfer phase; and T_{dtf} represents the data transfer phase duration. The buses precharging to the specific level between ground and V_{dd} also provides high noise immunity due to active mode for both buses that equal low output resistances of the drivers in pull up and pull down mode and; low total power consumed by drivers during the cycle of operation (transfer plus precharge).

The latched sense amplifier is faster due to the bus voltage swing passing directly to the high-gain nodes IT and IC of the cross- coupled latched amplifier, the lower number of stacked transistors that are connected between the supply voltage V_{dd} (or

V_{cc}) and nodes IT and IC, the fact that during latching of the IT and IC nodes, the nodes are charged by $K*V_{dd}$ and $(1-K)*V_{dd}$ instead of simply V_{dd}. Additionally, the speed of the latched sensing amplifier is effected little by the deviation of voltage V_{pr} and the deviation of the threshold voltage of the input transistors.

In addition to the higher speed and low power consumption of the data transfer arrangement in accordance with the present invention, the arrangement is also less sensitive to circuit parameters mismatching, data bus common mode noise and power buses' noises since both drivers are active during data transfer phase. During the appropriate bus precharge phase, the bus receiver is isolated from the bus lines.

Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus.

2. A data transfer arrangement in accordance with claim 1 wherein the latching sense amplifier comprises a cross coupled latched amplifier.

3. A data transfer arrangement in accordance with claim 1 wherein the bus drivers consist of active pull up/pull down bus drivers.

HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

ABSTRACT OF THE DISCLOSURE

A data transfer arrangement. The data transfer arrangement includes two active pull up/active pull down bus drivers and a voltage precharge source. A differential bus is coupled to the bus drivers and to the voltage precharge source. A latching sense amplifier is coupled to the differential bus and serves as the bus receiver. The bus drivers operate in a precharge phase and a data transfer phase. The bus receiver operates in an analogous but opposite manner, i.e., when the bus drivers are in the precharge phase, the bus receiver is in the data transfer phase and when the bus drivers are in the data transfer phase, the bus receiver is in a precharge phase

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which __X__ is attached hereto or ____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

J. Georg Seka, Reg. No. 24,491
Robert J. Bennett, Reg. No. 27,533
Charles E. Krueger, Reg. No. 30,077
Charles J. Kulas, Reg. No. 35,809
Kevin T. LeMond, Reg. No. 35,933
George B.F. Yee, Reg. No. 37,478
Chad S. Hilyard, Reg. No. 40,647
Gerald T. Gray, Reg. No. 41,797
Daniel D. Tagliaferri, Reg. No. 43,178
Thomas D. Franklin, Reg. No. 43,616
Patrick M. Boucher, Reg. No. 44,037

Send Correspondence to:	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)
Kevin T. LeMond **TOWNSEND and TOWNSEND and CREW LLP** **Two Embarcadero Center, 8th Floor** **San Francisco, California 94111-3834**	Name: Kevin T. LeMond Reg. No.: 35933 Telephone: 415-576-0200

Full Name of Inventor 1:	Last Name: **Podlesny**	First Name: **Andrew**	Middle Name or Initial: **V.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **Apt. 192, 38/2 Menzinsky St.**	City: **Moscow**	State/Country: **Russia**	Postal Code: **129281**
Full Name of Inventor 2:	Last Name: **Malshin**	First Name: **Alexander**	Middle Name or Initial: **V.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **Apt. 608, 50 Frunzenskaya Nabergnaya**	City: **Moscow**	State/Country: **Russia**	Postal Code: **119270**
Full Name of Inventor 3:	Last Name: **Solomatnikov**	First Name: **Alexander**	Middle Name or Initial: **Y.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **14, Bolshoi Savvinski Per.**	City: **Moscow**	State/Country: **Russia**	Postal Code: **119435**

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Andrew V. Podlesny	Alexander V. Malshin	Alexander Y. Solomatnikov
Date	Date	Date

SF 1060790 v1

Attorney Docket 020181-000500US (PPA-5)

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov
Application or Patent No.:
Filed or Issued:
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

[ ] the owner of the small business concern identified below
[X] an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Elbrus International Limited
Address of Small Business Concern: P.O. Box 265
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov described in:

[X] the specification filed herewith;
[ ] Application No. _____, filed _____;
[ ] Patent No. _____, issued _____.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim
Title of Person if Other than Owner: President
Address of Person Signing: 14 Bolshoy Savvinsky per.
Moscow 119435, Russia

Signature _____ Date 02/6/2000

SF 1058186 v1

Bib Data Sheet

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS-
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/505,656	02/17/2000 RULE _	326	2819	20181-5US

APPLICANTS

Andrew V. Podlesny, Moscow, RUSSIAN FEDERATION;
Alexander V. Malshin, Moscow, RUSSIAN FEDERATION;
Alexander Y. Solomatnikov, Moscow, RUSSIAN FEDERATION;

** CONTINUING DATA **********

THIS APPLN CLAIMS BENEFIT OF 60/120,531 02/17/1999

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 04/26/2000

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no 35 USC 119 (a-d) conditions met ☑ yes ☒ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	RUSSIAN FEDERATION	1	3	1

ADDRESS

20350

TITLE

High speed low power data transfer scheme

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
410	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number: 09/505,656

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	3 minus 20=	*
INDEPENDENT CLAIMS	1 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
	345.00	OR		690.00
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	690

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 8	Minus	** 20	=
Independent	* 2	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

jc678 U.S. PTO
09/505656
02/17/00

Class	Subclass.
326	95

ISSUE CLASSIFICATION

PATENT NUMBER
6366130
6366130

U.S. **UTILITY** Patent Application

O.I.P.E. SCANNED GTH(1) O.A. mc	PATENT DATE APR 0 2 2002

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/505656	D	326	95	2819	V. Tran

APPLICANTS
Andrew Podlesny
Alexander Malshin
Alexander Solomatnikov

TITLE
High speed low power data transfer scheme

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
326	95	326	86	87	90			
INTERNATIONAL CLASSIFICATION		327	57	55	52			
H03K 19/0185								
G11C 7/06								
					☐ Continued on Issue Slip Inside File Jacket			

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	1	2	1	8	1

☐ The term of this patent subsequent to _____ (date) has been disclaimed.	8/15/01 (Assistant Examiner) (Date)	NOTICE OF ALLOWANCE MAILED: 8/17/01
☐ The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____	Michael A Tokar (Primary Examiner) 8/16/01 (Date)	ISSUE FEE (1) — Amount Due: 620.- — Date Paid: 11-6-01
☐ The terminal ____ months of this patent have been disclaimed.	(Legal Instruments Examiner) (Date)	ISSUE BATCH NUMBER: K75

WARNING:
The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 6/99)

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in pocket on right inside flap)

Print Drawing: ___ sheet(s) ___

(FACE)

SEARCHED

Class	Sub.	Date	Exmr.
324	21-23	2-7-01	UTam
	26-28		
	30		
	86		
	87		
	90		
	93		
	95		
	98		
327	51-57		
updated above		5/18/01	UTam

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
Searched above		8/15/01	Utam

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.

(RIGHT OUTSIDE)

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	JMC		2/28/03
O.I.P.E. CLASSIFIER			
FORMALITY REVIEW	JW	65766	4-21-03
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✔ ..... Rejected
= ..... Allowed
— (Through numeral)... Canceled
÷ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

Claim Final	Claim Original	Date
1	1	10/15/04
	2	
2	3	=
3	4	
4	5	
5	6	
6	7	
7	8	
8	9	=
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
	31	
	32	
	33	
	34	
	35	
	36	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

Claim Final	Claim Original	Date
	51	
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
	66	
	67	
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
	77	
	78	
	79	
	80	
	81	
	82	
	83	
	84	
	85	
	86	
	87	
	88	
	89	
	90	
	91	
	92	
	93	
	94	
	95	
	96	
	97	
	98	
	99	
	100	

Claim Final	Claim Original	Date
	101	
	102	
	103	
	104	
	105	
	106	
	107	
	108	
	109	
	110	
	111	
	112	
	113	
	114	
	115	
	116	
	117	
	118	
	119	
	120	
	121	
	122	
	123	
	124	
	125	
	126	
	127	
	128	
	129	
	130	
	131	
	132	
	133	
	134	
	135	
	136	
	137	
	138	
	139	
	140	
	141	
	142	
	143	
	144	
	145	
	146	
	147	
	148	
	149	
	150	

If more than 150 claims or 10 actions staple additional sheet here

(LEFT INSIDE)

FORMALITIES LETTER

OC000000005078578

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENT AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

20350
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111

Date Mailed: 04/27/2000

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit **$ 690** *to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).*
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 820.**

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

FORMALITIES LETTER

OC000000005078578

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENT AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

20350
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111

OIPE JUN 27 2000 PATENT & TRADEMARK OFFICE JC56

Date Mailed: 04/27/2000

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit **$ 690** *to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).*
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 820.**

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

06/29/2000 GTEFFERA 00000070 201430 09505656

01 FC:201 345.00 CH
02 FC:205 65.00 CH

Secetvr

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Attn: Box Missing Parts
Washington, D.C. 20231

on 6/22/00

TOWNSEND and TOWNSEND and CREW LLP

By Kathryn Y. Lee

PATENT
Attorney Docket No. 20181-000500US
Client Ref. No.: PPA-5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Andrew V. Podlesny et al.

Application No.: 09/505,656

Filed: February 17, 2000

For: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

Examiner: Not Yet Assigned

Art Unit: 2819

TRANSMITTAL LETTER – RESPONSE TO NOTICE OF MISSING PARTS

Attn: Box Missing Parts
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice to File Missing Parts of Application - Filing Date Granted mailed April 27, 2000, enclosed are the following to be made of record in the above-identified application:

1) Executed Declaration and Power of Attorney
2) Verified Statement Claiming Small Entity Status
3) Copy of Notice of Missing Parts

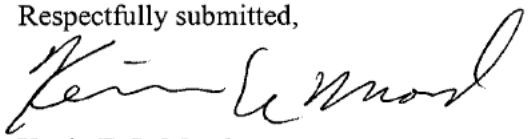
Please charge Deposit Account No. 20-1430 for the following fees:

Small entity:	(a)	Filing Fee (§ 1.16(a)) (Small Entity)	$ 345.00
	(c)	Missing Parts Surcharge	$ 65.00

TOTAL FEES TO BE CHARGED $410.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment, to Deposit Account No. 20-1430. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,



Kevin T. LeMond
Reg. No. 35, 933

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200
Fax (415) 576-0300
KTL:rgh

SF 1107691 v1

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which __ is attached hereto or __X__ was filed on February 17, 2000 as Application No. 09/505,656.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

J. Georg Seka, Reg. No. 24,491
Robert J. Bennett, Reg. No. 27,533
Charles E. Krueger, Reg. No. 30,077
Charles J. Kulas, Reg. No. 35,809
Kevin T. LeMond, Reg. No. 35,933
George B.F. Yee, Reg. No. 37,478
Chad S. Hilyard, Reg. No. 40,647
Gerald T. Gray, Reg. No. 41,797
Daniel D. Tagliaferri, Reg. No. 43,178
Thomas D. Franklin, Reg. No. 43,616
Patrick M. Boucher, Reg. No. 44,037

Send Correspondence to:	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)
Kevin T. LeMond **TOWNSEND and TOWNSEND and CREW LLP** **Two Embarcadero Center, 8th Floor** **San Francisco, California 94111-3834**	Name: Kevin T. LeMond Reg. No.: 35933 Telephone: 415-576-0200

Full Name of Inventor 1:	Last Name: **Podlesny**	First Name: **Andrew**	Middle Name or Initial: **V.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **Apt. 192, 38/2 Menzinsky St.**	City: **Moscow**	State/Country: **Russia**	Postal Code: **129281**
Full Name of Inventor 2:	Last Name: **Malshin**	First Name: **Alexander**	Middle Name or Initial: **V.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **Apt. 608, 50 Frunzenskaya Nabergnaya**	City: **Moscow**	State/Country: **Russia**	Postal Code: **119270**
Full Name of Inventor 3:	Last Name: **Solomatnikov**	First Name: **Alexander**	Middle Name or Initial: **Y.**	
Residence and Citizenship:	City: **Moscow**	State/Foreign Country: **Russia**	Country of Citizenship: **Russia**	
Post Office Address:	Post Office Address: **14, Bolshoi Savvinski Per.**	City: **Moscow**	State/Country: **Russia**	Postal Code: **119435**

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Andrew V. Podlesny	Alexander V. Malshin	Alexander Y. Solomatnikov
Date 06/14/2000	Date 06/14/2000	Date 06/14/2000

SF 1060790 v1

Attorney Docket 020181-000500US (PPA-5)

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov
Application or Patent No.:
Filed or Issued:
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

[ ] the owner of the small business concern identified below
[X] an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Elbrus International Limited
Address of Small Business Concern: P.O. Box 265
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov described in:

[X] the specification filed herewith;
[ ] Application No. _____, filed _____;
[ ] Patent No. _____, issued _____.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim
Title of Person if Other than Owner: President
Address of Person Signing: 14 Bolshoy Savvinsky per.
Moscow 119435, Russia

Signature _____ Date 02/6/2000

SF 1058186 v1

2819

PATENT

Attorney Docket No.: 20181-000500US

Client Reference No.: PPA-5

#5/Supp
IDS
3/2/01

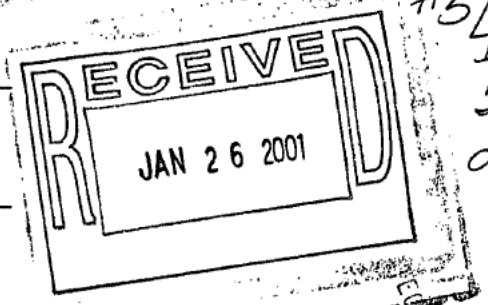
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

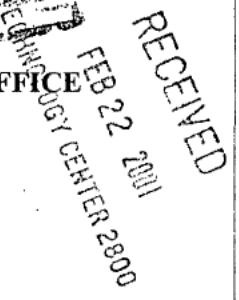
Assistant Commissioner for Patents
Washington, D.C. 20231

On 1/24/01

TOWNSEND and TOWNSEND and CREW LLP

By: Olivia





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Andrew V. Podlesny et al.

Application No.: 09/505,656

Filed: Herewith

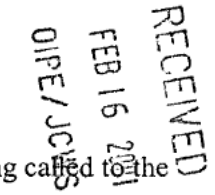
For: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

Examiner: Unassigned

Art Unit: 2819

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

Assistant Commissioner for Patents
Washington, D.C. 20231



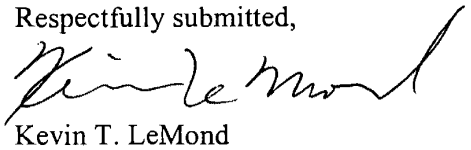
Sir:

The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copy of the reference is enclosed. It is respectfully requested that the cited reference be expressly considered during the prosecution of this application, and the reference be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Kevin T. LeMond
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
KTL:lo

SF 1178827 v1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/505,656	02/17/00	PODLESNY A	20181-5US

020350 MM92/0222
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-3834

EXAMINER	
TAN, V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 02/22/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Office Action Summary	Application No.	Applicant(s)	
	09/505,656	PODLESNY ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Objections

1. In claims 2 and 3 Change "A" to "The".

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. PAT. 5,598,371) in view of Hayakawa (U.S. PAT. 6,184,722 B1).

Lee et al. teaches all claimed features of claim 1 in Fig. 1, a data transfer arrangement comprising: two bus drivers (114, 116; 120, 122); a differential bus (line DIO and line DIOB) coupled to the bus drivers and to the voltage precharge source (PRECH); with the exception of teaching a latching sense amplifier coupled to the differential bus. However, Hayakawa teaches in Fig. 5A a latching sense amplifier (2) coupled to the differential bus (4, 6).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicants' invention to have combined the circuit of Lee et al. along with the circuit of Hayakawa to provide a sense amplifier that can sense a low level differential quickly and can amplifier low level differential small swing input signals.

Regarding claim 2, Hayakawa further teaches in Fig. 5A the data transfer arrangement of claim 1, wherein the latching sense amplifier comprises a cross coupled latch amplifier (Q3-Q6).

Regarding claim 3, Lee et al. further teaches in Fig. 1, the data transfer arrangement of claim 1, wherein the bus drivers consist of active pull up/pull down bus drivers (114, 114, 120, 122).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Proebsting teaches a differential sense amplifier circuit. Shiratake teaches a sense amplifier circuit. Yamauchi teaches a signal transmitting circuit, small receiving circuit, signal transmitting/receiving circuit. Yoon teaches a sense amplifiers including bipolar transistor input buffers and field effect transistor latch circuits. Decuir teaches a system and method for a switch data bus termination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

PATRICK WAMSLEY
PRIMARY EXAMINER

Vibol Tan

Patent Examiner, AU 2819

Notice of References Cited	Application/Control No. 09/505,656	Applicant(s)/Patent Under Reexamination PODLESNY ET AL.	
	Examiner Vibol Tan	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
	A	US-6154064-	11-2000	Proebsting	327	55
	B	US-6147514-	11-2000	Shiratake	327	55
	C	US-6028455-	02-2000	Yamauchi	327	52
	D	US-6184722-B1	02-2001	Hayakawa	327	55
	E	US-5894233-	04-1999	Yoon	327	55
	F	US-5781028-	07-1998	Decuir	326	30
	G	US-5598371-	01-1997	Lee et al.	365	189.05
	H	US- -				
	I	US- -				
	J	US- -				
	K	US- -				
	L	US- -				
	M	US- -				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification	
	N	- -					
	O	- -					
	P	- -					
	Q	- -					
	R	- -					
	S	- -					
	T	- -					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On July 20, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Julie Taylor Clough

PATENT
Attorney Docket No.: 20181-5
Client Reference No.: PPA-5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Andrew V. Podlesny et al.

Application No.: 09/505,656

Filed: June 27, 2000

For: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

Examiner: Vibol Tan

Art Unit: 2819

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants request a two-month extension of time from May 22, 2001 to July 22, 2001 and authorize the Commissioner to charge the fee therefor to our deposit account in accordance with the attached Fee Transmittal.

In response to the Office Action mailed February 22, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1 and 3. Please cancel claim 2 and add new claims 4-9.

1. (AMENDED) A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

07/25/2001 HABRHAB1 00000017 201430 09505656
01 FC:216 195.00 CH

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage.

2. (AMENDED) The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers.

3. (NEW) The data transfer arrangement in accordance with claim 1, wherein the first stage of the latching sense amplifier comprises:

a plurality of input pass transistors each having a gate, a source terminal, and a drain; and

a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain;

wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass transistors is coupled to an input, the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input, and the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input.

4. (NEW) The data transfer arrangement in accordance with claim 1, wherein the output stage of the latching sense amplifier comprises:

a plurality of input transistors each having a gate, a source terminal, and a drain; and

a pair of cross-coupled PMOS transistors each having a gate, a source terminal, and a drain;

a first PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of the first of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the first of the input transistors; and

a second PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of a second of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the second of the input transistors;

wherein the sources of the input transistors are coupled to a source of an NMOS transistor having a gate coupled to a clock signal input;

wherein the sources of the cross-coupled PMOS transistors are coupled to a voltage supply, the drains of the cross-coupled PMOS transistors are coupled to the drains of the input transistors; and

wherein the drains of the cross-coupled transistors provide a true and a complement phase of a data output signal.

93
Cont

5 6. (NEW) The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.

6 7. (NEW) The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.

7 8. (NEW) The data transfer arrangement in accordance with claim 3 wherein the active pull up and pull down bus drivers are NMOS transistors.

8 9. (NEW) A method of operation of a data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

9

A

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input, and

wherein the sense amplifier operates in two phases:

a precharge phase and a data transfer phase;

wherein the precharge phase operates when a control input clock signal is low, said phase comprising the steps of:

isolating the cross-coupled latch amplifier from a plurality of power buses by turning off an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to the inverted clock signal input;

passing a bus voltage swing to a plurality of internal nodes IT and IC of the latched amplifier;

93
Cont

precharging both dynamic gates to Vdd; and

providing a high true phase and a high complement phase of a data output signal; and

wherein the data transfer phase operates when a control input clock signal is high, said phase comprising the steps of:

isolating the internal nodes of the latched amplifier from the bus lines by turning off the pass input transistors;

connecting the cross-coupled latched amplifier to power buses by turning on an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to an inverted clock signal input;

amplifying each low voltage swing of the internal nodes to full logic levels;

discharging an output node of one of the dynamic gates to ground; and

providing a low true phase and a low complement phase of the data output signal.

10

REMARKS

Upon entry of this Amendment, which amends claims 1 and 3, cancels claim 2, and adds claims 4-9, claims 1 and 3-9 remain pending.

Claims 1-3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. PAT. 5,598,371) in view of Hayakawa (U.S. PAT. 6,184,722 B1).

These rejections are respectfully traversed and reconsideration is respectfully requested on the grounds that the Examiner has not shown claim 1 would have been obvious in view of prior art.

With regard to Lee et al., it is respectfully submitted that Lee et al. teaches a data transfer arrangement comprising two bus drivers and a differential bus coupled to the bus drivers and to the voltage precharge source (PRECH), where the voltage precharge source (PRECH) is coupled to a supply voltage Vcc.

In contrast, the present invention teaches precharging the buses to a specific level between ground and Vdd (Vpr = K*Vdd, where K is precharging voltage factor), as set out in the specification on page 4, lines 16-30. Precharging the buses to a specific level between ground and Vdd results in equal low differential voltage swings +dV,-Vd, providing increased speed of data transfer, high noise immunity due to the active mode and equal low output resistance of the driver in pull up and pull down modes, and low power consumption by the drivers during the cycle of operation.

Hayakawa teaches a latching sense amplifier coupled to the differential bus. Applicant respectfully submits that the circuit implementation of the latching sense amplifier in Hayakawa is different from the present embodiment.

The latch-type sense amplifier of the present invention has an output stage to avoid leakage currents and output glitches, which may appear because the potentials of nodes IT and IC are approximately equal to Vpr during the operating cycle of bus driver because the bus driver is precharged to a predetermined level between the ground and the supply voltage. Hayakawa does not teach a latching sense amplifier comprising two stages, where the input of the output stage is coupled to the output of the first stage.

The sources of cross-coupled latch amplifier NMOS transistors of the Hayakawa latch-type sense amplifier are coupled to the drains of the input pass transistors Q1 and Q2. In the present invention the sources of cross-coupled latch amplifier NMOS transistors are coupled to the drain of NMOS transistor N1, having a gate coupled to the clock signal input. The drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier MOS transistors and the input swing passes directly to the high-gain nodes IT and IC of the cross-coupled latched amplifier, providing a higher noise immunity than Hayakawa's.

In the present invention the sources of the PMOS transistors are coupled to the drain of a PMOS transistor having a gate coupled to the inverted clock input, whereas Hayakawa discloses a latch-type sense amplifier with the sources of the PMOS transistors coupled to the supply voltage.

Thus, it is respectfully submitted that none of the prior art, either alone or in combination, discloses, teaches or even suggests the latch-type sense amplifier disclosed in the present invention. Accordingly it is respectfully submitted that claim 1 is allowable.

Claims 3-8 depend, either directly or indirectly on claim 1 and, therefore, they are allowable for at least the reasons claim 1 is allowable. These claims further define and augment the features of applicant's invention.

New independent claim 9 was added. Claim 9 is directed to a method of operation of a data transfer arrangement. The support for claim 9 can be found in Specification on pages 2-5, lines 22-12. As discussed above none of the cited prior art references teach a data transfer arrangement as disclosed in the present invention, and, therefore claim 9 is allowable.

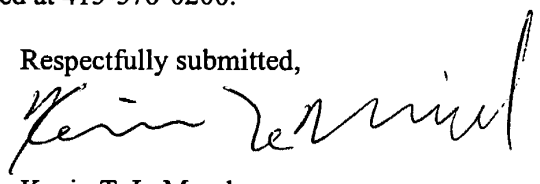
CONCLUSION:

Attached hereto is a marked-up version of the changes made to the claims by the current amendment along with a complete set of claims has been provided for convenience. The attached pages are captioned "Version With Markings To Show Changes Made" and "Claims Appendix."

In view of the foregoing, applicant submits that this application is now in condition for allowance. The issuance of a formal notification to that effect at an early date is requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Kevin T. LeMond
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
KTL/OV/jtc
SF 1237142 v3

Versions with Markings to Show Changes Made

1. (AMENDED) A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage.

3. (AMENDED) The data transfer arrangement in accordance with claim 1 wherein the bus drivers [**consist of**] comprise active pull-up and active pull-down bus drivers.

A

Claims Appendix

1. (AMENDED) A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage.

2. (CANCELED)

3. (AMENDED) The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers.

4. (NEW) The data transfer arrangement in accordance with claim 1, wherein the first stage of the latching sense amplifier comprises:

a plurality of input pass transistors each having a gate, a source terminal, and a drain; and

a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain;

wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass transistors is coupled to an input, the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input, and the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input.

A

5. (NEW) The data transfer arrangement in accordance with claim 1, wherein the output stage of the latching sense amplifier comprises:

a plurality of input transistors each having a gate, a source terminal, and a drain; and

a pair of cross-coupled PMOS transistors each having a gate, a source terminal, and a drain;

a first PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of the first of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the first of the input transistors; and

a second PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of a second of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the second of the input transistors;

wherein the sources of the input transistors are coupled to a source of an NMOS transistor having a gate coupled to a clock signal input;

wherein the sources of the cross-coupled PMOS transistors are coupled to a voltage supply, the drains of the cross-coupled PMOS transistors are coupled to the drains of the input transistors; and

wherein the drains of the cross-coupled transistors provide a true and a complement phase of a data output signal.

6. (NEW) The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.

7. (NEW) The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.

A

8. (NEW) The data transfer arrangement in accordance with claim 3 wherein the active pull up and pull down bus drivers are NMOS transistors.

9. (NEW) A method of operation of a data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input, and

wherein the sense amplifier operates in two phases:

a precharge phase and a data transfer phase;

wherein the precharge phase operates when a control input clock signal is low, said phase comprising the steps of:

isolating the cross-coupled latch amplifier from a plurality of power buses by turning off an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to the inverted clock signal input;

passing a bus voltage swing to a plurality of internal nodes IT and IC of the latched amplifier;

precharging both dynamic gates to Vdd; and

providing a high true phase and a high complement phase of a data output signal; and

wherein the data transfer phase operates when a control input clock signal is high, said phase comprising the steps of:

isolating the internal nodes of the latched amplifier from the bus lines by turning off the pass input transistors;

connecting the cross-coupled latched amplifier to power buses by turning on an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to an inverted clock signal input;

amplifying each low voltage swing of the internal nodes to full logic levels;

discharging an output node of one of the dynamic gates to ground; and

providing a low true phase and a low complement phase of the data output signal.

GAU 2819

Please type a plus sign (+) inside this box → [+]

PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

JC34 JUL 23 2001 PATENT TRADEMARK OFFICE

RECEIVED JUL 27 2001 TECHNOLOGY CENTER 2800

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/505,656
Filing Date	June 27, 2000
First Named Inventor	Andrew V. Podlesny, et al.
Group Art Unit	2819
Examiner Name	Vibol Tan
Total Number of Pages in This Submission: 14	Attorney Docket Number: 020181000500

ENCLOSURES *(check all that apply)*

☒ Fee Transmittal Form	☐ Assignment Papers *(for an Application)*	☐ After Allowance Communication to Group
☐ Fee Attached	☐ Drawing(s)	☐ Appeal Communication to Board of Appeals and Interferences
☒ Amendment / Response	☐ Licensing-related Papers	☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
☐ After Final	☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Petition to Convert to a Provisional Application	☐ Status Letter
☒ Extension of Time Request	☐ Power of Attorney, Revocation Change of Correspondence Address	☒ Other Enclosure(s) *(please identify below)*: Return Postcard
☐ Express Abandonment Request	☐ Terminal Disclaimer	
☐ Information Disclosure Statement	☐ Request for Refund	
☐ Certified Copy of Priority Document(s)	☐ CD, Number of CD(s)	
☐ Response to Missing Parts/ Incomplete Application	Remarks: The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430. **APPLICANTS HEREBY REQUEST A 2-MONTH EXTENSION OF TIME.**	
☐ Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm and Individual name	Townsend and Townsend and Crew LLP Kevin T. LeMond Reg No. 35,933
Signature	Kevin LeMond
Date	July 20, 2001

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: July 20, 2001

Typed or printed name	Julie Taylor Clough		
Signature	Julie Taylor Clough	Date	July 20, 2001

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be send to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.
SF 1249297 v1

A

PTO/SB/17 (09-00)
Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

Complete if Known	
Application Number	09/505,656
Filing Date	June 27, 2000
First Named Inventor	Andrew V. Podlesny, et al.
Examiner Name	Vibol Tan
Group Art Unit	2819
Attorney Docket No.	020181-000500US

TOTAL AMOUNT OF PAYMENT ($) 195.00

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☒ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ **Payment Enclosed:**

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	=	Fee Paid
Total Claims		-20**	=		X	=	
Independent Claims		-3**	=		X	=	
Multiple Dependent					X	=	

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	195
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,240	241	620	Petition to revive – unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

The Commissioner is authorized to charge any additional fees to the above noted Deposit Account.

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)195

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Kevin T. LeMond	Registration No. (Attorney/Agent)	35,933	Telephone	415-576-0200
Signature				Date	July 20, 2001

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231. SF 1249286 v1

I hereby certify that this correspondence is being sent by facsimile transmission to: 1 703 – 746-4043
Examiner Vibol Tan
Patent & Trademark Office
Washington, DC 20231

On August 14, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: _____
Lata Olivier

PATENT

FAX RECEIVED
AUG 14 2001
T.C. 2800

#7/B
8/16/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Vibol Tan
Andrew V. Podlesny et al.	Art Unit: 2819
Application No.: 09/505,656	SUPPLEMENTAL AMENDMENT
Filed: June 27, 2000	
For: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to our telephone conversation of this morning attached is Supplemental Amendment to Claim 1.

IN THE CLAIMS:

1. (TWICE AMENDED) A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

B1

11

B

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage;

wherein the differential bus and the differential data bus are precharged to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

Kevin T. LeMond
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
KTL:lo
SF 1258563 v1

12

Version With Markings To Show Changes Made

IN THE CLAIMS:

1. (TWICE AMENDED) A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage[.];

wherein the differential bus and the differential data bus are precharged to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor.

B

Atty Docket No. 020181-000400

PTO FAX NO.: **1 703- 746-4043**

ATTENTION: Examiner Vibol Tan
Group Art Unit 2819

OFFICIAL COMMUNICATION

FOR THE PERSONAL ATTENTION OF

EXAMINER Vibol Tan

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following documents, in re Application of Podlesney et al., Application No. 09/505,656, filed June 27, 2000, for HIGH SPEED LOW POWER DATA TRANSFER SCHEME is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Documents Attached

1. SUPPLEMENTAL AMENDMENT TO CLAIM 1

Number of pages being transmitted, including this page: 3

Dated: August 14, 2001

Lata Olivier

PLEASE CONFIRM RECEIPT OF THIS PAPER BY RETURN FACSIMILE AT (415) 576-0300

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834
Telephone: (415) 576-0200
Fax: (415) 576-0300
SF 1258556 v1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

020350 MM91/0817
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-3834

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/505,656	02/17/00	008	TAN, V 2819	08/17/01
First Named Applicant PODLESNY,		35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 20181-5US	326-095.000	K75	UTILITY	YES	$620.00	11/19/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/505,656	02/17/00	PODLESNY	A	20181-5US

020350 MM91/0817
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-3834

EXAMINER	
TAN, V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 08/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Notice of Allowability	Application No.	Applicant(s)	
	09/505,656	PODLESNY ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the supplemental amendment filed 08/14/2001*.
2. ☒ The allowed claim(s) is/are *1 and 3-9*.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☒ Information Disclosure Statements (PTO-1449), Paper No. *5*.
6☐ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

DETAILED ACTION

1. The application having been allowed, formal drawings are required in response to this Office Action.

2. The following is an examiner's statement of reasons for allowance: applicants' arguments have been fully considered and deemed to be persuasive. The present invention teaches precharging the buses to a specific level between ground and Vdd, which results in equal low differential voltage swings, providing increased speed of data transfer. The prior art of Lee et al. does not teach such precharging buses as described above.

3. Claims 1 and 3-9 are allowed. Applicants have canceled claim 2.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan

Patent Examiner, AU 2819

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800

FORM PTO-1449 (Modified)	Attorney Docket No.: 20181-000500US	Application No.: 09/505,656
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: Andrew V. Podlesny et al.	
	Filing Date: February 17, 2000	Group: 2819

Reference Designation — **U.S. PATENT DOCUMENTS** — Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
A	Article "On the Parallel Evaluation of Polynomials"in IEEE Transactions On Computer, Vol. C-22, No. 1, January 1973 by Kiyoshi Maruyama					
B						
C						
D						
E						

EXAMINER — DATE CONSIDERED 8/9/01

OIPE JC46 JAN 26 2001 PATENT & TRADEMARK OFFICE

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

RECEIVED
FEB 22 2001
TECHNOLOGY CENTER 2800

Form PTO 948 (Rev. 03/01) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 09/505656

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 2/17/00 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ___ Color drawings are not acceptable until petiton is granted. Fig(s) ___
   - ___ Pencil and non black ink not permitted. Fig(s) ___
2. PHOTOGRAPHS. 37 CFR 1.84(b)
   - ___ Full-tone set is required. Fig(s) ___
   - ___ Photographs may not be mounted. 37 CFR 1.84(c)
   - ___ Poor quality (half-tone). Fig(s) ___
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ___ Paper not flexible, strong, white, and durable. Fig(s) ___
   - ___ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) ___
   - ___ Mylar, velum paper is not acceptable (too thin). Fig(s) ___
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - ___ 21.0 cm by 29.7 cm (DIN size A4)
   - ___ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ___ All drawing sheets not the same size. Sheet(s) ___
   - ___ Drawings sheets not an acceptable size. Fig(s) ___
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
   - Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm SIZE: A4 Size
   - Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm SIZE: 8 1/2 x 11
   - Margins not acceptable. Fig(s) 1-2
   - ☒ Top (T) ☒ Left (L) ___ Right (R) ___ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   - REMINDER: Specification may require revision to correspond to drawing changes.
   - Partial views. 37 CFR 1.84(h)(2)
   - ___ Brackets needed to show figure as one entity. Fig(s) ___
   - ___ Views not labeled separately or properly. Fig(s) ___
   - ___ Enlarged view not labeled separately or properly. Fig(s) ___
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   - ___ Hatching not indicated for sectional portions of an object. Fig(s) ___
   - ___ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) ___
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) ___
9. SCALE. 37 CFR 1.84(k)
   - ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) ___
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
    - ___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) ___
11. SHADING. 37 CFR 1.84(m)
    - ___ Solid black areas pale. Fig(s) ___
    - ___ Solid black shading not permitted. Fig(s) ___
    - ___ Shade lines, pale, rough and blurred. Fig(s) ___
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    - ___ Numbers and reference characters not plain and legible. Fig(s) 1-2
    - ___ Figure legends are poor. Fig(s) ___
    - ___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) ___
    - ___ English alphabet not used. 37 CFR 1.84(p)(2) Figs ___
    - ___ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) ___
13. LEAD LINES. 37 CFR 1.84(q)
    - ___ Lead lines cross each other. Fig(s) ___
    - ___ Lead lines missing. Fig(s) ___
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    - ___ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) ___
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) ___
16. CORRECTIONS. 37 CFR 1.84(w)
    - ___ Corrections not made from prior PTO-948 dated ___
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ___ Surface shading shown not appropriate. Fig(s) ___
    - ___ Solid black shading not used for color contrast. Fig(s) ___

COMMENTS

REVIEWER ___ DATE 8/15/01 TELEPHONE NO 308-0011

ATTACHMENT TO PAPER NO. ___

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities – 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

020350 MM91/0817
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-3834

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Donald Mixon (Depositor's name)

(Signature)

November 6, 2001 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/505,656	02/17/00	008	TAN, V 2819	08/17/01

First Named Applicant: PODLESNY,

35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 20181-5US	326-095.000	K75	UTILITY	YES	$640.00	11/19/01

1. Change of correspondence address or indication of " Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Townsend and Townsend and Crew LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Elbrus International Limited

(B) RESIDENCE: (CITY & STATE OR COUNTRY) George Town Grand Cayman, Grand Cayman Islands

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☐ Issue Fee

☐ Advance Order - # of Copies _____

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER 20-1430

(ENCLOSE AN EXTRA COPY OF THIS FORM)

☒ Issue Fee

☐ Advance Order - # of Copies 11

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Kevin T. LeMond, Reg. 35,933 (Date) 11/06/01

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

02/05/2002 EAREGAY2 00000153 201430 09505656

01 FC:242 640.00 CH
02 FC:561 33.00 CH

TRANSMIT THIS FORM WITH FEE

2-1-2

PTO UTILITY GRANT
Paper Number 6

The Commissioner of Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to an statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

Bruce Lehman
Commissioner of Patents and Trademarks

Attest Mary [illegible]

The United States of America

PATENT AND TRADEMARK OFFICE
UNITED STATES OF AMERICA

Form PTO-1584 (Rev. 2/97)

FPI-LOM

(RIGHT INSIDE)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Box Issue Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

On November 6, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: _____

PATENT
Attorney Docket No.: 020181-000500US

#9 Rec'd

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: E. Peavey
Andrew V. Podlesny et al.	Art Unit: 3626
Application No.: 09/505,656	
Filed: February 17, 2000	TRANSMITTAL OF FORMAL DRAWINGS
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	

Box Issue Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

Attn: Official Draftsman

Sir:

Applicant submits herewith a set of corrected drawings in connection with the above captioned application. The new drawings includes the changes required by the Examiner in form of the Examiner's Comment which was issued in conjunction with the Notice of Allowance and Issue Fee dated August 17, 2001.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

Kevin T. LeMond
Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
KTL/dxm
SF 1298073 v1

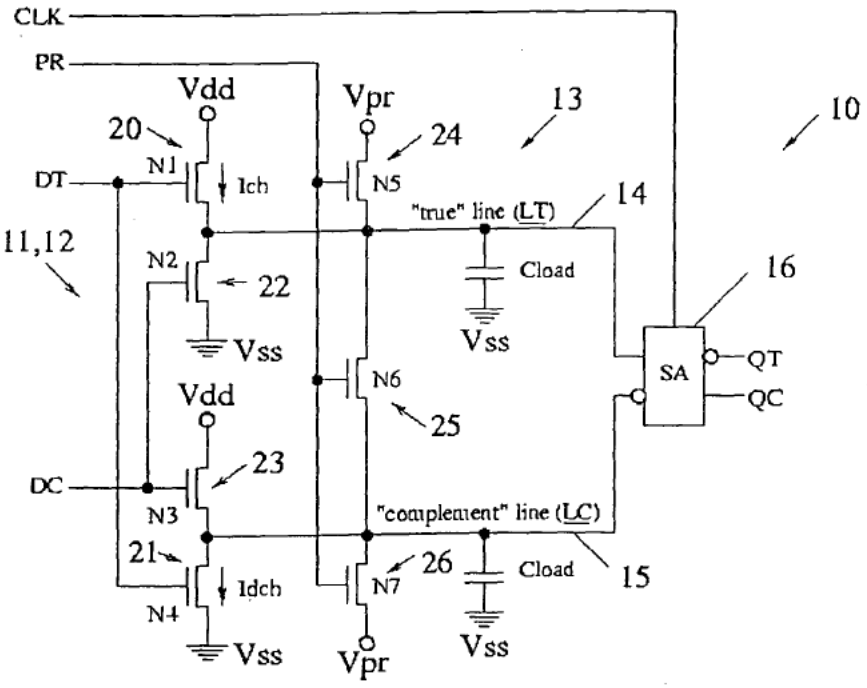

CLK
PR
Vdd
Vpr
13
10
20
24
N1
Ich
N5
DT
"true" line (LT)
14
11,12
N2
22
Cload
16
Vss
Vss
QT
SA
N6
Vdd
25
QC
23
DC
N3
"complement" line (LC)
21
26
Cload
15
Idch
N7
N4
Vss
Vpr
Vss
Bus drivers
Precharge circuit
Bus lines
Bus reciever

FIG.1.

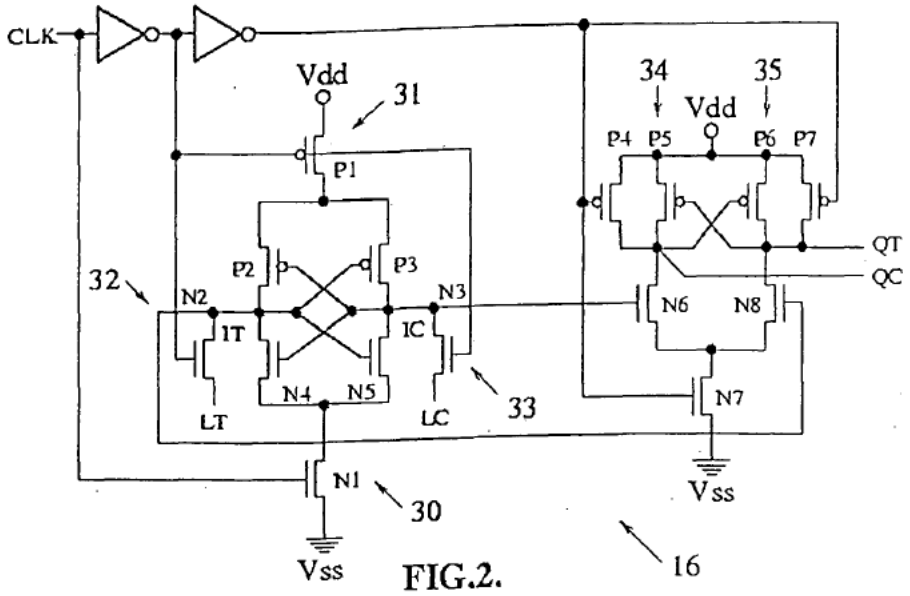

CLK
Vdd
31
P1
32
P2
P3
N2
N3
1T
1C
N4
N5
LT
LC
33
N1
30
Vss
34
35
Vdd
P4
P5
P6
P7
QT
QC
N6
N8
N7
Vss
16

FIG.2.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11.

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julie Taylor Clough

PATENT
Docket No.: 020181-000500US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.:
Andrew V. Podlesny, et al.	Examiner:
Patent No.: 6,366,130	Art Unit:
Issued: April 2, 2002	CORRECTION OF ENTITY STATUS AND PAYMENT OF DEFICIENCY OWED UNDER 37 CFR §§ 1.27(g) and 1.28(c)
Application No.: 09/505,656	
Filed: February 17, 2000	
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	
Customer No.: 20350	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

The following submission of deficiency payment and itemization is believed to meet the requirements of 37 C.F.R. §§ 1.28(c)(1) and (c)(2). Furthermore, Applicants understand that under 37 CFR § 1.28(d) this submission is treated under § 1.27(g)(2) as a notification of loss of entitlement to small entity status. Therefore, Applicants respectfully request the deficiency payment be processed and the correct entity status be accorded to the application.

ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

DATE OF PAYMENT	TYPE OF FEE	SMALL ENTITY FEE ACTUALLY PAID	(CURRENT) LARGE ENTITY FEE FOR ACTION	DEFICIENCY PAYMENT OWED
June 22, 2000	Filing	$345	$850	$505
June 22, 2000	Missing Parts Surcharge	$65	$130	$65
November 6, 2001	Issue Fee	$640	$1510	$870
October 3, 2005	4th Maintenance Fee	$450	$980	$530
September 22, 2009	8th Maintenance Fee	$1240	$2480	$1240
				Total $3210

TOTAL DEFICIENCY PAYMENT OWED: $3210

Applicant hereby authorizes the Commissioner to deduct the total deficiency owed of $3210 from Deposit Account No. 20-1430. Please deduct any additional fees due from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

J. Georg Seka
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
JGS:jtc
63318995 v1

Electronic Acknowledgement Receipt	
EFS ID:	10032923
Application Number:	09505656
International Application Number:	
Confirmation Number:	7462
Title of Invention:	High speed low power data transfer scheme
First Named Inventor/Applicant Name:	Andrew V. Podlesny
Customer Number:	20350
Filer:	J. Georg Seka/Julie Clough
Filer Authorized By:	J. Georg Seka
Attorney Docket Number:	20181-5US
Receipt Date:	05-MAY-2011
Filing Date:	17-FEB-2000
Time Stamp:	19:02:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Entity_020181_005000US.pdf	68881 60745883f62fa9632990d7e6fdf029592bbdc8aa	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	68881

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

#10

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julia Taylor Clough

PATENT
Docket No.: 020181-000500US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.:
Andrew V. Podlesny, et al.	Examiner:
Patent No.: 6,366,130	Art Unit:
Issued: April 2, 2002	CORRECTION OF ENTITY STATUS AND PAYMENT OF DEFICIENCY OWED UNDER 37 CFR §§ 1.27(g) and 1.28(c)
Application No.: 09/505,656	
Filed: February 17, 2000	
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	
Customer No.: 20350	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

The following submission of deficiency payment and itemization is believed to meet the requirements of 37 C.F.R. §§ 1.28(c)(1) and (c)(2). Furthermore, Applicants understand that under 37 CFR § 1.28(d) this submission is treated under § 1.27(g)(2) as a notification of loss of entitlement to small entity status. Therefore, Applicants respectfully request the deficiency payment be processed and the correct entity status be accorded to the application.

ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

DATE OF PAYMENT	TYPE OF FEE	SMALL ENTITY FEE ACTUALLY PAID	(CURRENT) LARGE ENTITY FEE FOR ACTION	DEFICIENCY PAYMENT OWED
June 22, 2000	Filing	$345	$850	$505
June 22, 2000	Missing Parts Surcharge	$65	$130	$65
November 6, 2001	Issue Fee	$640	$1510	$870
October 3, 2005	4th Maintenance Fee	$450	$980	$530
September 22, 2009	8th Maintenance Fee	$1240	$2480	$1240
				Total $3210

TOTAL DEFICIENCY PAYMENT OWED: $3210

Applicant hereby authorizes the Commissioner to deduct the total deficiency owed of $3210 from Deposit Account No. 20-1430. Please deduct any additional fees due from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

J. Georg Seka
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
JGS:jtc
63318995 v1

Electronic Acknowledgement Receipt

EFS ID:	10032923
Application Number:	09505656
International Application Number:	
Confirmation Number:	7462
Title of Invention:	High speed low power data transfer scheme
First Named Inventor/Applicant Name:	Andrew V. Podlesny
Customer Number:	20350
Filer:	J. Georg Seka/Julie Clough
Filer Authorized By:	J. Georg Seka
Attorney Docket Number:	20181-5US
Receipt Date:	05-MAY-2011
Filing Date:	17-FEB-2000
Time Stamp:	19:02:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Entity_020181_005000US.pdf	68881 607458831f62fa9632990d7e6fdf029592bbdc8aa	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	68881

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julie Taylor Clough

PATENT
Docket No.: 020181-000500US

05/16/2011 DALLEN 00000005 201430 09505656
01 FC:1461 1440.00 DA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2011 MAY -9 PM 4:20

In re application of:	Confirmation No.:
Andrew V. Podlesny, et al.	Examiner:
Patent No.: 6,366,130	Art Unit:
Issued: April 2, 2002	CORRECTION OF ENTITY STATUS AND PAYMENT OF DEFICIENCY OWED UNDER 37 CFR §§ 1.27(g) and 1.28(c)
Application No.: 09/505,656	
Filed: February 17, 2000	
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	
Customer No.: 20350	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

The following submission of deficiency payment and itemization is believed to meet the requirements of 37 C.F.R. §§ 1.28(c)(1) and (c)(2). Furthermore, Applicants understand that under 37 CFR § 1.28(d) this submission is treated under § 1.27(g)(2) as a notification of loss of entitlement to small entity status. Therefore, Applicants respectfully request the deficiency payment be processed and the correct entity status be accorded to the application.

05/16/2011 DALLEN 00000006 201430 6366130
01 FC:1599 1770.00 DA

ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

DATE OF PAYMENT	TYPE OF FEE	SMALL ENTITY FEE ACTUALLY PAID	(CURRENT) LARGE ENTITY FEE FOR ACTION	DEFICIENCY PAYMENT OWED
June 22, 2000	Filing	$345	$850	$505
June 22, 2000	Missing Parts Surcharge	$65	$130	$65
November 6, 2001	Issue Fee	$640	$1510	$870
October 3, 2005	4th Maintenance Fee	$450	$980	$530
September 22, 2009	8th Maintenance Fee	$1240	$2480	$1240
				Total $3210

TOTAL DEFICIENCY PAYMENT OWED: $3210

Applicant hereby authorizes the Commissioner to deduct the total deficiency owed of $3210 from Deposit Account No. 20-1430. Please deduct any additional fees due from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

J. Georg Seka
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
JGS:jtc
63318995 v1

#11

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, via EFS web on 5-5-11

KILPATRICK TOWNSEND & STOCKTON LLP

By: Julia Taylor Clough

PATENT
Docket No.: 020181-000500US

05/16/2011 DALLEN 00000005 201430 09505656
01 FC:1461 1440.00 DA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2011 MAY -9 PM 4:20

In re application of:	Confirmation No.:
Andrew V. Podlesny, et al.	Examiner:
Patent No.: 6,366,130	Art Unit:
Issued: April 2, 2002	CORRECTION OF ENTITY STATUS AND PAYMENT OF DEFICIENCY OWED UNDER 37 CFR §§ 1.27(g) and 1.28(c)
Application No.: 09/505,656	
Filed: February 17, 2000	
For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME	
Customer No.: 20350	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-identified issued patent is no longer entitled to small entity status.

The following submission of deficiency payment and itemization is believed to meet the requirements of 37 C.F.R. §§ 1.28(c)(1) and (c)(2). Furthermore, Applicants understand that under 37 CFR § 1.28(d) this submission is treated under § 1.27(g)(2) as a notification of loss of entitlement to small entity status. Therefore, Applicants respectfully request the deficiency payment be processed and the correct entity status be accorded to the application.

05/16/2011 DALLEN 00000006 201430 6366130
01 FC:1599 1770.00 DA

Adjustment date: 06/10/2011 CKHLOK
05/16/2011 DALLEN 00000006 201430 6366130
01 FC:1599 1770.00 CR

06/10/2011 CKHLOK 00003819 201430 6366130
01 FC:1559 1770.00 DA

ITEMIZATION AND CALCULATION OF THE DEFICIENCY OWED

DATE OF PAYMENT	TYPE OF FEE	SMALL ENTITY FEE ACTUALLY PAID	(CURRENT) LARGE ENTITY FEE FOR ACTION	DEFICIENCY PAYMENT OWED
June 22, 2000	Filing	$345	$850	$505
June 22, 2000	Missing Parts Surcharge	$65	$130	$65
November 6, 2001	Issue Fee	$640	$1510	$870
October 3, 2005	4th Maintenance Fee	$450	$980	$530
September 22, 2009	8th Maintenance Fee	$1240	$2480	$1240
				Total $3210

TOTAL DEFICIENCY PAYMENT OWED: $3210

Applicant hereby authorizes the Commissioner to deduct the total deficiency owed of $3210 from Deposit Account No. 20-1430. Please deduct any additional fees due from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

J. Georg Seka
Reg. No. 24,491

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
JGS:jtc
63318995 v1

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

KILPATRICK TOWNSEND & STOCKTON LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

MAILED
JUN 13 2011
OFFICE OF PETITIONS

In re Patent of Podlesny et al. :
Patent No. 6,366,130 :
Issue Date: April 2, 2002 : Letter
Application No. 09/505,656 :
Filing Date: February 17, 2000 :
Attorney Docket No. 020181-000500US :

This is a notice regarding the request for acceptance of a fee deficiency submission under 37 CFR 1.28(c) filed May 5, 2011.[1]

The deficiency payment of $3,210 is hereby accepted.

The change of status to large entity has been entered and made of record.

Telephone inquiries regarding this communication should be directed to Petitions Attorney Steven Brantley at (571) 272-3203.

Charles Steven Brantley
Senior Petitions Attorney
Office of Petitions

[1] The Office notes a duplicate copy of the request was filed on May 9, 2011.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Patent No. 6366130

NOTICE OF *INTER PARTES* REEXAMINATION

Notice is hereby given that a request for *inter partes* reexamination of U.S. Patent No. 6366130 was filed on 1-19-12 under 35 U.S.C. § 311 and 37 C.F.R. § 1.913.

The reexamination proceeding has been assigned Control No. 95/ 000657.

This Notice incorporates by reference into the patent file, all papers entered into the reexamination file.

Note: This Notice should be entered into the patent file.

AO 121 (6/90)

Patent

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET	DATE FILED	UNITED STATES DISTRICT COURT,
11-cv-04356	06/27/2011	NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION

PLAINTIFF	DEFENDANT
Cascades Computer Innovation, LLC	Hynix Semiconductor, Inc, et al

PATENT NO.	DATE OF PATENT	PATENTEE
6,366,130	April 2, 2002	High Speed Low Power Data Transfer Scheme

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK Michael W. Dobbins	(BY) DEPUTY CLERK Haydee Pawlowski	DATE June 29, 2011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

POWER OF ATTORNEY PATENT REEXAMINATION AND CHANGE OF CORRESPONDENCE ADDRESS

The undersigned patent owner hereby appoints: Clifford H. Kraft, attorney registered with the United States Patent and Trademark Office hold registration number 35,229 to represent it in all transactions involving Reexamination number 95/000,657 of United States Patent number 6,366,130 entitled:

"High Speed Low Power Data Transfer Scheme"

All prior powers of attorneys and appointments are hereby revoked.

The Correspondence Address for all correspondence in this case should be sent to:

Clifford H. Kraft
320 Robin Hill Dr.
Naperville IL. 60540

CUSTOMER NUMBER: 74642

Telephone: 708 528-9092

ELBRUS INTERNATIONAL LIMITED

BY:

Signed: _____ Date: 04/06/2012

Name: Leonid N. Nazarov Title: Manager

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 7462

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/505,656	02/17/2000 RULE	326	2819	20181-5US

APPLICANTS

Andrew V. Podlesny, Moscow, RUSSIAN FEDERATION;
Alexander V. Malshin, Moscow, RUSSIAN FEDERATION;
Alexander Y. Solomatnikov, Moscow, RUSSIAN FEDERATION;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/120,531 02/17/1999

**** FOREIGN APPLICATIONS *********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 04/26/2000

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	RUSSIAN FEDERATION	1	3	1
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS
74642

TITLE

High speed low power data transfer scheme

FILING FEE RECEIVED		
410	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

CONFIRMATION NO. 7462

20350
KILPATRICK TOWNSEND & STOCKTON LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

POWER OF ATTORNEY NOTICE

OC000000053654767

Date Mailed: 04/10/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/06/2012.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/rbell/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/505,656	02/17/2000	Andrew V. Podlesny	20181-5US

CONFIRMATION NO. 7462

74642
CLIFFORD H. KRAFT
320 ROBIN HILL DR.
NAPERVILLE, IL 60540

POA ACCEPTANCE LETTER

OC000000053654815

Date Mailed: 04/10/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/06/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/rbell/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET	DATE FILED	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
14 cv 5691	7/24/14	

PLAINTIFF	DEFENDANT
Cascades Computer Innovation, LLC	Samsung Electronics Co., Ltd.

PATENT NO.	DATE OF PATENT	PATENTEE
6,366,130 B1	4/2/2002	Elbrus International Limited

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK Thomas G. Bruton	(BY) DEPUTY CLERK Marlan Cowan	DATE 8/12/14

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET	DATE FILED	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
14 cv 5691	7/24/14	
PLAINTIFF Cascades Computer Innovation, LLC		**DEFENDANT** Samsung Electronics Co., Ltd.

PATENT NO.	DATE OF PATENT	PATENTEE
6,366,130 B1	4/2/2002	Elbrus International Limited

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK Thomas G. Bruton	(BY) DEPUTY CLERK Marlan Cowan	DATE 8/12/14