

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ELBRUS INTERNATIONAL LIMITED,
Patent Owner.

Case IPR2015-01523
Patent 6,366,130

Before JUSTIN T. ARBES, JEFFREY W. ABRAHAM, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition seeking *inter partes* review of claims 1–3, 5–7, and 9 of U.S. Patent No. 6,366,130 B1 (Ex. 1001, “the ’130 patent”), as amended by *Inter Partes* Reexamination Certificate No. US 6,366,130 C1 (“Reexam. Cert.”). Paper 2 (“Pet.”). Elbrus International Limited (“Patent Owner”) filed a Patent Owner Preliminary Response to the Petition. Paper 8 (“Prelim. Resp.”). After considering the Petition and Preliminary Response, we determine that Petitioner has not established a reasonable likelihood of prevailing with respect to any of the challenged claims of the ’130 patent. *See* 35 U.S.C. § 314(a). Accordingly, we deny the Petition and do not institute *inter partes* review.

II. BACKGROUND

A. *Related Proceedings*

The parties identify *Cascades Computer Innovation, LLC. v. Samsung Electronics Co., Ltd.*, Case No. 1-14-cv-05691 (N.D. Ill.), currently pending, as well as pending *inter partes* review petition in Case IPR2015-01524, as also pertaining to the ’130 patent. Pet. 1–2; Paper 4, 3.

B. *The ’130 Patent*

The ’130 patent, titled “High Speed Low Power Data Transfer Scheme,” issued on April 2, 2002, with a reexamination certificate issuing on August 4, 2014. The ’130 patent is directed to a “high speed and low power [complementary metal-oxide semiconductor (CMOS)] data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver.” Ex. 1001, 1:24–

28, Fig. 1. In one embodiment, the latching sense amplifier is arranged as a “cross coupled latched amplifier.” *Id.* at 1:36–38, Fig. 2.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5–7, and 9. Claim 1 is the only independent claim challenged, and is reproduced below:

1. A data transfer arrangement comprising:
 - two bus drivers;
 - a voltage precharge source;
 - a differential bus coupled to the bus drivers and to the voltage precharge source; and
 - a latching sense amplifier coupled to the differential bus;wherein the latching sense amplifier comprises:
 - a first stage including a cross-coupled latch coupled to a differential data bus; and
 - an output stage coupled to an output of said first stage;wherein the output of the first stage is coupled to an input of the output stage;
- wherein the differential bus and the differential data bus are precharge to a voltage V_{pr} between V_{dd} and ground, where $V_{pr}=K*V_{dd}$, and K is a precharging voltage factor.

Id. at 4:2–17.

D. References

Petitioner relies on the following references:

Ternullo, Jr. et al., U.S. Patent No. 6,052,328, filed Dec. 22, 1997, issued Apr. 18, 2000 (“Ternullo,” Ex. 1005).

Sukegawa, U.S. Patent No. 5,828,241, issued Oct. 27, 1998 (“Sukegawa,” Ex. 1006).

Hardee, U.S. Patent No. 6,249,469 B1, filed July 1, 1996, issued June 19, 2001 (“Hardee,” Ex. 1007).

E. The Asserted Grounds

Petitioner asserts the following grounds of unpatentability:

Reference(s)	Statutory Basis	Claim(s) Challenged
Ternullo	§102	1–3, 5, and 6
Ternullo and Hardee	§103	7
Ternullo and Sukegawa	§103	9

III. ANALYSIS

A. Claim Construction

Petitioner offers constructions for two terms, “latching sense amplifier” and “stage.” Pet. 9–11. Petitioner contends that “latching sense amplifier” should be construed to mean “a circuit, including a latch, that detects and amplifies signals.” *Id.* at 9. Petitioner contends that “stage” should be construed to mean “portion of a circuit.” *Id.* at 10.

Patent Owner argues that these terms are commonly used and well-known in the art, and should be given their plain and ordinary meaning. Prelim. Resp. 5–8.

In an *inter partes* review, claim terms in an unexpired patent are

interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1276–79 (Fed. Cir. 2015).

We determine that no express claim construction is required for purposes of this Decision.

B. References

1. Ternullo

Ternullo discloses a “semiconductor memory device having pairs of data lines for reading and writing data signals to and from a matrix of memory cells.” Ex. 1005, 2:38–40. The device in Ternullo contains several pairs of data lines and components between the memory cells and the input/output pad. *Id.* at 3:49–52. Included among these components are data line sense amplifier (32), data line latch sense amplifier (36), and input receiver and output sense amplifier (40). *Id.* at 4:5–20, Fig. 1. Using figures and corresponding explanations in the specification, Ternullo discloses the circuitry in each component used to provide desired read and write operations. *See generally id.* at 4:5–14:26, Figs. 1–12.

2. Sukegawa

Sukegawa discloses a “signal transmission circuit which enables the distance of signal transmission . . . to be increased, while the signal delay and power consumption are reduced.” Ex. 1006, Abstract. Sukegawa teaches that “the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals.” *Id.* at 1:12–15. Sukegawa provides circuit diagrams illustrating, and corresponding descriptions in the specification describing, the specific

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