AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00902	9/22/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Samsung Electronics Co., LTD., Samsung Electronics America, Inc., and Samsung Telecommunications America LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,542,045		
2 7,777,753		
3 8,054,315		
4 8,681,164		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon *initiation of* action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00930	10/1/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above--entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,542,045		
2 7,777,753		
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4 8,681,164		
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DECISION/JUDGEMENT

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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	SOLICITOR JUN 23 2014 U.S. PATENT & TRADEMARK OFFICE

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00691	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	LG Electronics, Inc. and LG Electronics USA, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED

INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,542,045		
2	7,777,753		
3	8,054,315		
4	8,681,164		
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

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Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:		
	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

SOLICITOR
JUN 23 2014
U.S. PATENT & TRADEMARK OFFICE

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00690	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	HTC Corporation and HTC America Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

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DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00689	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Motorola Mobility, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	06/02/2009	7542045	96-S-012C3 (850063.553C3)	6996

30423 7590 05/13/2009

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jefferson Eugene Owen, Freemont, CA;
Raul Zegers Diaz, Palo Alto, CA;
Osvaldo Colavin, Tucker, GA;

Electronic Patent Application Fee Transmittal

Application Number:	11956165
Filing Date:	13-Dec-2007
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	Patrick C.R. Holmes/Angie Rodriguez
Attorney Docket Number:	96-S-012C3 (850063.553C3)

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	1	3	3
		Total in USD ($)		**1813**

Electronic Acknowledgement Receipt

EFS ID:	5159775
Application Number:	11956165
International Application Number:	
Confirmation Number:	6996
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	Patrick C.R. Holmes/Angie Rodriguez
Filer Authorized By:	Patrick C.R. Holmes
Attorney Docket Number:	96-S-012C3 (850063.553C3)
Receipt Date:	15-APR-2009
Filing Date:	13-DEC-2007
Time Stamp:	16:07:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1813
RAM confirmation Number	2112
Deposit Account	191353
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	**Document Description**	**File Name**	**File Size(Bytes)/ Message Digest**	**Multi Part /.zip**	**Pages (if appl.)**
1	Issue Fee Payment (PTO-85B)	96S012C3.pdf	338246 8f35c252e9cd7029cd4cb477e1c93d2b7640aec5	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	34207 718d9da7d8b18a370db675d930fe1a94cef42ba9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	372453		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

30423 7590 04/06/2009

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012C3 (850063.553C3)	6996

TITLE OF INVENTION: ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/06/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, HAU H	2628	345-541000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lisa K. Jorgenson
2 David V. Carlson
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: STMicroelectronics, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Carrollton, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 1

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-1353 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Patrick C.R. Holmes Date 4-15-09

Typed or printed name PCRH Registration No. 46,380

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

30423 7590 04/06/2009

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 04/06/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012C3 (850063-553C3)	6996

TITLE OF INVENTION: ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/06/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

30423 7590 04/06/2009

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MAIL STATION 2346
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CARROLLTON, TX 75006

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012C3 (850063.553C3)	6996

TITLE OF INVENTION: ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/06/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, HAU H	2628	345-541000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012C3 (850063.553C3)	6996

30423 7590 04/06/2009

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 04/06/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/956,165	OWEN ET AL.	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/02/2009*.

2. ☒ The allowed claim(s) is/are *1,2,4,6-18 and 20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/29/2008
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Hau H Nguyen/
Primary Examiner, Art Unit 2628

Terminal Disclaimer

1. The terminal disclaimer filed on 2/20/2009 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,321,368 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 4/29/2008 was *partially* considered by the examiner because some of the references (NPL) do not have a date; therefore, all references are considered except where lined through.

Allowable Subject Matter

2. Claims 1, 2, 4, 6-18 and 20 are allowed.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

The prior art taken singly or in combination does not teach or suggest, an electronic system, among other things, comprising

an arbiter circuit coupled to both the microprocessor system and the video decoder for controlling access to the main memory by the video decoder and the microprocessor.

Conclusion

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6996

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/956,165	12/13/2007	375	2628	96-S-012C3 (850063.553C3)

APPLICANTS

Jefferson Eugene Owen, Freemont, CA;
Raul Zegers Diaz, Palo Alto, CA;
Osvaldo Colavin, Tucker, GA;

**** CONTINUING DATA ***************************

This application is a CON of 10/174,918 06/19/2002 PAT 7,321,368
which is a CON of 09/539,729 03/30/2000 PAT 6,427,194
which is a CON of 08/702,910 08/26/1996 PAT 6,058,459

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /HAU H NGUYEN/ Examiner's Signature	☐ Met after Allowance H.N. Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	6	20	5

ADDRESS

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006
UNITED STATES

TITLE

ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

FILING FEE RECEIVED		
1450	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L18	91	17 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:50
L17	270	15 and 16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:50
L16	3019	(decod$3 decoder) with (arbiter arbitrat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:50
L15	3042	((system host main) near2 memory) with (arbiter arbitrat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:49
L14	38	("4257095" | "4774660" | "4894565" | "5027400" | "5212742" | "5250940" | "5363500" | "5371893" | "5450542" | "5459519" | "5461679" | "5522080" | "5557538" | "5576765" | "5579052" | "5590252" | "5598525" | "5621893" | "5623672" | "5682484" | "5748203" | "5774206" | "5774676" | "5778096" | "5793384" | "5797028" | "5809245" | "5809538" | "5812789" | "5815167" | "5835082" | "5912676" | "5923665" | "5936616" | "5960464" | "6058459" | "6297832" | "6330644").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/03/13 14:09
L13	70	12 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:49

L12	236	10 and 11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:49
L11	1301	(decoder decoding) with arbit $6 with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:48
L10	3850	(cpu microprocessor (central adj process$3 adj unit)) with arbit$6 with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:48
L9	11246	(cpu microprocessor (central adj process$3 adj unit)) with arbit$6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:48
L8	40	7 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:45
L7	334	(video near2 decod$3) with arbit$6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:44
L6	9	("4257095" | "5459519" | "5682484" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/03/13 13:40
L5	116	("5461679").URPN.	USPAT	OR	ON	2009/03/13 13:38
L4	13	("4257095" | "5212742" | "5459519" | "5682484" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789" | "5815167" | "5960464" | "6058459").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/03/13 13:26
L3	2	(("6058459") or ("6427194")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2009/03/13 13:12

L2	6	"US 6427194"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2009/03/13 13:06
L1	2	(("5,461,679") or ("5,797,028")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2009/03/13 12:54

3/13/09 3:23:41 PM
C:\Documents and Settings\HNguyen23\My Documents\EAST\workspaces\11_956165.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	**Art Unit**
	HAU H NGUYEN	2628

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
345	541	G 0 6 F 15 / 167 (2006.0)	
CROSS REFERENCE(S)		G 0 9 G 5 / 39 (2006.0)	
		G 0 9 G 5 / 36 (2006.01.01)	

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
345	542	531	547		

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
2	2	17	18												
	3		19												
3	4	11	20												
	5														
4	6														
5	7														
6	8														
7	9														
8	10														
9	11														
10	12														
12	13														
13	14														
14	15														
15	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/HAU H NGUYEN/ Primary Examiner.Art Unit 2628	03/13/2009	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
/HN/	AA	4,257,095	03/17/81	Nadir	710	119	
	AB	4,774,660	09/27/88	Conforti	364	200	
	AC	4,894,565	01/16/90	Marquardt	307	518	
	AD	5,027,400	06/25/91	Baji et al.	380	20	
	AE	5,212,742	05/18/93	Normile et al.	382	166	
	AF	5,250,940	10/05/93	Valentaten et al.	345	189	
	AG	5,363,500	11/08/94	Takeda	395	425	
	AH	5,371,893	12/06/94	Price et al.	395	725	
	AI	5,450,542	09/12/95	Lehman et al.	395	162	
	AJ	5,459,519	10/17/95	Scalise et al.	348	431.1	
	AK	5,461,679	10/24/95	Normile et al.	283	304	
	AL	5,522,080	05/28/96	Harney	395	727	
	AM	5,557,538	09/17/96	Retter et al.	364	514 A	
	AN	5,576,765	11/19/96	Cheney et al.	348	407	
	AO	5,579,052	11/26/96	Artieri	348	416	
	AP	5,590,252	12/31/96	Silverbrook	395	133	
	AQ	5,598,525	01/28/97	Nally et al.	395	520	
	AR	5,621,893	04/15/97	Joh	395	200.02	
	AS	5,623,672	04/22/97	Popat	395	728	
	AT	5,682,484	10/28/97	Lambrecht	710	128	
	AU	5,748,203	05/05/98	Tang et al.	345	521	
	AV	5,774,206	06/30/98	Wasserman et al.	395	200.77	
	AW	5,774,676	06/30/98	Stearns et al.	709	247	
	AX	5,778,096	07/07/98	Stearns	382	233	

EXAMINER /Hau Nguyen/	DATE CONSIDERED 03/31/2009

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /HN/

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	APPLICATION NO.
	96-S-012C3 (850063.553C3)	11/956,165
	APPLICANTS	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Jefferson Eugene Owen et al.	
	FILING DATE	GROUP ART UNIT
	December 13, 2007	2621

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
/HN/	AA	5,793,384	08/11/98	Okitsu	345	535	
	AB	5,797,028	08/18/98	Gulick et al.	395	800.32	
	AC	5,809,245	09/15/98	Zenda	345	204	
	AD	5,809,538	09/15/98	Pollman et al.	711	151	
	AE	5,812,789	09/22/98	Diaz et al.	709	247	
	AF	5,815,167	09/29/98	Muthal	345	541	
	AG	5,960,464	09/28/99	Lam	711	202	
	AH	5,835,082	11/10/98	Perego	345	202	
	AI	5,912,676	06/15/99	Malladi et al.	345	521	
	AJ	5,923,665	07/13/99	Sun et al.	370	477	
	AK	5,936,616	08/10/99	Torborg, Jr. et al.	345	202	
	AL	6,058,459	05/02/00	Owen et al.	711	151	
	AM	6,297,832	10/02/01	Mizuyabu et al.	345	540	
/HN/	AN	6,330,644	12/11/01	Yamashita et al.	711	147	

FOREIGN PATENT DOCUMENTS

/HN/		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	06-030442	02/04/94	JP (with English abstract)		
	AP	06-178274	06/24/94	JP (with English abstract)		
	AQ	06-348238	12/24/94	JP (with English abstract and machine translation)		
	AR	2,100,700	01/17/95	CA		
	AS	0 673 171	09/20/95	EP		
	AT	08-018953	01/19/96	JP (with English abstract and machine translation)		
/HN/	AU	96/20567	07/04/96	WIPO		

EXAMINER	/Hau Nguyen/	DATE CONSIDERED	03/31/2009

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /HN/

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
/HN/	AA	0 495 574	03/19/97	EP		
	AB	2740583	04/30/97	FR (with English abstract)		
	AC	0827110	03/04/98	EP		
	AD	0827348	03/04/98	EP		
	AE	10-108117	04/24/98	JP (with English abstract)		
	AF	10-145739	05/29/98	JP (with English abstract)		
	AG	0 710 029	03/27/02	EP		
	AH	0772159	01/21/04	EP		
	AI	69631364	11/04/04	DE (with English abstract)		
	AJ	0 639 032	07/18/94	EP (with English abstract)		

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

/HN/	AK		U.S. District Court, Eastern District of Texas Live (Sherman), Civil Docket For Case #: 4:03-cv-00276-LED, STMicroelectronics, Inc., Plaintiff v. Motorola, Inc., and Freescale Semiconductor, Inc., Defendants, Counterclaim Plaintiffs v. STMicroelectronics N.V., and STMicroelectronics, Inc., Counterclaim Defendants, date filed 18 July 2003, 47 pages
/HN/	AL		Bryan Ackland, "The Role of VLSI in Multimedia," *IEEE Journal of Solid-State Circuits*, April 1994, Vol. 29, No. 4, pages 381-388.
/HN/	AM		Joel F. Adam and David L. Tennenhouse, "The Vidboard: A Video Capture and Processing Peripheral for a Distributed Multimedia System," *ACM Multimedia*, August 1-6, 1993, Vol. 5, No. 2, pages 113-120.
/HN/	AN		Matthew Adiletta, et al., "Architecture of a Flexible Real-Time Video Encoder/Decoder: The DECchip 21230," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 136-148.
/HN/	AO		T. Araki, et al., "Video DSP Architecture for MPEG2 CODEC," *ICASSP-94 S_2AUVN, Speech Processing 2, Audio, Underwater Acoustics, VLSI & Neural Networks*, April 19-22, 1994, Vol. 2, pages 417-420.
/HN/	AP		Doug Bailey, et al., "Programmable Vision Processor/Controller for Flexible Implementation of Current and Future Image Compression Standards," *IEEE Micro*, October 1992, pages 33-39.

EXAMINER /Hau Nguyen/	DATE CONSIDERED 03/31/2009

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/HN/	AG		The Motorola MCD212 Video Decoder and System Controller ("MCD212")(as described in the Advance Information manual, published in the U.S. August 1995, at MOT-S 723153-723240)
/HN/	AH		Apple Macintosh Quadra 840AV when executing the "Fusionrecorder 1.0" application as described in the 1993 Developer Note entitled "Macintosh Quadra 840AV and Macintosh Centris 660AV Computers
/HN/	AI		C-Cube CL450 MPEG Video Decoder ("CL450") as described in the "CL450 MPEG Decoder User's Manual," C-Cube Microsystems, Milpitas, CA 1992 (MOT-S 721789-721874)
/HN/	AJ		S. Undy et al., "A low-cost graphics and multimedia workstation chip set," *IEEE Micro*, Vol. 14, No. 2, April 1994, Pages 10-22.
/HN/	AK		Bhed, H. and P. Srinivasan, "A High-Performance Cross-Platform MPEG Decoder," *Digital Video Compression on Personal Computers: Algorithms and Technologies, SPIE Proceedings*, February 7-8, 1994, Vol.2187, pp. 241-248

EXAMINER /Hau Nguyen/	DATE CONSIDERED 03/31/2009

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

1130564_1.DOC Date: April 29, 2008

REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /HN/

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
/HN/	AA		Bursky D., "Highly Integrated Controller Eases MPEG-2 Adoption," *Electronic Design*, Vol. 43, No. 17, pp.141-142, August 21,1995.
/HN/	AB		Butler, B. and T. Mace, "The Great Leap Forward," *PC Magazine*, pp. 241-244, 246, 248, 250, 253-254, 256, 260-261, 264, 266-268, 273-275, 278, October 11, 1994.
/HN/	AC		Doquilo, J. "Symmetric Multiprocessing Servers: Scaling the Performance Wall," *Infoworld*, pp. 82-85, 88-92, March 27, 1995.
/HN/	AD		Galbi, D. et al., "An MPEG-1 Audio/Video Decoder with Run-Length Compressed Antialiased Video Overlays," *IEEE International Solid State Circuits Conference*, pp. 286-287, 381, 1995.
/HN/	AE		Giorgis, T., "SMP Network Operating Systems," *Computer Dealer News*, Vol. 12, No. 16, August 8,1996.
/HN/	AF		King, A., *Inside Windows 95*, Microsoft Press, Redmond Washington, pp.85-90, 1994.
/HN/	AG		Maturi, G., "Single Chip MPEG Audio Decoder, "*IEEE Transactions on Consumer Electronics*, Vol. 38, No. 3, pp. 348-356, August 1992.
/HN/	AH		"MPEG Video Overview," *SGS-Thomson Microelectronics Technical Note*, pp. 1-4, 1992.
/HN/	AI		Video Electronics Standards Association, "VESA Unified Memory Architecture Hardware Specifications Proposal," Version: 1.0p, pp. 1-38, October 31, 1995.
/HN/	AJ		Video Electronics Standards Association, "VESA Unified Memory Architecture VESA BIOS Extensions (VUMA-SBE Proposal), Version 1.0p, pp. 1-26, November 1, 1995.

EXAMINER /Hau Nguyen/	DATE CONSIDERED 03/31/2009

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /HN/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	541, 531, 542, 547, 555, 501, 519, 545	3/13/09	HN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB text search updated and attached	3/13/09	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
345	541, 542, 531, 547	3/13/09	HN

	/HAU H NGUYEN/ Primary Examiner.Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/13/2009								
1	1	=								
2	2	=								
	3	-								
3	4	=								
	5	-								
4	6	=								
5	7	=								
6	8	=								
7	9	=								
8	10	=								
9	11	=								
10	12	=								
12	13	=								
13	14	=								
14	15	=								
15	16	=								
16	17	=								
17	18	=								
	19	-								
11	20	=								

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L19	10	((video near decoder) and arbiter).clm.	US-PGPUB	OR	ON	2009/03/13 15:24
L20	298	((cpu microprocessor) and (arbitrat$3 arbiter)).clm.	US-PGPUB	OR	ON	2009/03/13 15:45
L21	1318	(video near decoder).clm.	US-PGPUB	OR	ON	2009/03/13 15:45
L22	5	20 and 21	US-PGPUB	OR	ON	2009/03/13 15:45
L23	12	(memory with arbiter with decoder).clm.	US-PGPUB	OR	ON	2009/03/13 15:48
L24	49	(memory with (arbitrat $3 arbiter) with (cpu microprocessor (host near2 processor))).clm.	US-PGPUB	OR	ON	2009/03/13 15:51
L25	52	(decoder with (arbitrat $3 arbiter)).clm.	US-PGPUB	OR	ON	2009/03/13 15:51
L26	3	24 and 25	US-PGPUB	OR	ON	2009/03/13 15:51

3/13/09 3:52:33 PM
C:\Documents and Settings\HNguyen23\My Documents\EAST\workspaces\11_956165.wsp

Interference Search 11/956165

H.N.

OK TO ENTER: /HN/

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2620

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	11/956,165
Filed	:	December 13, 2007
For	:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	March 2, 2009

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 CFR 1.116

Commissioner for Patents:

In response to the Office Action dated December 30, 2008, please enter the following response.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/956,165	OWEN ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 10/01/08	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

Felicia D. Roberts

7,321,368 (reconsidered due to the PA filed 3/2/09)

U.S. Patent and Trademark Office

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2620

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	11/956,165
Filed	:	December 13, 2007
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Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	March 2, 2009

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 CFR 1.116

Commissioner for Patents:

In response to the Office Action dated December 30, 2008, please enter the following response.

REMARKS

In the Office Action mailed December 30, 2008, the Examiner noted that a timely filed terminal disclaimer may be used to overcome the non-statutory double patenting rejection. Applicants had previously submitted such a terminal disclaimer, however the Examiner noted that the power of attorney was one of the older types which was in use some years ago and named more than ten practitioners in the power of attorney. Accordingly, applicants were referred to MPEP Sections 402 and 403 to correct the problem. Applicants' attorney has reviewed Sections 402 and 403 and in particular the first part of Section 402 which refers to 37 CFR 1.32(c)(3) and Section 403.01. Sub-part (3) of 37 CFR 1.32(c) indicates that a separate paper should be included which states which of the practitioners named in the power of attorney to be recognized by the Office as being of record in the application to which the power is directed. Further, MPEP 403.01 authorized an attorney appointed by an associate power of attorney to file such a request for associate powers dated before June 25, 2004. Accordingly, such a paper is included herewith.

The attached paper makes clear that only three persons are to be recognized as being of record in the application. Among those which are recognized in the application is David V. Carlson, who signed the terminal disclaimer dated October 1, 2008. Accordingly, it is believed that that terminal disclaimer dated October 1, 2008 can now be validly entered in the present application.

It the Examiner believes that this approach is not correct, she is invited to call applicants' attorney at the number listed below to provide specific instructions as to the preferred course of action. Having reviewed MPEP Sections 402 and 403, it is believed that the present submission should be acceptable to satisfy the Examiner's request, and for this reason issuance of the patent to allowance is respectfully requested.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

DVC:lch

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1306202_1.DOC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	11/956,165
Filed	:	December 13, 2007
For	:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	March 2, 2009

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT OF ATTORNEYS TO BE RECOGNIZED

UNDER 37 CFR 1.32(c)(3)

Commissioner for Patents:

In accordance with 37 CFR 1.32(c)(3) and MPEP 403.01, applicants hereby state that the attorneys to be recognized by the Office as being of record in the application are the following individuals:

David V. Carlson – Reg. No. 31,153

Lisa K. Jorgenson – Reg. No. 34,845

E. Russell Tarleton – Reg. No. 31,800

The above statement is made based on the power of attorney provided to Lisa K. Jorgenson in August of 1996 and her subsequent appointment of an associate power of attorney on April 12, 1999 which includes all of the individuals listed above.

A copy of the power of attorney and appointment of the associate power is provided as set forth in MPEP 402. A copy of the associate power of attorney and the authority to file this request is set forth in MPEP 403.01, which has been followed.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

Enclosure:
Copy of Declaration and Power of Attorney

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1306175_1.DOC

This Declaration copy is intended for the attached continuation application t . submitted on December 13, 2007; attorney docket . .50063.553C3.

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Video and/or Audio Decompression and/or Compression Device that Shares a Memory

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Lisa K. Jorgenson, Reg. No. 34,845 and Irena Lager, Reg. No. 39,260 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

Please send all correspondence to:

Lisa K. Jorgenson
Reg. No. 34,845
SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006
(214) 466-7414

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: Aug 22, 1996
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
98B Escondido Village
Stanford, CA 94305

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: _____
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: Raul Zegers Diaz
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: 8/20/96
Residence and Post Office Address:
~~98B Escondido Village~~
~~Stanford, CA 94305~~ 750 Montrose Avenue #2
Palo Alto, CA 94303

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: _____
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
98B Escondido Village
Stanford, CA 94305

Citizenship: United States of America

Inventor's Signature: Olavio Osvaldo
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: August 19, 1996
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

This POA copy is intended for the attached continuation application being submitted on December 13, 2007; attorney docket no. 850063.553C3.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson E. Owen et al.
Application No.	:	08/702,910
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY
Examiner	:	Glenn Gossage
Art Unit	:	2751
Docket No.	:	96-S-12 (850063.553)
Date	:	April 12, 1999

Assistant Commissioner for Patents
Washington, DC 20231

APPOINTMENT OF ASSOCIATE POWER OF ATTORNEY

Sir:

I, Lisa K. Jorgenson, attorney of record in the above-identified application, appoint as associate attorneys David V. Carlson, Reg. No. 31,153; Michael J. Donohue, Registration No. 35,859, Kevin S. Ross, Reg. No. 42,116; Dale C. Barr, Reg. No. 40,498; Kevin S. Costanza, Reg. No. 37,801, Brian L. Johnson, Reg. No. 40,033, Paul F. Rusyn, Reg. No. 42,118, Dennis M. de Guzman, Reg. No. 41,702; E. Russell Tarleton, Reg. No. 31,800, John M. Wechkin, Reg. No. 42,216; Robert D. McCutcheon, Reg. No. 38,717; and Theodore E. Galanthay, Reg. No. 24,122.

It is requested that correspondence continue to be addressed to Lisa K. Jorgenson at:

Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006-5039

Respectfully submitted,
STMicroelectronics, Inc.

Lisa K. Jorgenson
Lisa K. Jorgenson
Registration No. 34,845

LKJ:BLJ:jab1

1310 Electronics Drive
Carrollton, Texas 75006-5039
(972) 466-7414
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u:\float\jab1\850063.553-Assocpoa

Electronic Acknowledgement Receipt

EFS ID:	4889561
Application Number:	11956165
International Application Number:	
Confirmation Number:	6996
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Laura Hernandez
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C3 (850063.553C3)
Receipt Date:	02-MAR-2009
Filing Date:	13-DEC-2007
Time Stamp:	19:51:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		553C3_RESP_.pdf	74233 616ba8ee9b875f62d70bcd4f20035069d6a7cb81	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Applicant Arguments/Remarks Made in an Amendment	2	3

Warnings:					
Information:					
2	Miscellaneous Incoming Letter	553C3_STMT_OF_ATTYS.pdf	129527 60307de7820b36f60f5c0fc784c976ac66216ce0	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	203760		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/956,165	OWEN ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☐ APPROVED	☒ DISAPPROVED
Date Filed : 10/01/08	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

Felicia D. Roberts

7,321,368

(more than 10 practitioners listed on the POA -see rule 37 CFR 1.32(c)(3))

U.S. Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012C3 (850063.553C3)	6996

30423 7590 12/30/2008

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2628	
MAIL DATE	**DELIVERY MODE**
12/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/956,165	OWEN ET AL.	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/29/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-2, 4, 6-18, and 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7, 13-25 of U.S. Patent No. 7,321,368. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the features of claims 1-2, 4, 6-18, and 20 of the instant application are contained in claims 1-7, 13-25 of U.S. Patent No. 7,321,368. For at least this reason, claims 1-2, 4, 6-18, and 20 would have been obvious by claims 1-7, 13-25 in U.S. Patent No. 7,321,368.

Please see the table below.

Instant Application 11/956165	U.S. Patent No. 7,321,368
1.An electronic system comprising: a bus coupleable to a main memory having stored therein data corresponding to video images to be decoded and also decoded data corresponding to video images that have previously been decoded; a video decoder coupled to the bus for receiving encoded video compressed images and for outputting data for displaying the decoded video images on a display device, the decoder configured to receive receiving data from the main memory corresponding to at least one previously decoded video image and to a current video image to be decoded and outputting decoded video data corresponding to a current video image to be displayed, the current video image to be displayed adapted to be stored in the main memory; a microprocessor system configured to be coupled to the main memory, the microprocessor system for storing non-image data in and retrieving non-image data from the main memory; and an arbiter circuit coupled to both the microprocessor system and the video decoder for controlling the access to said main memory by the video decoder and the microprocessor.	1. An electronic system comprising: a main memory having stored therein data corresponding to images to be decoded and also decoded data corresponding to images that have previously been decoded; a bus coupled to the memory; a decoder coupled to the bus for receiving compressed images and for outputting data for displaying the decoded images on a display device, the decoder receiving data from the main memory corresponding to at least one previously decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being stored in the main memory; a microprocessor system coupled to the main memory, the microprocessor system storing non-image data in and retrieving data from the main memory; and an arbiter circuit coupled to both the microprocessor system and the decoder for controlling the access to said main memory by the decoder and the microprocessor.

Note: although Applicant has filed a terminal disclaimer to the cited patent above, the Power of Attorney is invalid because more than ten practitioners in the Power of Attorney. Applicant is referred to MPEP sections 402 and 403 to correct the problem.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/22/2008								
	1	✓								
	2	✓								
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	20	✓								

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
/HN/	AA	4,257,095	03/17/81	Nadir	710	119	
	AB	4,774,660	09/27/88	Conforti	364	200	
	AC	4,894,565	01/16/90	Marquardt	307	518	
	AD	5,027,400	06/25/91	Baji et al.	380	20	
	AE	5,212,742	05/18/93	Normile et al.	382	166	
	AF	5,250,940	10/05/93	Valentaten et al.	345	189	
	AG	5,363,500	11/08/94	Takeda	395	425	
	AH	5,371,893	12/06/94	Price et al.	395	725	
	AI	5,450,542	09/12/95	Lehman et al.	395	162	
	AJ	5,459,519	10/17/95	Scalise et al.	348	431.1	
	AK	5,461,679	10/24/95	Normile et al.	283	304	
	AL	5,522,080	05/28/96	Harney	395	727	
	AM	5,557,538	09/17/96	Retter et al.	364	514 A	
	AN	5,576,765	11/19/96	Cheney et al.	348	407	
	AO	5,579,052	11/26/96	Artieri	348	416	
	AP	5,590,252	12/31/96	Silverbrook	395	133	
	AQ	5,598,525	01/28/97	Nally et al.	395	520	
	AR	5,621,893	04/15/97	Joh	395	200.02	
	AS	5,623,672	04/22/97	Popat	395	728	
	AT	5,682,484	10/28/97	Lambrecht	710	128	
	AU	5,748,203	05/05/98	Tang et al.	345	521	
	AV	5,774,206	06/30/98	Wasserman et al.	395	200.77	
	AW	5,774,676	06/30/98	Stearns et al.	709	247	
	AX	5,778,096	07/07/98	Stearns	382	233	

EXAMINER /Hau Nguyen/	DATE CONSIDERED 12/22/2008

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/HN/	AA	5,793,384	08/11/98	Okitsu	345	535	
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	AC	5,809,245	09/15/98	Zenda	345	204	
	AD	5,809,538	09/15/98	Pollman et al.	711	151	
	AE	5,812,789	09/22/98	Diaz et al.	709	247	
	AF	5,815,167	09/29/98	Muthal	345	541	
	AG	5,960,464	09/28/99	Lam	711	202	
	AH	5,835,082	11/10/98	Perego	345	202	
	AI	5,912,676	06/15/99	Malladi et al.	345	521	
	AJ	5,923,665	07/13/99	Sun et al.	370	477	
	AK	5,936,616	08/10/99	Torborg, Jr. et al.	345	202	
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	AM	6,297,832	10/02/01	Mizuyabu et al.	345	540	
	AN	6,330,644	12/11/01	Yamashita et al.	711	147	

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/HN/	AO	06-030442	02/04/94	JP (with English abstract)		
/HN/	AP	06-178274	06/24/94	JP (with English abstract)		
/HN/	AQ	06-348238	12/24/94	JP (with English abstract and machine translation)		
/HN/	AR	2,100,700	01/17/95	CA		
/HN/	AS	0 673 171	09/20/95	EP		
/HN/	AT	08-018953	01/19/96	JP (with English abstract and machine translation)		
/HN/	AU	96/20567	07/04/96	WIPO		

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/HN/	AA	0 495 574	03/19/97	EP		
	AB	2740583	04/30/97	FR (with English abstract)		
	AC	0827110	03/04/98	EP		
	AD	0827348	03/04/98	EP		
	AE	10-108117	04/24/98	JP (with English abstract)		
	AF	10-145739	05/29/98	JP (with English abstract)		
	AG	0 710 029	03/27/02	EP		
	AH	0772159	01/21/04	EP		
	AI	69631364	11/04/04	DE (with English abstract)		
	AJ	0 639 032	07/18/94	EP (with English abstract)		

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/HN/	AK		U.S. District Court, Eastern District of Texas Live (Sherman), Civil Docket For Case #: 4:03-cv-00276-LED, STMicroelectronics, Inc., Plaintiff v. Motorola, Inc., and Freescale Semiconductor, Inc., Defendants, Counterclaim Plaintiffs v. STMicroelectronics N.V., and STMicroelectronics, Inc., Counterclaim Defendants, date filed 18 July 2003, 47 pages
/HN/	AL		Bryan Ackland, "The Role of VLSI in Multimedia," *IEEE Journal of Solid-State Circuits*, April 1994, Vol. 29, No. 4, pages 381-388.
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	AB		Mark Baugher, "The OS/2 Resource Reservation System," *Multimedia Computing and Networking 1995*, February 1995, Vol. 2417, pages 167-176.
	AC		Allen J. Baum et al., "A Multimedia Chipset for Consumer Audio-Visual Applications," *IEEE Transactions on Consumer Electronics*, August 1997, Vol. 43, No. 3, pages 646-648.
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	AE		Philip Bonannon et al., "The Architecture of the Dali Main-Memory Storage Manager," *Multimedia Tools and Applications*, 1997, Vol. 4, pages 115-151.
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	AG		V. Michael Bove, Jr., "The Impact of New Multimedia Representations on Hardware and Software Systems," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 34-39.
	AH		Apurva Brahmbatt, "A VLSI Architecture for Real Time Code Book Generator and Encoder of a Vector Quantizer," *International Conference on Image Processing*, IEEE Signal Processing Society, Vol. 2, September 16-19, 1996, pages 991-994.
	AI		Dave Bursky, "Codec Compresses Images in Real Time: Real-Time Motion Video or Still Images Can be Compressed with Single-Chip Multistandard Core," *Electronic Design*, October 3, 1993.
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	AB		Geng-Lin Chen et al., "Video Encoder Architecture for MPEG2 Real Time Encoding," *IEEE Transactions Consumer Electronics*, August 1996, Vol. 42, No. 3, pages 290-299.
	AC		Raymond M.K. Cheng and Donald W. Gillies, "Disk Management for a Hard Real-Time File System," *Multimedia Systems*, Vol. 4, No. 2, 1996, pages 255-260.
	AD		Leonardo Chiariglione, "MPEG: A Technological Basis for Multimedia Applications," *Multimedia*, Spring 1995, Vol. 2, No. 1.
	AE		Winston Sijin Choe et al., "ATM-Based Multi-Party Conferencing System," *IEEE Global Telecommunications Conference*, November 1995, Vol. 1 of 3, pages 592-596.
	AF		Francoise Colaitis, "Opening Up Multimedia Object Exchange with MHEG," *Multimedia*, Summer 1994, Vol. 2, No. 2.
	AG		Geoff Coulson et al., "The Design of a QoS-Controlled ATM-Based Communications System in Chorus," *IEEE Journal on Selected Areas in Communications*, May 1995, Vol. 13, No. 4, pages 686-699.
	AH		Rabin Deka, "A Comprehensive Study of Digital Signal Processing Devices," *Microprocessors and Microsystems*, May 1995, Vol. 19, No. 4, pages 209-221.
	AI		Erwan Demairy et al., "On the Correctness of Multimedia Applications," *The 11th Euromicro Conference on Real-Time Systems*, IEEE Computer Society, June 9-11, 1999, pages 226-233.
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1130564_1.DOC Date: April 29, 2008

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	AB		Subramanian Ganesan, "A Dual-DSP Microprocessor System for Real-Time Digital Correlation," *Microprocessors and Microsystems*, Vol. 15, No. 7, September 1991, pages 379-384.
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	AH		James L. Green, "Capturing Digital Video Using DVI, Multimedia and the i750 video processor," *Dr. Dobb's Journal*, July 1992, Vol. 17, Issue 7.
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	AJ		Fouad Guediri and Pavani Chilamakuri, "An Affordable Solution to Real-Time Video Compression," *Technical Conference, Session 10 Imaging & HDTV*, March 8, 1995, pages 261-265.
	AK		Karl Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," *IEEE Computer Graphics and Applications*, November 1992, pages 53-64.
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	AM		T. Russell Hsing, "The Challenge of VLSI Technology to Low-Bit Rate Video," pages 164-168.

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	AC		Khoa D. Huynh and Taghi M. Khoshgoftaar, "Performance Analysis of Advanced I/O Architectures for PC-based Video Servers," *Multimedia Systems*, Vol. 2, No. 1, 1994, pages 36-50.
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EXAMINER /Hau Nguyen/	DATE CONSIDERED 12/22/2008

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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1130564_1.DOC Date: April 29, 2008

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	APPLICATION NO.
	96-S-012C3 (850063.553C3)	11/956,165
	APPLICANTS	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Jefferson Eugene Owen et al.	
	FILING DATE	GROUP ART UNIT
	December 13, 2007	2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
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	FILING DATE	GROUP ART UNIT
	December 13, 2007	2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
/HN/	AA		Bursky D., "Highly Integrated Controller Eases MPEG-2 Adoption," *Electronic Design*, Vol. 43, No. 17, pp.141-142, August 21,1995.
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1130564_1.DOC Date: April 29, 2008

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	75	("4257095" | "4774660" | "4894565" | "5027400" | "5212742" | "5250940" | "5363500" | "5371893" | "5450542" | "5459519" | "5461679" | "5522080" | "5557538" | "5576765" | "5579052" | "5590252" | "5598525" | "5621893" | "5623672" | "5682484" | "5748203" | "5774206" | "5774676" | "5778096" | "5793384" | "5797028" | "5809245" | "5809538" | "5812789" | "5815167" | "5835082" | "5912676" | "5923665" | "5936616" | "5960464" | "6058459" | "6297832" | "6330644").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/22 04:17
L1	1	("7,321,368").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2008/12/22 04:01
S47	1	("7321368").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2008/04/25 23:26

12/22/08 4:36:05 AM
C:\Documents and Settings\HNguyen23\My Documents\EAST\workspaces\11_956165.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	541, 531, 542, 547, 555, 501, 519, 545	12/22/08	HN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	12/22/08	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/HAU H NGUYEN/ Primary Examiner.Art Unit 2628

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	11/956,165
Filed	:	December 13, 2007
For	:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	October 1, 2008

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Commissioner for Patents:

In response to the Office Action dated May 1, 2008, please extend the period of time for response two (2) months, to expire on October 1, 2008. Enclosed are a Petition for an Extension of Time and the requisite fee. Please amend the application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electronic system comprising:

a bus coupleable ~~couplable~~ to a main memory having stored therein data corresponding to video images to be decoded and also decoded data corresponding to video images that have previously been decoded;

a video decoder coupled to the bus for receiving encoded video ~~compressed~~ images and for outputting data for displaying the decoded video images on a display device, the decoder configured to receive ~~receiving~~ data from the main memory corresponding to at least one previously decoded video image and to a current video image to be decoded and outputting decoded video data corresponding to a current video image to be displayed, the current video image to be displayed adapted to be ~~being~~ stored in the main memory;

a microprocessor system configured to be coupled to the main memory, the microprocessor system for storing non-image data in and retrieving non-image data from the main memory; and

an arbiter circuit coupled to both the microprocessor system and the video decoder for controlling the access to said main memory by the video decoder and the microprocessor.

2. (Currently Amended) An electronic system according to claim 1, wherein the video decoder directly supplies a display adapter with an image under decoding which is not used to decode a subsequent image.

3. (Canceled)

4. (Currently Amended) An electronic system according to claim 1, wherein the video decoder is integrated into a computer motherboard.

5. (Canceled)

6. (Currently Amended) An electronic system comprising:

a fast bus ~~couplable~~coupleable a main memory having stored therein data corresponding to video images to be decoded, decoded data corresponding to video images that have previously been decoded, and non-image data that contains information other than video image information and does not contain any video image information;

a plurality of bus interfaces coupled to the fast bus;

a video decoder configured to be coupled to the main memory via a first bus interface and adapted to receive compressed video images and output a data stream of decoded video images adapted to be displayed on a display device, the video decoder configured to receive ~~receiving~~ data from the main memory corresponding to at least one previously decoded and to a current video image to be decoded and outputting decoded data corresponding to a current video image to be displayed, the current image adapted to be ~~being~~ stored in the main memory;

a central processing circuit configured to be coupled to the main memory via a second bus interface, the central processing circuit storing non-image data in and retrieving non-image data from the main memory; and

an arbiter circuit coupled to the video decoder and to the second bus interface of the central processing circuit for controlling access to the bus via the respective bus interfaces of data to and from the first bus interface of the central processing circuit and the video decoder.

7. (Currently Amended) An electronic circuit for use with a bus coupled to a system memory and a device, comprising:

a video decoder coupled to the bus for receiving ~~compressed~~ encoded video images and for outputting video data for displaying the video decoded images on a display

device, the video decoder configured to receive data from the system memory corresponding to at least one previously decoded image and to a current image to be decoded and configured to output decoded data corresponding to a current image to be displayed, the current image being stored in system memory; and

a memory arbiter coupled to both the device and the video decoder configure to control access to the system memory by the video decoder and the device.

8. (Original) An electronic circuit according to claim 7, wherein the decoder directly supplies a display device with an image under decoding which is not used to decode a subsequent image.

9. (Original) An electronic circuit according to claim 7, wherein the device is a microprocessor system.

10. (Original) An electronic circuit according to claim 7, wherein the decoder and arbiter circuit are integrated into a computer motherboard.

11. (Original) An electronic circuit according to claim 7, wherein the decoder and arbiter are integrated into a single chip.

12. (Currently Amended) An electronic circuit according to claim 7, wherein the ~~compressed~~ encoded images are encoded in the MPEG standard.

13. (Currently Amended) An electronic circuit for use with a memory, comprising:

a bus ~~couplable~~coupleable to the memory;

a decoder coupled to the bus for receiving ~~compressed~~ encoded video images and for outputting data for displaying the decoded video images on a display device, the decoder configured to receive ~~receiving~~ data from the memory corresponding to at least one previously

decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being output for storing ~~stored~~ in the memory;

a central processing unit coupled to the bus for accessing memory; and

an arbiter coupled to the decoder and to the central processing unit for controlling access to the bus.

14. (Original) An electronic circuit according to claim 13, wherein the decoder directly supplies a display device with an image under decoding which is not used to decode a subsequent image.

15. (Original) An electronic circuit according to claim 13, wherein the bus, decoder, central processing unit, and arbiter are integrated into a computer motherboard.

16. (Original) An electronic circuit according to claim 13 wherein the bus, decoder, central processing unit, and arbiter are integrated into a single chip.

17. (Original) An electronic circuit according to claim 13, wherein the compressed images are encoded in the MPEG standard.

18. (Currently Amended) An electronic circuit according to claim 13, wherein the central processing unit is configured for storing~~es~~ non-image data in and retrieves data from the memory.

19. (Canceled)

20. (Original) The circuit according to claim 7 further including an independent signal path, separate from the bus, by which the arbiter is coupled to the device and the video decoder.

REMARKS

This reply is response to a rejection mailed on May 5, 2008.

The sole basis for the rejection was a double patenting rejection under 35 U.S.C. 101 for double patenting to the same invention in view of U.S. Patent 7,321,368 (the '368 patent). This was a statutory type double patenting rejection.

Applicant traverses the double patenting rejection. Applicant believes that the claims as filed a clearly different in scope and content from the present claims. In order to more clearly confirm this difference, applicant has amended some of the claims by amendment submitted herewith.

Applicant cancels herewith claims 3, 5, and 19.

One of the main differences between the claims of the present application and many claims of the '368 patent is that the current claims do not contain a main memory as an element of the claim. Looking at claim 1 of the '368 patent, the first claimed feature is "a main memory having stored therein. . . ." The present claims do not and did not claim this feature.

Turning to claim 1, it contains the feature of "a bus coupleable to a main memory having stored therein data corresponding to video images. . . ." It does not contain the feature of "a main memory having stored therein . . . ." Other language in the claim also makes clear that while the system is configured to work with a memory, the memory is not an actual component of the claim itself. Claim 1 has been amended to clarify this distinction at various places. For example, claim 1 as now written states: "the decoder configured to receive data from the main memory . . . . a microprocessor system configured to be coupled to the main memory, . . ."

There are other differences in the claim, as will be apparent from reading the claims as amended herein.

The claim makes clear that the main memory is not a claim element. Since the claimed components and features are different, and the claims of the issued 7,321,368 patent contains features not found in the claims of the present application and the claims of the present application contain limitations and features not found in the '368 patent, a statutory double patenting rejection is not proper and should be withdrawn.

Applicant accepts that the claims of the present application are similar in many respects to those of the issued '368 patent. A terminal disclaimer is enclosed to address these concerns. Thus, while an obviousness type double patenting rejection may be proper, and to overcome such, a terminal disclaimer is provided, the claims are of different scope and contain different elements, and the statutory double patenting rejection should be withdrawn.

The remaining claims of the present application are different from the issued claims of the '368 patent on similar grounds. For example, claim 6, which is similar in some respects to issued claim 7 of the '368 patent, does not contain a main memory as an element. It also contains different language such as: "a fast bus coupleable a main memory having stored therein data corresponding to video images to be decoded, . . .

a video decoder configured to be coupled to the main memory via a first bus interface . . . ."

Claim 7 contains the language that it is: "for use with a bus coupled to a system memory. . . . the video decoder configured to receive data from the system memory corresponding to at least one previously decoded image and to a current image. . . ."

Other claims contain similar distinctions, making clear that the main memory itself is not a claimed element.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

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David V. Carlson
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1163330_1.DOC

Electronic Patent Application Fee Transmittal

Application Number:	11956165
Filing Date:	13-Dec-2007
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	David V. Carlson/Laura Shockey
Attorney Docket Number:	96-S-012C3 (850063.553C3)

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with $0 paid	1252	1	460	460

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory disclaimer	1814	1	130	130
		Total in USD ($)		**590**

Electronic Acknowledgement Receipt

EFS ID:	4045909
Application Number:	11956165
International Application Number:	
Confirmation Number:	6996
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Laura Shockey
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C3 (850063.553C3)
Receipt Date:	01-OCT-2008
Filing Date:	13-DEC-2007
Time Stamp:	19:43:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$590
RAM confirmation Number	8296
Deposit Account	191090
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Miscellaneous Incoming Letter	553C3_FEE_DEF.pdf	48698 861a3fb52eb9f573c5c4491be1c023f7065034cb	no	1
Warnings:					
Information:					
2	Extension of Time	553C3_EXT_TIME.pdf	87494 82cd2b5d9f974adad5bb041be0a96d26c93ee413	no	1
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	553C3_TERMINAL_DISCLAIMER.pdf	84711 8fb1ae2caf435dc542e7308e4e213980e1f1705f	no	1
Warnings:					
Information:					
4		553C3_AMEND.pdf	86851 4f9fb3f5fb2357661a37aa94df281edc10c60154	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	8

Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	32845 3eccf954d792030d78619d5ae697dce3823e4ca7	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	340599	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	11/956,165
Filed	:	December 13, 2007
For	:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	October 1, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FEE DEFICIENCY AUTHORIZATION FORM

Commissioner for Patents:

Applicants hereby authorize the Director to charge any deficiencies in fees due by way of the enclosed papers only under 37 CFR 1.16 and 1.17 to Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1247079_1.DOC

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) **FY 2008** **(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)**	Docket Number 96-S-012C3 (850063.553C3)
Application Number 11/956,165	Filed December 13, 2007
For ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY	
Art Unit 2628	Examiner Hau H. Nguyen

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$120	$60	$_____
☒	Two months (37 CFR 1.17(a)(2))	$460	$230	$460
☐	Three months (37 CFR 1.17(a)(3))	$1050	$525	$_____
☐	Four months (37 CFR 1.17(a)(4))	$1640	$820	$_____
☐	Five months (37 CFR 1.17(a)(5))	$2230	$1115	$_____

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge the above fees, or credit any overpayment, to Deposit Account Number 19-1090.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the ☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☒ attorney or agent of record. Registration No. 31,153

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. _____ .

/David V. Carlson/	October 1, 2008
Signature	Date
David V. Carlson	206-622-4900
Typed or printed name	Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 1247078_1.DOC

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 96-S-012C3 (850063.553C3)

In re Application of: Jefferson Eugene Owen

Application No.: 11/956,165

Filed: December 13, 2007

For: ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

The owner*, STMicroelectronics, Inc. of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 7,321,368 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Registration No. 31,153

/David V. Carlson/ — Signature

October 1, 2008 — Date

David V. Carlson — Typed or printed name

(206) 622-4900 — Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this statement. See MPEP § 324.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 1247259_1.DOC

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/956,165	12/13/2007	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 10/01/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X $ =		OR	X $50=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X $ =		OR	X $210=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/BONNIE PHOENIX/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012C3	6996

30423 7590 05/01/2008

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2628	
MAIL DATE	**DELIVERY MODE**
05/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/956,165	OWEN ET AL.	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

2. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1-20 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-7, 13-25 of prior U.S. Patent No. 7,321,368. This is a double patenting rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hau H. Nguyen/

Examiner, Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/25/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11956165	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	541, 531, 542, 547, 555, 501, 519, 545	4/25/08	HN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	4/25/08	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	11/956,165
Filed	:	December 13, 2007
For	:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
Art Unit	:	2621
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	April 29, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

Commissioner for Patents:

In accordance with 37 CFR 1.56 and 1.97 through 1.98, applicants wish to make known to the Patent and Trademark Office the references set forth on the attached Information Disclosure Statement. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior U.S. Patent No. 7,321,368, issued January 22, 2008; which is a continuation of U.S. Patent No. 6,427,194, issued July 30, 2002; which is a continuation of U.S. Patent No. 6,058,459, issued May 2, 2000.

The present application contains some text and drawings in common with U.S. Patent Application No. 08/702,911, filed August 26, 1996, and issued September 22, 1998 as U.S. Patent No. 5,812,789, entitled: "VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE" by Raul Z. Diaz and Jefferson E. Owen, which had the same effective filing date and ownership as the present application, and to that extent is related to the present application, which is incorporated herein by reference. All the references, expect one, that are listed on the attached Information

Disclosure Statement were submitted to and/or cited by the Patent and Trademark Office in just this prior application, which issued as U.S. Patent No. 7,321,368 and, therefore, are not required to be provided in this application; a copy of that one new reference is provided, EP 0 639 032 A2 to Didier et al.

If the Examiner wishes, copies of any and all cited art will be provided upon request.

Applicant's attorney is aware of a law suit involving a patent in the same general subject matter, namely, a law suit involving U.S. Patent 5,182,789. This patent is not in the continuation chain of the present application, but was filed on the same date and shares some of the technical disclosure. The undersigned attorney has obtained from the public records a docket sheet printout of the litigation, which is included on the attached Information Disclosure Statement. It is the first item listed on the second page of the 1449 under the section titled "Other Prior Art," which is shown as item AK on page 3 of 13.

If the Examiner wishes to have any documents from these court papers, he is requested to let the attorney signing below know and it will be ordered from the court records to be able to be provided it to the Examiner.

Applicant's attorney believes that providing the court's docket sheet to Examiner and offering to obtain any requested documents fulfills the duty of disclosure under 37 C.F.R. 1.56 and MPEP 2001.6(c). If the Examiner believes more is needed to complete this duty, he is requested to let the attorney know.

As to any reference supplied, applicants do not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserve the right to traverse or antedate any such reference, as by a showing under 37 CFR 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Applicants believe this Information Disclosure Statement has been timely filed, however, the Director is authorized to charge any fee due by way of this Information Disclosure Statement to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

DVC:lcs

Enclosures:
Information Disclosure Statement
Cited Reference (1)

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1130565_1.DOC

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,257,095	03/17/81	Nadir	710	119	
	AB	4,774,660	09/27/88	Conforti	364	200	
	AC	4,894,565	01/16/90	Marquardt	307	518	
	AD	5,027,400	06/25/91	Baji et al.	380	20	
	AE	5,212,742	05/18/93	Normile et al.	382	166	
	AF	5,250,940	10/05/93	Valentaten et al.	345	189	
	AG	5,363,500	11/08/94	Takeda	395	425	
	AH	5,371,893	12/06/94	Price et al.	395	725	
	AI	5,450,542	09/12/95	Lehman et al.	395	162	
	AJ	5,459,519	10/17/95	Scalise et al.	348	431.1	
	AK	5,461,679	10/24/95	Normile et al.	283	304	
	AL	5,522,080	05/28/96	Harney	395	727	
	AM	5,557,538	09/17/96	Retter et al.	364	514 A	
	AN	5,576,765	11/19/96	Cheney et al.	348	407	
	AO	5,579,052	11/26/96	Artieri	348	416	
	AP	5,590,252	12/31/96	Silverbrook	395	133	
	AQ	5,598,525	01/28/97	Nally et al.	395	520	
	AR	5,621,893	04/15/97	Joh	395	200.02	
	AS	5,623,672	04/22/97	Popat	395	728	
	AT	5,682,484	10/28/97	Lambrecht	710	128	
	AU	5,748,203	05/05/98	Tang et al.	345	521	
	AV	5,774,206	06/30/98	Wasserman et al.	395	200.77	
	AW	5,774,676	06/30/98	Stearns et al.	709	247	
	AX	5,778,096	07/07/98	Stearns	382	233	

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,793,384	08/11/98	Okitsu	345	535	
	AB	5,797,028	08/18/98	Gulick et al.	395	800.32	
	AC	5,809,245	09/15/98	Zenda	345	204	
	AD	5,809,538	09/15/98	Pollman et al.	711	151	
	AE	5,812,789	09/22/98	Diaz et al.	709	247	
	AF	5,815,167	09/29/98	Muthal	345	541	
	AG	5,960,464	09/28/99	Lam	711	202	
	AH	5,835,082	11/10/98	Perego	345	202	
	AI	5,912,676	06/15/99	Malladi et al.	345	521	
	AJ	5,923,665	07/13/99	Sun et al.	370	477	
	AK	5,936,616	08/10/99	Torborg, Jr. et al.	345	202	
	AL	6,058,459	05/02/00	Owen et al.	711	151	
	AM	6,297,832	10/02/01	Mizuyabu et al.	345	540	
	AN	6,330,644	12/11/01	Yamashita et al.	711	147	

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	AO	06-030442	02/04/94	JP (with English abstract)		
	AP	06-178274	06/24/94	JP (with English abstract)		
	AQ	06-348238	12/24/94	JP (with English abstract and machine translation)		
	AR	2,100,700	01/17/95	CA		
	AS	0 673 171	09/20/95	EP		
	AT	08-018953	01/19/96	JP (with English abstract and machine translation)		
	AU	96/20567	07/04/96	WIPO		

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	AA	0 495 574	03/19/97	EP		
	AB	2740583	04/30/97	FR (with English abstract)		
	AC	0827110	03/04/98	EP		
	AD	0827348	03/04/98	EP		
	AE	10-108117	04/24/98	JP (with English abstract)		
	AF	10-145739	05/29/98	JP (with English abstract)		
	AG	0 710 029	03/27/02	EP		
	AH	0772159	01/21/04	EP		
	AI	69631364	11/04/04	DE (with English abstract)		
	AJ	0 639 032	07/18/94	EP (with English abstract)		

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	AK		U.S. District Court, Eastern District of Texas Live (Sherman), Civil Docket For Case #: 4:03-cv-00276-LED, STMicroelectronics, Inc., Plaintiff v. Motorola, Inc., and Freescale Semiconductor, Inc., Defendants, Counterclaim Plaintiffs v. STMicroelectronics N.V., and STMicroelectronics, Inc., Counterclaim Defendants, date filed 18 July 2003, 47 pages
	AL		Bryan Ackland, "The Role of VLSI in Multimedia," *IEEE Journal of Solid-State Circuits*, April 1994, Vol. 29, No. 4, pages 381-388.
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	AB		Mark Baugher, "The OS/2 Resource Reservation System," *Multimedia Computing and Networking 1995*, February 1995, Vol. 2417, pages 167-176.
	AC		Allen J. Baum et al., "A Multimedia Chipset for Consumer Audio-Visual Applications," *IEEE Transactions on Consumer Electronics*, August 1997, Vol. 43, No. 3, pages 646-648.
	AD		Vasudev Bhaskaran et al., "Multimedia Architectures: From Desktop Systems to Portable Appliances," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 14-25.
	AE		Philip Bonannon et al., "The Architecture of the Dali Main-Memory Storage Manager," *Multimedia Tools and Applications*, 1997, Vol. 4, pages 115-151.
	AF		C. Bouville et al., "DVFLEX: A Flexible MPEG Real Time Video CODEC," *International Conference on Image Processing*, September 16-19, 1996, Vol. II of III, pages 829-832.
	AG		V. Michael Bove, Jr., "The Impact of New Multimedia Representations on Hardware and Software Systems," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 34-39.
	AH		Apurva Brahmbatt, "A VLSI Architecture for Real Time Code Book Generator and Encoder of a Vector Quantizer," *International Conference on Image Processing*, IEEE Signal Processing Society, Vol. 2, September 16-19, 1996, pages 991-994.
	AI		Dave Bursky, "Codec Compresses Images in Real Time: Real-Time Motion Video or Still Images Can be Compressed with Single-Chip Multistandard Core," *Electronic Design*, October 3, 1993.
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	AD		Leonardo Chiariglione, "MPEG: A Technological Basis for Multimedia Applications," *Multimedia*, Spring 1995, Vol. 2, No. 1.
	AE		Winston Sijin Choe et al., "ATM-Based Multi-Party Conferencing System," *IEEE Global Telecommunications Conference*, November 1995, Vol. 1 of 3, pages 592-596.
	AF		Francoise Colaitis, "Opening Up Multimedia Object Exchange with MHEG," *Multimedia*, Summer 1994, Vol. 2, No. 2.
	AG		Geoff Coulson et al., "The Design of a QoS-Controlled ATM-Based Communications System in Chorus," *IEEE Journal on Selected Areas in Communications*, May 1995, Vol. 13, No. 4, pages 686-699.
	AH		Rabin Deka, "A Comprehensive Study of Digital Signal Processing Devices," *Microprocessors and Microsystems*, May 1995, Vol. 19, No. 4, pages 209-221.
	AI		Erwan Demairy et al., "On the Correctness of Multimedia Applications," *The 11th Euromicro Conference on Real-Time Systems*, IEEE Computer Society, June 9-11, 1999, pages 226-233.
	AJ		C.H. Van Dusen et al., "From Concept to an Implementation," *International Broadcasting Convention*, September 12-16, 1996.
	AK		Santanu Dutta et al., "VLSI Issues in Memory-System Design for Video Signal Processors," *IEEE* 1995, pages 498-503.
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	AA		Borko Furht, "Processor Architectures for Multimedia: A Survey," *Multimedia Modeling*, November 17-20, 1997, pages 89-109.
	AB		Subramanian Ganesan, "A Dual-DSP Microprocessor System for Real-Time Digital Correlation," *Microprocessors and Microsystems*, Vol. 15, No. 7, September 1991, pages 379-384.
	AC		Wanda Gass, "Architecture Trends of MPEG Decoders for Set-Top Box," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 162-169.
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	AF		Robert J. Gove et al., "Image Computing Requirements for the 1990s: From Multimedia to Medicine," *The International Society for Optical Engineering, Medical Imaging V: Image Capture, Formatting and Display,* February 1991, Vol. 1444, pages 318-333.
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	AH		James L. Green, "Capturing Digital Video Using DVI, Multimedia and the i750 video processor," *Dr. Dobb's Journal*, July 1992, Vol. 17, Issue 7.
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	AL		Y. Hoffner and M.F. Smith, "Communication between two microprocessors through common memory," *Microprocessors and Microsystems*, July/August 1982, Vol. 6, No. 6, pages 303-308.
	AM		T. Russell Hsing, "The Challenge of VLSI Technology to Low-Bit Rate Video," pages 164-168.

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	AJ		D. Kim et al., "A Real-Time MPEG Encoder Using a Programmable Processor," *IEEE*, 1994, pages 161-170.
	AK		Toshiro Kinugasa et al., "A Video Pre/Post-processing LSI for Video Capture," *1996 Digest of Technical Papers*, June 5-7, 1996, pages 396-397.
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	AD		Woobin Lee et al., "MediaStation 5000: Integrating Video and Audio," *Multimedia*, Summer 1994, Vol. 1, No. 2, pages 50-61.
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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C3 (850063.553C3)	APPLICATION NO. 11/956,165
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE December 13, 2007	GROUP ART UNIT 2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
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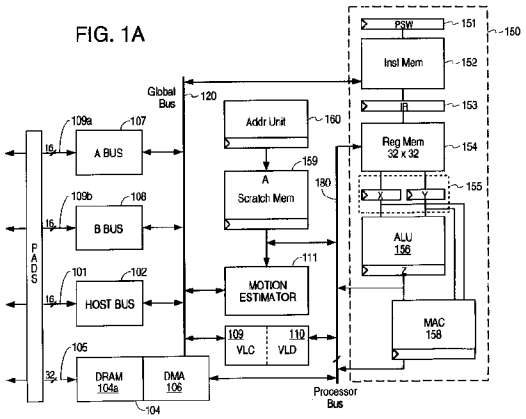
(54) **Structure and method for a multistandard video encoder/decoder.**

(57) A structure and a format for providing a video signal encoder under the MPEG standard are provided. In one embodiment, the video signal interface is provided with a decimator for providing input filtering for the incoming signals. In one embodiment, the central processing unit (CPU) and multiple coprocessors implements DCT and IDCT and other signal processing functions, generating variable length codes, and provides motion estimation and memory management. The instruction set of the central processing unit provides numerous features in support for such features as alpha filtering, eliminating redundancies in video signals derived from motion pictures and scene analysis. In one embodiment, a matcher evaluates 16 absolute differences to evaluate a "patch" of eight motion vectors at a time.

FIG. 1A



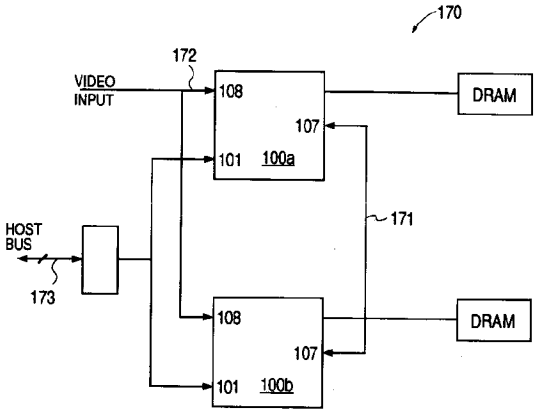


FIG. 1B

EP 0 639 032 A2

Rank Xerox (UK) Business Services
(3.10/3.09/3.3.4)

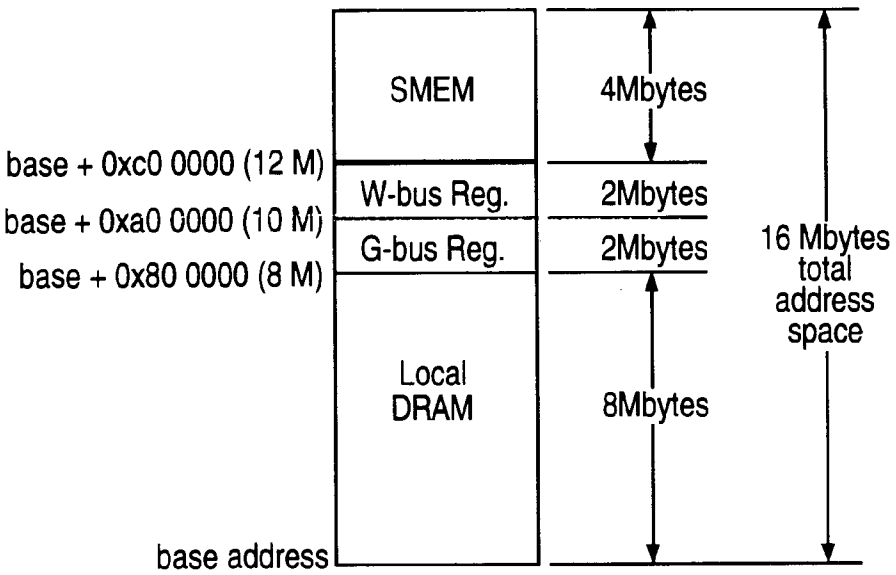

SMEM
4Mbytes
base + 0xc0 0000 (12 M)
W-bus Reg.
2Mbytes
base + 0xa0 0000 (10 M)
G-bus Reg.
2Mbytes
base + 0x80 0000 (8 M)
16 Mbytes total address space
Local DRAM
8Mbytes
base address

FIG. 1C

Background of the Invention

1. Field of the Invention

The present invention relates to integrated circuit designs; and, in particular, the present invention relates to integrated circuit designs for image processing.

2. Discussion of the Related Art

The Motion Picture Experts Group (MPEG) is an international committee charged with providing a standard (hereinbelow "MPEG standard") for achieving compatibility between image compression and decompression equipment. This standard specifies both the coded digital representation of video signal for the storage media, and the method for decoding. The representation supports normal speed playback, as well as other playback modes of color motion pictures, and reproduction of still pictures. The MPEG standard covers the common 525- and 625-line television, personal computer and workstation display formats. The MPEG standard is intended for equipment supporting continuous transfer rate of up to 1.5 Mbits per second, such as compact disks, digital audio tapes, or magnetic hard disks. The MPEG standard is intended to support picture frames of approximately 288 X 352 pixels each at a rate between 24Hz and 30Hz. A publication by MPEG entitled "Coding for Moving Pictures and Associated Audio for digital storage medium at 1.5Mbit/s," included herein as Appendix A, provides in draft form the proposed MPEG standard, which is hereby incorporated by reference in its entirety to provide detailed information about the MPEG standard.

Under the MPEG standard, the picture is divided into a matrix of "Macroblock slices" (MBS), each MBS containing a number of picture areas (called "macroblocks") each covering an area of 16 X 16 pixels. Each of these picture areas is further represented by one or more 8 X 8 matrices which elements are the spatial luminance and chrominance values. In one representation (4:2:2) of the macroblock, a luminance value (Y type) is provided for every pixel in the 16 X 16-pixel picture area (i.e. in four 8 X 8 "Y" matrices), and chrominance values of the U and V (i.e., blue and red chrominance) types, each covering the same 16 X 16 picture area, are respectively provided in two 8 X 8 "U" and two 8 X 8 "V" matrices. That is, each 8 X 8 U or V matrix has a lower resolution than its luminance counterpart and covers an area of 8 X 16 pixels. In another representation (4:2:0), a luminance value is provided for every pixel in the 16 X 16 pixels picture area, and one 8 X 8 matrix for each of the U and V types is provided to represent the chrominance values of the 16 X 16-pixel picture area. A group of four contiguous pixels in a 2 X 2 configuration is called a "quad pixel"; hence, the macroblock can also be thought of as comprising 64 quad pixels in an 8 X 8 configuration.

The MPEG standard adopts a model of compression and decompression based on lossy compression of both interframe and intraframe information. To compress interframe information, each frame is encoded in one of the following formats: "intra", "predicted", or "interpolated". Intra encoded frames are least frequently provided, the predicted frames are provided more frequently than the intra frames, and all the remaining frames are interpolated frames. In a prediction frame ("P-picture"), only the incremental changes in pixel values from the last I- picture or P-picture are coded. In an interpolation frame ("B- picture"), the pixel values are encoded with respect to both an earlier frame and a later frame. By encoding frames incrementally, using predicted and interpolated frames, the redundancy between frames can be eliminated, resulting in a high efficiency in data storage. Under the MPEG, the motion of an object moving from one screen position to another screen position can be represented by motion vectors. A motion vector provides a shorthand for encoding a spatial translation of a group of pixels, typically a macroblock.

The next steps in compression under the MPEG standard provide lossy compression of intraframe information. In the first step, a 2-dimensional discrete cosine transform (DCT) is performed on each of the 8 X 8 pixel matrices to map the spatial luminance or chrominance values into the frequency domain.

Next, a process called "quantization" weights each element of the 8 X 8 transformed matrix, consisting of 1 "DC" value and sixty-three "AC" values, according to whether the pixel matrix is of the chrominance or the luminance type, and the frequency represented by each element of the transformed matrix. In an I-picture, the quantization weights are intended to reduce to zero many high frequency components to which the human eye is not sensitive. In P- and B- pictures, which contain mostly higher frequency components, the weights are not related to visual perception. Having created many zero elements in the 8 X 8 transformed matrix, each matrix can be represented without further information loss as an ordered list consisting of the "DC" value, and alternating pairs of a non-zero "AC" value and a length of zero elements following the non-zero value. The values on the list are ordered such that the elements of the matrix are

presented as if the matrix is read in a zig_zag manner (i.e., the elements of a matrix A are read in the order A00, A01, A10, A02, A11, A20 etc.). This representation is space efficient because zero elements are not represented individually.

Finally, an entropy encoding scheme is used to further compress, using variable-length codes, the representations of the DC coefficient and the AC value-run length pairs. Under the entropy encoding scheme, the more frequently occurring symbols are represented by shorter codes. Further efficiency in storage is thereby achieved.

The steps involved in compression under the MPEG standard are computationally intensive. For such a compression scheme to be practical and widely accepted, however, a high speed processor at an economical cost is desired. Such processor is preferably provided in an integrated circuit.

Other standards for image processing exist. These standards include JPEG ("Joint Photographic Expert Group") and CCITT H.261 (also known as "P x 64"). These standards are available from the respective committees, which are international bodies well-known to those skilled in the art.

Summary of the Invention

In accordance with the present invention, a structure and a method for encoding digitized video signals are provided. In one embodiment, the video signals are stored in an external memory system, and the present embodiment provides (a) two video ports each configurable to become either an input port or an output port for video signals; (b) a host bus interface circuit for interfacing with an external host computer; (c) a scratch-pad memory for storing a portion of the video image; (d) a processor for arithmetic and logic operations, which computes discrete cosine transforms and quantization on the video signals to obtain coefficients for compression under a lossy compression algorithm; (e) a motion estimation unit for matching objects in motion between frames of images of the video signals, and outputting motion vectors representing the motion of objects between frames; and (f) a variable-length coding unit for applying an entropy coding scheme on the quantized coefficients and motion vectors.

In one embodiment, a global bus is provided to be accessed by video ports, the host bus interface, the scratch-pad memory, the processor, the motion estimation unit, and the variable-length coding unit. The global bus provides data transfer among the functional units. In addition, in that embodiment, a processor bus having a higher bandwidth than the global bus is provided to allow higher band-width data transfer among the processor, the scratch-pad memory, and the variable-length coding units. A memory controller controls data transfers to and from the external memory while at the same time provides arbitration the uses of the global bus and the processor bus.

Multiple copies of the structure of the present invention can be provided to form a multiprocessor of video signals. Under such configuration, one of the video ports in each structure would be used to receive the incoming video signal, and the other video port would be used for communication between the structure and one or more of its neighboring structures.

In accordance with another aspect of the present invention, one of the two video port in one embodiment comprises a decimation filter for reducing the resolution of incoming video signals. In one embodiment, one of the video ports include an interpolator for restoring the reduced resolution video into a higher resolution upon video signal output.

In accordance with another aspect of the present invention, a memory with a novel address mechanism is provided to sort video signals arriving at the structure of the present invention in pixel interleaved order into several regions of the memory, such that the data in the several regions of this memory can be read in block interleaved order, which is used in subsequent signal processing steps used under various video processing standards, including MPEG.

In accordance with another aspect of the present invention, a synchronizer circuit synchronizes the system clock of one embodiment with an external video clock to which the incoming video signals are synchronized. The synchronization circuit provides for accurate detection of an edge transition in the external clock within a time period which is comparable with a flip-flop's metastable period, without requiring an extension of the system clock period.

In one embodiment of the present invention, a "corner turn" memory is provided. In this corner-turn memory, a selected region is mapped to two set of addresses. Using an address in the first set of addresses, a row of memory cells are accessed. Using an address in the second set of addresses, a column of memory cells are accessed. The corner-turn memory is particularly useful for DCT and IDCT operations where each macroblock of pixels are accessed in two passes, one pass in column order, and the other pass in row order.

In accordance with another aspect of the present invention, a scratch pad memory having a width four times the data path of the processor is provided. In addition, two set of buffer registers, each set including registers of the width of the data path, are provided as buffers between the processor and the scratch pad memory. The buffer registers operates at the clock rate of the processor, while the scratch pad memory can operate at a lower clock rate. In this manner, the bandwidths of the processor and the scratch pad memory are matched without the use of expensive memory circuitry. Each set of buffer registers are either loaded from, or stored into, the scratch pad as a one register having the width of the scratch pad memory, but accessed by the processor individually as registers having the width of the data path. In one set of the buffer registers, each register is provided with two addresses. Using one address, the four data words (each having the width of the data path) are stored into the register in the order presented. Using the other address, prior to storing into the buffer register, a transpose is performed on the four halfwords of the higher order two data words. A similar transpose is performed on the four halfwords of the lower order two data words. The latter mode, together with the corner turn memory allows pixels of a macroblock to be read from, or stored into, the scratch pad memory either in row order or in column order.

In accordance with another aspect of the present invention, the pixels of a macroblock are stored in one of two arrangements in the external dynamic random access memory. Under one arrangement, called the "scan-line" mode, four horizontally adjacent pixels are accessed at a time. Under the other arrangement, which is suitable for fetching reference pixels in motion estimation, pixels are fetched in tiles (4 by 4 pixels) in column order. A novel address generation scheme is provided to access either the memory for scan-line elements or for quad pels. Since most filtering involves quad pels (2 X 2 pixels), the quad pel mode arrangement is efficient in access time and storage, and avoids rearrangement and complex address decoding.

In accordance with another aspect of the present invention, the operand input terminals of the arithmetic and logic unit in the process is provided a set of "byte multiplexors" for rearranging the four 9-bit bytes in each operand in any order. Because each 9-bit byte can be used to store the value of a pixel, so that the arithmetic and logic unit can operate on the pixels in a quad pel stored in a 36-bit operand simultaneously, the byte multiplexor allows rearranging the relative positions of the pixels within the 36-bit operands, numerous filtering operations can be achieved by simply setting the correct pixel configuration. In one embodiment, in accordance with the present invention, filters for performing pixel offsets, decimations, in either horizontal or vertical directions, or both are provided using the byte multiplexor. In addition, the present invention provides higher compression ratios, using novel functions for (a) activities analysis, used in applying adaptive control of quantization, and (b) scene analysis, used in reduction of interframe redundancy.

In accordance with another aspect of the present invention, a fast detector of a zero result in an adder is provided. The fast zero detector includes a number of "zero generator" circuits and a number of zero propagator circuits. The fast detector signals the presence of a zero result within, as a function of the length of the adder's operands, logarithm time, rather than linear time.

In accordance with another aspect of the present invention, the present invention provides a structure and a method for a non-linear "alpha" filter. Under this non-linear filter, thresholds T_1 and T_2 are set by the two parameters m and n. If the absolute difference between the two input values of the non-linear filter are less than T_1 or greater than T_2, a fixed relative weight are accorded the input values, otherwise a relative weight proportional to the absolute difference is accorded the input values. This non-linear filter finds numerous application in signal processing. In one embodiment, the non-linear filter is used in deinterlacing and temporal noise reduction applications.

In accordance with another aspect of the present invention, a structure for performing motion estimation is provided, including: (a) a memory for storing said macroblocks of a current frame and macroblocks of a reference frame; (b) a filter receiving a first group of pixels from the memory for resampling; and (c) a matcher receiving the resampled first group of pixels and a second group of pixels from a current macroblock, for evaluation of a number of motion vectors. The matcher provides a score representing the difference between the second group of pixels and the first group of pixels for each of the motion vectors evaluated. In this embodiment, the best score over a macroblock is selected as the motion vector for the macroblock. In one embodiment, the matcher evaluates 8 motion vectors at a time using a 2 X 8 "slice" of current pixels and a 4 X 12 pixel reference area.

In accordance with another aspect of the present invention, a structure is provided for encoding by motion vectors a current frame of video data, using a reference frame of video data. The structure includes a memory circuit for storing (a) adjacent current macroblocks from a row j of current macroblocks, designated $C_{j,p}$, $C_{j,p+1}$, ..., $C_{j,p+n-1}$ in the order along one direction of the row of macroblocks; and (b) adjacent reference macroblocks from a first column i of reference macroblocks, designated $R_{q,i}$,$R_{q+1,i}$, ...,

$R_{q+m-1,i}$ and a second column $C_{j+1,p}$ $C_{p+1,p+1,...}$, $C_{j+1,p+n+1}$. The adjacent reference macroblocks are reference macroblocks within the range of the motion vectors, with each of said current macroblocks being substantially equidistance from the $R_{q,i}$ and $Rq+_{m-1,i}$ reference macroblocks. The structure of the present invention evaluates each of the adjacent current macroblocks against each of the adjacent reference macroblocks under the motion vectors, so as to select a motion vector representing the best match between each of said current macroblock and a corresponding one of said reference macroblocks. When evaluation of the current macroblock against the set of reference frame macroblock in the memory circuit is completed, the current macroblock $C_{j,p}$ is remove from the memory circuit and replaced by a current macroblock $C_{j,p+n}$,said current macroblock $C_{j,p+n}$ being the current macroblock adjacent said macroblock $C_{j,p+n-1}$. At the same time, the column of adjacent reference macroblocks $R_{q,i}$, $R_{q+1,i}$, ..., $R_{q+m-1,i}$ are removed from the memory circuit and replaced by the next column of adjacent reference macroblocks $R_{q,i+1}$,$R_{q+1,i+1}$, ..., $R_{q+m-1,i+1}$. In this manner, each current macroblock, while in memory, is evaluated against the largest number of reference macroblocks which can be held in the memory circuit, thereby minimizing the number of time current and reference macroblocks have to be loaded into memory. Of course, for purely convenience reasons, the terms "rows" and "columns" are used to describe the relationship between current and reference macroblocks. It is understood that a column of current macroblocks can be evaluated against a row of reference macroblock, within the scope of the present invention.

In accordance with the present invention, the control structure for controlling evaluation of motion vectors is provided by a counter which includes first and second fields representing respectively the current macroblock and the reference macroblock being evaluated. Under the controlling scheme of one embodiment, each of the first and second fields are individually counted, such that when the first field reaches a maximum, a carry is generated to increment the count in the second field. The number of counts in the first and second fields are respectively , the number of current and reference macroblocks. In this manner, each current macroblock is evaluated completely with the reference macroblocks in the memory circuit.

In accordance with another aspect of the present invention, an adaptive thresholding circuit is provided in the zero-packing circuit prior to entropy encoding of the DCT coefficients into variable length code. In this adaptive threshold circuit, a current DCT coefficient is set to zero, if the immediately preceding and the immediately following DCT coefficients are both zero, and the current DCT coefficient is less than a programmable threshold. This thresholding circuit allows even higher compression ratio by extending a zero runlength.

The present invention is better understood upon consideration of the detailed description below and the accompanying drawings.

Brief Description of the Drawings

Figure 1a is a block diagram of an embodiment of the present invention provided in an MPEG encoder chip 100.

Figure 1b shows a multi-chip configuration in which two copies of chip 100, chips 100a and 100b, are used.

Figure 1c is a map of chip 100's address space.

Figure 2 is a block diagram of video port 107 of chip 100 shown in Figure 1.

Figure 3a shows a synchronization circuit 300 for synchronizing video data arrival at port 107 with an external video source, which provides video at 13.5 Mhz under 16-bit mode, and 27 Mhz under 8-bit mode.

Figure 3b shows the times at which the samples of video clock signal Vclk indicated in Figure 3a are obtained.

Figure 4a is a timing diagram of video port 107 for latching video data provided at 13.5Mhz on video bus 190a under 16-bit mode.

Figure 4b is a timing diagram of video port 107 for latching video data provided at 27 Mhz on video bus 190a under 8-bit mode.

Figure 5a shows the sequence in which 4:2:2 video data arrives at port 107.

Figure 5b is a block diagram of decimator 204 of video port 107.

Figure 5c is a tables showing, at each phase of the CIF decimation, the data output R_{out} of register 201, the operand inputs A_{in} and B_{in} of 14-bit adder 504, the carry-in input C_{in}, and the data output Dec of decimator 204.

Figure 5d is a tables showing, at each phase of the CCR 601 decimation, the data output R_{out} of register 201, the operand inputs A_{in} and B_{in} of 14-bit adder 504, the carry-in input C_{in}, and the data output Dec of decimator 204.

Figure 6a is a block diagram of interpolator 206.

Figure 6b is an address map of video FIFO 205, showing the partition of video FIFO 205 into Y region 651, U region 652 and V region 653, and the storage locations of data in a data stream 654 received from decimator 204.

Figure 6c illustrates the generation of addresses for accessing video FIFO 205 from the contents of address counter 207, during YUV separation, or during video output.

Figure 6d illustrates the sequence in which stored and interpolated luminance and chrominance pixels are output under interpolation mode.

Figure 6e shows two block interleaved groups 630 and 631 in video FIFO 205.

Figure 7a is an overview of data flow between memory blocks relating to CPU 150.

Figure 7b illustrates in further detail the data flow between P memory 702, QMEM 701, registers R0-R23, and scratch memory 159.

Figure 7c shows the mappings of registers P4-P7 into the four physical registers corresponding to registers P0-P3.

Figure 7d shows the mappings between direct and alias addresses of the higher 64 36-bit locations in SMEM 159.

Figure 8a is a block diagram of memory controller 104, in accordance with the present invention.

Figure 8b show a bit assignment diagram for the channel memory entries of channel 1.

Figure 8c show a bit assignment diagram for the channel memory entries of channels 0, and 3-7.

Figure 8d shows a bit assignment diagram for the channel memory entry of channel 2.

Figure 9a shows chip 100 interfaced with an external 4-bank memory system 103 in a configuration 900.

Figure 9b is a timing diagram for an interleaved access under "reference" mode of the memory system of configuration 900.

Figure 9c is a timing diagram for an interleaved access under "scan-line" mode of the memory system of configuration 900.

Figures 10a and 10b shows pixel arrangements 1000a and 1000b, which are respectively provided to support scan-line mode operation and reference frame fetching during motion estimation.

Figure 10c shows the logical addresses for scan-line mode access.

Figure 10d shows the logical addresses for reference frame fetching.

Figure 10e shows a reference frame fetch in which the reference frame crosses a memory page boundary.

Figures 11a and 11b are timing diagrams showing respectively data transfers between external memory 103 and SMEM 159 via QG register 810.

Figure 12 illustrates the pipeline stages of CPU 150.

Figure 13a shows a 32-bit zero-lookahead circuit 1300, comprising 32 generator circuits 1301 and propagator circuits.

Figure 13b shows the logic circuits for generator circuit 1301 and propagator circuit 1302.

Figures 14a and 14b show schematically the byte multiplexors 1451 and 1452 of ALU 156.

Figure 15a is a block diagram of arithmetic unit 750.

Figure 15b is a schematic diagram of MAC 158.

Figure 15c(i) illustrates an example of "alpha filtering" in the mixing filter for combining chroma during a deinterlacing operation.

Figure 15c(ii) is a block diagram of a circuit 1550 for computing the value of alpha.

Figure 15c(iii) shows the values of alpha obtainable from the various values of parameters m and n.

Figures 15d(i)-15d(iv) illustrates instructions using the byte multiplexors of arithmetic unit 750, using one mode selected from each of the HOFF, VOFF, HSHRINK and VSHRINK instructions, respectively.

Figure 15e shows the pixels involved in computing activities of quad pels A and B as input to a STAT1 or STAT2 instruction.

Figure 15f shows a macroblock of luminance data for which a measure of activity is computed using repeated calls to a STAT1 or a STAT2 instruction.

Figures 16a and 16b are respectively a block diagram and a data and control flow diagram of motion estimator 111.

Figure 16c is a block diagram of window memory 705, showing odd and even banks 705a and 705b.

Figure 16d shows how, in the present invention, vertical half-tiles of a macroblock are stored in odd and even memory banks of window memory 750.

Figure 17 illustrates a 2-stage motion estimation algorithm which can be executed by motion estimator 111.

Figures 18a and 18b show, with respect to reference macroblocks, a decimated current macroblock and the range of a motion vector having an origin at the upper right corner of the current macroblock for the first stage of a B frame motion estimation and a P frame motion estimation respectively.

Figure 18c shows, with respect to reference macroblocks, a full resolution current macroblock and the range of a motion vector having an origin at the upper right corner of the current macroblock for the second stage of motion estimation in both P-frame and B-frame motion estimations.

Figure 18d shows the respectively locations of current and reference macroblocks in the first stage of a B frame motion estimation.

Figure 18e shows the respective locations of current and reference macroblocks in the first stage of a P frame motion estimation.

Figure 18f shows both a 4 X 4 tile current macroblock 1840 and a 5 X 5 tile reference region 1841 in the second stage of motion estimation.

Figure 18g shows the fields of a state counter 1890 having programmable fields for control of motion estimation.

Figure 18h shows the four possibilities by which a patch of motion vectors crosses a reference frame boundary.

Figure 18i shows the twelve possible ways the reference frame boundary can intersect the reference and current macroblocks in window memory 705 under the first stage motion estimation for B-frames.

Figure 18j shows, for each of the 12 cases shown in Figure 18h, the INIT and WRAP values for each of the fields in state counter 1890.

Figure 18k shows the twenty possible ways the reference frame boundary can intersect the current and reference macroblocks in window memory 705.

Figure 18l shows, for each of the twenty cases shown in Figure 18k, the corresponding INIT and WRAP values for each of the fields of state counter 1890.

Figures 18m-1 and 18m-2 show the clipping of motion estimation with respect to the reference frame boundary for either the second stage of a 2-stage motion estimation, or the third stage of a 3-stage motion estimation.

Figure 18n provides the INIT and WRAP values for state counter 1890 corresponding to the reference frame boundary clipping shown in Figures 18m-1 and 18m-2.

Figure 19a illustrates the algorithm used in matcher 1606 for evaluate eight motion vectors over eight cycles.

Figure 19b shows the locations of the "patch" of eight motion vector evaluated for each slice of current pixels.

Figure 19c shows the structure of matcher 1608.

Figure 19d shows the pipeline in the motion estimator 111 formed by the registers in subpel filter 1606.

Figures 20a and 20b together form a block diagram of VLC 109.

Detailed Description of the Preferred Embodiments

1. Overview

Figure 1a is a block diagram of an embodiment of the present invention provided in an encoder/decoder integrated circuit 100 ("chip 100"). In this embodiment, chip 100 encodes or decodes bit stream compatible with MPEG, JPEG and CCITT H.64. As shown in Figure 1a, chip 100 communicates through host bus interface 102 with a host computer (not shown) over 32-bit host bus 101. Host bus interface 102 implements the IEEE 1196 NuBus standard. In addition, chip 100 communicates with an external memory 103 (not shown) over 32-bit memory bus 105. Chip 100's access to external memory 103 is controlled by a memory controller 104, which includes dynamic random access memory (DRAM) controller 104a and direct memory access (DMA) controller 106. Chip 100 has two independent 16-bit bidirectional video ports 107 and 108 receiving and sending data on video busses 190a and 190b respectively. Video ports 107 and 108 are substantially identical, except that port 107 is provided with a decimation filter, and port 108 is provided with an interpolator. Both the decimator and the interpolator circuits of ports 107 and 108 are described in further detail below.

The functional units of chip 100 communicate over an internal global bus 120, these units include the central processing unit (CPU) 150, the variable-length code coder (VLC) 109, variable-length code decoder (VLD) 110, and motion estimator 111. Central processing unit 150 includes the processor status word register 151, which stores the state of CPU 150, instruction memory ("I mem") 152, instruction register 153, register file ("RMEM") 154, which includes 31 general purpose registers R1-R31, byte multiplexor 155,

arithmetic logic unit ("ALU") 156, memory controller 104, multiplier-accumulator (MAC) 158, and scratch memory ("SMEM") 159, which includes address generation unit 160. Memory controller 104 provides access to external memory 103, including direct memory access (DMA) modes.

Global bus 120 is accessed by SMEM 159, motion estimator 111, VLC 109 and VLD 110, memory controller 104, instruction memory 152, host interface 102 and bidirectional video ports 107 and 108. A processor bus 180 is used for data transfer between SMEM 159, VLC 109 and VLD 110, and CPU 150.

During video operations, the host computer initializes chip 100 by loading the configuration registers in the functional units of chip 100, and maintains the bit streams sending to or receiving from video ports 107 and 108.

Chip 100 has an memory address space of 16 megabytes. A map of chip 100's address space is provided in Figure 1c. As shown in Figure 1c, chip 100 is assigned a base address. The memory space between the base address and the location (base address + 7FFFFF[1]) is reserved for an external dynamic random access memory (DRAM). The memory space between location (base address + 800000) to location (base address + 9FFFFF) is reserved for registers addressable over global bus 120. The memory space between location (base address + A00000) and location (base address + BFFFFF) is reserved for registers addressable over a processor bus or write-back bus ("W bus") 180a. A scratch or cache memory, i.e. memory 159, is allocated the memory space between location (base address + C00000) and location (base address + FFFFFF).

A multi-chip system can be built using multiple copies of chip 100. Figure 1b shows a two-chip configuration 170, in which two copies of chip 100, chips 100a and 100b are provided. Up to 16 copies of chip 100 can be provided in a multi-chip system. In such a system, video port 108 of each chip is connected to a reference video bus, such as bus 171, which is provided for passing both video data and non-video data between chips. Each chip receives video input at port 107. In Figure 1b, the video input port 107 of each chip receives input data from external video bus 172. Each chip is provided a separate 16-megabyte address space which is not overlapping with other chips in the multi-chip configuration.

2. Video Ports 107 and 108

Video ports 107 and 108 can each be configured for input or output functions. When configured as an input port, video port 107 has a decimator for reducing the resolution of incoming video data. When configured as an output port, video port 108 has an interpolator to output data at a higher resolution than chip 100's internal representation. Figure 2 is a block diagram of video port 107. Video port 107 can operate in either a 16-bit mode or an 8-bit mode. When the video port is configured as an input port, video data is read from video bus 109a into 16 X 8 register file 201, which is used as a first-in-first-out (FIFO) memory under the control of read counter 202 and write counter 203. Under 8-bit input mode, read counter 202 receives an external signal V_active, which indicates the arrival of video data. Decimation filter or decimator 204, which receives video data from register file 201, can be programmed to allow the data received to pass through without modification, to perform CCR 601 filtering, or CIF decimation. In video port 108, where decimator 204 is absent, only YC_bC_r separation is performed.

The results from decimator 204 are provided to a 32 X 4-byte video FIFO (VFIFO) 205. The contents of video FIFO 205 are transferred by DMA, under the control of memory controller 104, to external memory 103. Because various downstream processing functions, e.g. DCT, IDCT operations or motion estimation, operate on chrominance and luminance data separately, chrominance and luminance data are separately stored in external memory 103 and moved into and out of video FIFO 205 blocks of the same chrominance or luminance type. Typically, the blocks of chrominance and luminance data covering the same screen area are retrieved from external memory 103 in an interleaved manner ("block interleaved" order). By contrast, input and output of video data on video busses 109a and 109b are provided sample by sample, interleaving chrominance and luminance types ("pixel interleaved" order). To facilitate the sorting of data from pixel interleaved order to block interleaved order ("YUV separation"), during data input, and in the other direction during data output, a special address generation mechanism is provided. This address generation mechanism, which is discussed in further detail below, stores the pixel interleaved data arriving at video port 107 or 108 into video FIFO 205 in block interleaved order. During output, the address generation mechanism reads block interleaved order data from video FIFO 205 in pixel interleaved order for output.

Address counters 207 and 208 are provided to generate the addresses necessary for reading and writing data streaming into or out of video FIFO 205. Address counter 207 is a 9-bit byte counter, and address counter 208 is a 7-bit word counter. In this embodiment, two extra bits are provided in each of

[1] Addresses in this descriptions are provided in hexadecimal, unless otherwise stated.

counters 207 and 208, to allow video FIFO 205 to overflow without losing synchronization with the external video data stream, in the event that a DMA transfer to and from external memory 103 cannot take place in time.

When the video port is configured for video output, video data is retrieved from external memory 103 and provided to interpolator 206, which can be programmed to allow the data to pass through without modification or to provide a (1,1) interpolation. The output data of interpolator 206 is provided as output of chip 100 on video bus 109a.

a. The Synchronizer

Chip 100 operates under an internal clock ("system clock") of chip 100 at a rate of 60 Mhz. However, incoming video data are synchronized with an external clock ("video clock"). Under 8-bit mode, video data arrive at video port 107 at 27 Mhz. Under 16-bit mode, video data arrive at video port 107 at 13.5 Mhz. The system and video clocks are asynchronous with respect to each other. Consequently, for the video data to be properly received, a synchronization circuit 300, which is shown in Figure 3a, is provided to synchronize the video data arriving at video port 107.

Figure 4a shows a timing diagram of video port 107 under 16-bit input mode. As shown in Figure 4a, 16-bit video data arrives at port 107 synchronous with an external video clock signal Vclk 404a, i.e. the video clock, at 13.5 Mhz. Internally, the synchronization circuit generates a write signal 401, which is derived from detecting the transitions of video clock 404a, to latch the 16-bit video data into register file 201 as two 8-bit data. Figure 4a shows the data stream 403a representing the 8-bit data stream. In Figure 4a, 16-bit video data are ready at video port 107 at times t_0 and t_2, and 8-bit video data are latched at times t_0, t_1, t_2, and t_3.

Figure 4b shows a timing diagram of video port 107 operating under 8-bit input mode. Under the 8-bit input mode, the write signal 401, which is derived from detecting the transitions of video clcok 404b, latches at into register file 201 each 8-bit data word of video data stream 403a at times t_0, t_1, t_2, and t_3.

Since the external video clock is asynchronous to the internal system clock, valid data can be latched only within a window of time after a rising edge of the video clock. Thus, valid data are latched only when the rising edges of the video clock are properly detected. In the prior art, such rising edges are detected by sampling the video clock using a flip-flop. However, if the rising edge of the video clock occurs at a time so close to the sampling point that it violates the set-up or the hold time of the flip-flop, the flip-flop can enter a metastable state for an indefinite period of time. During this period of metastability, another sampling by the flip-flop on the input video clock signal cannot take place without risking the loss of data. In chip 100, where the usual time for the output data of a flip-flop to settle is approximately 3 nanoseconds, this metastable period can exceed 12 nanoseconds.

Under the 8-bit input mode, a rising edge in the external video clock occurs every 37 nanoseconds. To detect this rising edge, the sampling frequency is required to be at least twice the frequency of the video clock Vclk, which translates to a period of no more than 18.4 nanoseconds. As mentioned above, if a rising edge occurs too closely in time to a sampling point, the sampling flip-flop enters into a metastable state. Because a metastable flip-flop may require in excess of 12 nanoseconds to resolve, i.e. more than half of the available time between arrivals of the clock edges of the video clock, the detections of rising edges in the video clock signal occur in an unpredictable manner. In certain circumstances, some rising edges would be missed. (In the 16-bit mode, however, because the input data arrives approximately every 74 nanoseconds, there is ample time for the metastable flip-flop to resolve before the arrival of the next rising edge of the video clock).

To ensure that a rising edge of the external video clock is always caught, the external video clock is sampled at both the rising edges and the falling edges of the system clock. By contrast, the video data at video port 107 or 108 are only sampled at the rising edges of the system clock. A synchronization circuit 300, shown in Figure 3a, is provided to detect the edges on the video clock.

As shown in Figure 3a, the video clock (Vclk) is provided to the data inputs of two 2-bit shift registers 301 and 302. Shift register 301 comprises D flip-flops 301a and 301b, and shift register 302 comprises D flip-flop 302a and 302b. shift registers 301 and 302 are clocked by the rising and the falling edges of system clock SClk, respectively. In addition, the output data of shift register 301 is provided to a data input terminal of D flip-flop 305, which is also clocked by the falling edge of system clock Sclk. Preferably, D flip-flop 301a is skewed to have a rapid response to a rising edge at its data input terminal. Likewise, D flip-flop 302a is skewed to have a rapid response to a falling edge at its data input terminal. Such response skewing can be achieved by many techniques known in the art, such as the use of ratio logic and the use of a high gain in the master stage of a master-slave flip-flop.

NAND gates 310-313 are provided in an AND-OR configuration. NAND gates 310 and 311 each detect a rising edge transition, and NAND gate 312 detects a falling edge transition. An edge transition detected in any of NAND gates 310-312 results in a logic '1' in NAND gate 313. NAND gate 312 is used in the 16-bit mode to detect a falling edge of the video clock. This falling edge is used in the 16-bit mode to confirm latching of the second 8-bit data of the 16-bit data word on video port 107.

The operation of synchronization circuit 300 can be described with the aid of the timing diagram shown in Figure 3b and the time annotations indicated on the signal lines of Figure 3a. Figure 3b shows the states of system clock signal (Sclk) at times t_1 to t_4. The time annotation on each signal line in Figure 3a indicates, at time t_4, the sample of the video clock held by the signal line. For example, since the sample of the video clock at time t_1 propagates to the output terminal of D flip-flop 301b after two rising edges of the system clock, the output terminal of D flip-flop 301b at time t_4 is annotated "t_1" to indicate the value of D flip-flop 301b's output data. Similarly, at time t_4, which is immediately after a falling edge of the system clock, the output datum of D flip-flop 305 is also labelled "t_1", since it holds the sample of the video clock at time t_1.

At time t_4, therefore, NAND gate 310 compares an inverted sample of the video clock at time t_1 with a sample of the video clock at time t_2. If a rising edge transition occurs between times t_1 and t_2, a zero is generated at the output terminal of NAND gate 310. NAND gate 310, therefore, detects a rising edge arriving after the sampling edge of the system clock. At the same time, NAND gate 311 compares an inverted sample of the video clock at time t_2 with a sample of the video clock at time t_3. Specifically, if a rising edge occurs between times t_2 and t_3, a zero is generated at the output terminal of NAND gate 311. Thus, NAND gate 311 detects a rising edge of the video clock arriving before the sampling edge of the system clock.

The output datum of NAND gate 313 is latched into register 314 at time t_5. The value in register 314 indicates whether a rising edge of Vclk is detected between times t_1 and t_3. This value is reliable because, even if D flip-flop 301a enters into a metastable state as a result of a rising edge of video clock signal Vclk arriving close to time t_3, the metastable state would have been resolved by time t_5.

In video port 107, NAND gate 312 is provided to detect a falling edge of the video clock under the 16-bit mode of operation.

b. The Decimator

Video port 107 processes video signals of resolutions between CCR 601 (i.e. 4:2:2, 720 X 480) and QCIF (176 X 144). In one application, CCR 601 video signals are decimated by decimator 204 to CIF (352 X 288) resolution. Figure 5a shows the sequence in which CCR 601 Y (luminance), C_b and C_r (chrominance) data arrive at port 107.

Decimation is performed by passing the input video through digital filters. In CCR 601 filtering, the chrominance data are not filtered, but the digital filter for luminance data provides as filtered pixels, each denoted Y*, according to the equation:

$$Y^*_0 = \frac{2(Y_{-1}+Y_1)+6Y_0}{8}$$

where Y_0 is the luminance data at the center tap, and Y_{-1} and Y_1 are luminance data of the pixels on either side of pixel Y_0.

In this digital filter, after providing as output the filtered luminance pixel Y^*_0, the center tap moves to input luminance sample Y_1.

For CIF decimation, the digital filter for luminance samples has the equation,

$$Y^*_0 = \frac{16Y_0+9(Y_{-1}+Y_1)-(Y_3+Y_{-3})}{32}$$

where Y_{-3}, Y_{-2}, Y_{-1}, Y_0, Y_1, Y_2, Y_3 are consecutive input luminance data (Y_{-2} and Y_2 are multiplied with a zero coefficient in this embodiment).

Unlike the CCR 601 filtering, the center tap moves to Y_2, so that the total number of filtered output samples is half the total number of input luminance samples to achieve a 50% decimation. Under CIF decimation, C_r and C_b type chrominance data are also filtered and decimated. The decimation equations are:

$$Cr^*_0 = \frac{Cr_0 + Cr_{-1}}{2} \; ; \; Cb^*_0 = \frac{Cb_0 + Cb_{-1}}{2}$$

where Cr_0 and Cr_{-1}, and Cb_0 and Cb_{-1} are consecutive samples of the C_r and C_b types. The C_b and C_r filters then operate on the samples Cr_1 and Cr_2, Cb_1, and Cb_2 respectively. Consequently, under CIF decimation, the number of filtered output samples in each of the C_b and C_r chrominance types is half the number of the corresponding chrominance type input pixels.

Figure 5b is a block diagram of decimator 204. As shown in Figure 5b, Decimator 204 comprises phase decoder 501, multiplexors 502 and 503, a 14-bit adder 504, latch 505 and limiter 506. Phase decoder 501 is a state machine for keeping track of input data into decimator 204, so as to properly sequence the input samples for digital filtering. Figure 5c is a table showing, at each phase of CIF decimation, the data output R_{out} of register 201, the operand inputs A_{in} and B_{in}, and the carry-in input C_{in} of adder 504, and the data output Dec of decimator 204 after limiting at limiter 506. Similarly, Figure 5d is a table showing, at each phase of the CCIR 601 decimation, the data output R_{out} of register 201, the operand inputs A_{in} and B_{in}, and the carry-in input C_{in} of adder 504, and the data output Dec of decimator 204 after limiting at limiter 506.

During a decimation operation, a data sample is retrieved from register file 201. The bits of this data sample are shifted left an appropriate number of bit positions, or inverted, to scale the data sample by a factor of 4, 8, 16 or -1, before being provided as input data to multiplexor 502. When scaling by 16 is required, 15 is added to the input datum to multiplexor 502 to compensate precision loss due to an integer division performed in limiter 506. Multiplexor 502 also receives as an input datum the latched 14-bit result of adder 504 right-shifted by three bits. Under the control of phase decoder 501, multiplexor 502 selects one of its input data as an input datum to adder 504, at adder 504's A_{in} inputterminal. Multiplexor 503 selects the data sample (left-shifted by four bits) from register 201, a constant zero, or the latched result of 14-bit adder 504. The output datum of multiplexor 503 is provided as data input to 14-bit adder 504, at the B_{in} input terminal.

The output datum of 14-bit adder 504 is latched at the system clock rate (60 Mhz) into register 505. Limiter 506 right-shifts the output datum of register 505 by 5 bits, so as to limit the output datum to a value between 0 and 255. The output datum of limiter 506 is provided as the data output of decimator 204.

As mentioned above, video port 108 can alternatively be configured as an output port. When configured as an output port, port 108 provides, at the user's option, a (1, 1) interpolation between every two consecutive samples of same type chrominance or luminance data.

Figure 6a shows interpolator 206 of chip 100. As shown in Figure 6a, during video output mode, an address generator 601, which includes address counters 207 and 208, is provided to read from video FIFO 205 samples of video data. Consecutive samples of video data of the same type are latched into 8-bit registers 602 and 603. Data contained in register 602 and 603 are provided as input operands to adder 604. Each result of adder 604 is divided by 2, i.e. right-shifted by one bit, and latched into register 605. In this embodiment, registers 602 and 603 are clocked at 60 Mhz, and register 605 is clocked at 30 Mhz.

When video bus 109a is configured as an input bus, video FIFO 205 receives from decimator 204 the decimated video data, which is then transferred to external memory 103. Alternatively, when video bus 109a is configured as an output bus, video data are received from external memory 103 and provided in a proper sequence to interpolator 206 for output to video bus 109a. The operation of the video FIFO in video port 107 is similar to that of video FIFO 205.

When YUV separation is performed during input mode, or when interpolation is performed during output mode, video FIFO 205 is divided into four groups of locations ("block interleaved groups"). Each block interleaved group comprises a 16-byte "Y-region", an 8-byte "U-region", and an 8-byte "V-region". Data transfers between video FIFO 205 and external memory 103 occur as DMA accesses under memory controller 104's control. Address counters 207 and 208 generate the addresses required to access video FIFO 205.

Figure 6b is an address map 650 of a block interleaved group in video FIFO 205, showing the block interleaved group partitioned into Y-region 651, U-region 652 and V-region 653. A data stream 654 arriving from decimator 204 is shown at the top of address map 650. Shown in each of the regions are the locations

of data from data stream 654.

Address map 650 also represents the data storage location for performing interpolation, when video port 107 is configured as an output port. As shown in Figure 6b, the Y-region 651 is offset from the U-region 652 by sixteen bytes, and the U-region 652 is further offset from the V-region 653 by eight bytes. In addition, adjacent groups of block interleaved locations are offset by 32 bytes.

Address counter 207 generates the addresses of video FIFO 205 for YUV separation during input mode, and the addresses for interpolation during output mode. Figure 6c illustrates address generation by address counter 207 for accessing video FIFO 205. As shown in Figure 6c, address counter 207 comprises a 11-bit counter 620 counting at 60 Mhz. Embedded fields in counter 620 include a 9-bit value C[8:0], and bits "p" and "ex". The positions of these bits in counter 620 are shown in Figure 6c. The "p" bit, which is the least significant bit of counter 620, represents the two phases of an interpolation operation. These two phases of an interpolation operation correspond to operand loadings into registers 602 and 603 (Figure 6a) during the (1, 1) interpolation.

During interpolation, every other luminance sample, every other red type chrominace sample (C_r), and every other blue chrominance sample (C_b) are interpolated. Figure 6d shows, under interpolation mode, the sequence in which stored and interpolated luminance and chrominace samples are output.

Bit C[0] of binary counter 620 counts at 30 Mhz. Since video data samples are received or output at video ports 107 and 108 in pixel interleaved order at 30 MHz, bit C[0] of binary counter 620 indicates whether a luminance sample or a chrominance sample is received or output. Since bit C[1] counts at half the rate of bit C[0], for chrominance samples, bit C[1] indicates whether a C_b or a C_r type chrominance sample is output.

Bits C[8:0] are used to construct the byte address B[8:0] (register 625) for accessing video FIFO 205. Bits B[6:5] indicate which of the four block interleaved groups in video FIFO 205 is addressed. Thus, bits B-[8:5] form a "group address". Incrementer 621 receives bits C[8:2] and, during interpolation, increments the number represented by these bits. Bits C[8:2] is incremented whenever the following expression evaluates to a logical true value:

$$(ex \wedge p) \wedge (\overline{C[0]} \vee C[1])$$

where $\wedge$ is the logical operator "and" and $\vee$ is the logical operator "or". Bit "ex" of binary counter 620 indicates an interpolation output. Thus, according to this expression, incrementer 621 increments C[8:2] at one of the two phases of the interpolation operation, every other luminance output, or every other blue or red chrominance output. In this embodiment, when the output sample is not an interpolated output sample, incrementer 621 is disabled. Consequently, both registers 602 and 603 (Figure 6a) obtain their values from the same byte address. In effect, the same sample is fetched twice, so that each non-interpolated sample is really obtained by performing a 1-1 interpolating using two identical values.

The data output of incrementer 621 is referenced as D[6:0]. As shown in Figure 6c, the group address B[6:5] is provided by bits D[4:3]. Since a toggle of bit B[4] indicates a jump of 16 byte addresses, bit B[4] can be used to switch, within a block interleaved group, between the luminance and the chrominance regions. Accordingly, bit B[4] adopts the value of negated bit C[0]. In addition, since a toggle of bit B[3] indicates a jump of eight byte addresses, bit B[3] can be used to switch, when a chrominance sample is fetched, between the U and V regions of a block interleaved group. Thus, as shown in Figure 6c, bit B[3] has the value of bit C[1].

The unregistered value 624 contains a value E[4:0] formed by the ordered combination of bit C[1], bits D[2:0] and the bit which value is provided by the expression

$$((C[1] \wedge p) \veebar ex),$$

where $\veebar$ is the "exclusive-or" operator. Bits E[4:1] provides the byte address bits B[3:0] during output of a chrominance sample, and bits E[3:0] provides byte address bits B[3:0] during output of a luminance sample. Bit E[0] ensures the correct byte address is output when an "odd" interpolated luminance sample is output. (U + V refer to chrominance pixel types C_b + C_r respectively.)

Figure 6e shows two adjacent block interleaved groups 630 and 631. Group 630 comprises Y-region 630a, U-region 630b and V-region 630c and group 631 comprises Y-region 631a, U-region 631b and V-region 631c. In Figure 6e, the labels 1-31 in group 630 represent the positions, in pixel interleaved order, of the pixels stored at the indicated locations of video FIFO 205. Likewise, the labels 32-63 in group 631 represent the positions, in pixel interleaved order, of the pixels stored at the indicated locations. The control

structure of Figure 6c ensures that the proper group addresses are generated when the output sequence crosses over from output samples obtained or interpolated from pixels in group 630 to samples obtained or interpolated from pixels in group 631.

3. The Memory structure

Internally, chip 100 has six major blocks of memory circuits relating to CPU 150. These memory circuits, which are shown in Figure 7a, include instruction memory 152, register file 154, Q memory 701 ("QMEM"), SMEM 159, address memory ("AMEM") 706, and P memory 702 ("PMEM"). In addition, a FIFO memory ("VLC FIFO") 703 (not shown) is provided for use by VLC 109 and VLD 110 during the coding and decoding of variable-length codes. A "zig-zag" memory 704 ("Z mem", not shown) is provided for accessing DCT coefficients in either zigzag or binary order. Finally, a window memory 705 ("WMEM", not shown) is provided in motion estimator 111 for storing the current and reference blocks used in motion estimation.

In Figure 7a, an arithmetic unit 750 represents both ALU 156 and MAC 158 (Figure 1). Instructions for arithmetic unit 750 are fetched from instruction memory 152. Instruction memory 152 is implemented in chip 100 as two banks of 512 X 32 bit single port SRAMs. Each bank of instruction memory 152 is accessed during alternate cycles of the 60 Mhz system clock. Instruction memory 152 is loaded from global bus 120.

The two 36-bit input operands and the 36-bit result of arithmetic unit 750 are read and written into the 32 general purpose registers R0-R31 of register file 154. The input operands are provided to arithmetic unit 750 over 36-bit input busses 751a and 751b. The result of arithmetic unit 750 are provided by 36-bit output bus 752. (In this embodiment, register R0 is a pseudo-register used to provide the constant zero).

QMEM 701, which is organized as eight 36-bit registers Q0-Q7, shares the same addresses as registers R24-R31. To distinguish between an access to one of registers R24-R31 and an access to one of the registers in QMEM 701, reference is made to a 2-bit configuration field "PQEn" (P-Q memories enable) in CPU 150's configuration register. In this embodiment, registers R0-R23 are implemented by 3-port SRAMs. Each of registers R0-R23 is clocked at the system clock rate of 60 MHz, and provides two read-ports, for data output onto busses 751a and 751b, and one write port, for receiving data from bus 752. Registers R24-R31 are accessed for read and write operations only when the "PQEN" field is set to '00'. The access time for each of registers R0-R23 is 8 nanoseconds. The write ports of registers R0-R31 are latched in the second half period of the 60 Mhz clock, to allow data propagation in the limiting and clamping circuits of arithmetic unit 750.

SMEM 159, which is organized as a 256 X 144-bit memory, serves as a high speed cache between external memory 103 and the register file 154. SMEM 159 is implemented by single-port SRAM with an access time under two periods of the 60 Mhz system clock (i.e. 33 nanoseconds).

To provide higher performance, special register files QMEM 701 and PMEM 702 are provided as high speed paths between arithmetic unit 750 and SMEM 159. Output data of SMEM 159 are transferred to QMEM 701 over the 144-bit wide processor bus 180b). Input data to be written into SMEM 159 are written into PMEM 702 individually as four 36-bit words. When all four 36-bit words of PMEM 702 contain data to be written into SMEM 159, a single write into SMEM 159 of a 144-bit word is performed. SMEM 159 can also be directly written from a 36-bit data bus in "W bus" 180a, bypassing PMEM 702. W bus 180a comprises a 36-bit data bus and a 6-bit address bus. Busses 180a and 180b form the processor bus 180 shown in Figure 1.

In this embodiment, QMEM 701 is implemented by 3-port 8 X 36 SRAMs, allowing (i) write access on bus 108b as two quad-word (i.e. 144-bit) registers, and (ii) read access on either bus 751a or 751b as eight 36-bit registers. The access time for QMEM 701 is 16 nanoseconds. PMEM 702 allows write access from both W bus 180a and QGMEM 810 (see below). QGMEM 810 is an interface between global bus 120 and processor bus 180a. PMEM 702 is read by SMEM 159 on an 144-bit bus 708 (not shown).

Figure 7b illustrates in further detail the interrelationships between QMEM 701, PMEM 702, SMEM 159 and registers R0-R31. As shown in Figure 7b, PMEM 702 receives either 32-bit data on global bus 120, or 36-bit data on W bus 180a. Write decoder 731 maps the write requests on W-bus 180a or global bus 120a into one of the eight 36-bit registers P0-P7. Physically, PMEM 702 is implemented by only four actual 36-bit registers. Each of the registers P0-P3 is mapped into one of the four actual registers. The halfwords of each of registers P4-P7 map into two of the four actual registers. Figure 7c shows the correspondence between registers P4-P7 and registers P0-P3, which are each mapped into the four actual registers. As shown in Figure 7c, the higher and lower order halfwords (i.e. bits [31:16] and bits [15:0], respectively) of register P4 are mapped respectively into the lower order halfwords (i.e. bits [15:0]) of register P1 and P0.

The higher and lower order halfwords (i.e. bits [31:16] and bits [15:0], respectively) of register P5 are mapped respectively into the higher order halfwords of registers P1 and P0. The higher and lower order halfwords of register P6 are mapped respectively into the lower order halfwords of registers P3 and P2. The higher and lower order halfwords of register P7 are mapped respectively into the higher order halfwords of registers P3 and P2. In this manner, an instruction storing a quad pel (4 by 16-bits) into registers P4 and P5, or registers P6 and P7 would also have transposed the quad pel prior to storing the quad pel into SMEM 159. In conjunction with the "quarter turn" memory (described below), registers P4-P7 provides a means for writing a macroblock of pixels in column or row order and reading the macroblock back in the corresponding row or column order.

PMEM 702 is read only by the StoreP instruction, and stores over bus 708 the four actual registers as a 144-bit word into SMEM 159. The 144-bit word stored into SMEM 159 is formed by concatenating the contents of the four actual registers, in the order of corresponding registers P0-P3.

Thirty-two 36-bit locations in SMEM 159 are each provided two addresses. These addresses occupy the greatest 64 (36-bit word) addresses of SMEM 159's address space. The first set of addresses ("direct addresses"), at hexadecimal 3c0-3df), are mapped in the same manner as the remaining lower 36-bit locations of SMEM 159. The second set of addresses ("alias addresses"), at hexadecimal 3e0-3ff, are aliased to the direct addresses. The mappings between the direct and the alias addresses are shown in Figure 7d. The aliases are assigned in such a way that, if a macroblock is written in row order into these addresses, using the second set of addresses and using registers P4-P7 of PMEM 702, and read back in sequential order using the first (direct) address, the macroblock is read back in column and row transposed order. Since the present embodiment performs 2-dimensional DCT or an IDCT operation on a macroblock in two passes, one pass being performed in row order and the other pass being performed in column order, these transpose operations provide a highly efficient mechanism of low overhead to perform the 2-dimensional DCT or IDCT operation.

As shown in Figure 7b, SMEM 159 can also be written directly from W bus 180a, thereby bypassing PMEM 702. Multiplexers 737a-737d selects as input data to SMEM 159 between the data on bus 708 and W bus 180a. Drivers 738 are provided for writing data into SMEM 159. Decoder 733 decodes read and write requests for access to SMEM 159.

An address memory ("AMEM") 706, which is implemented as an 8 X 10 bit SRAM, stores up to eight memory pointers for indirect or indexed access of SMEM 159 at 36-bit locations. An incrementer 707 is provided to facilitate indexed mode access of SMEM 159.

Zigzag memory 704 and window memory 705 are described below in conjunction with VLC 109 and motion estimator 111.

4. Memory Controller 104

Chip 100 accesses external memory 103, which is implemented by dynamic random access memory (DRAM). Controller 104 supports one, two or four banks of memory, and up to a total of eight megabytes of DRAM.

Memory controller 104 manages the accesses to both external memory 103 and the internal registers. In addition, memory controller 104 also (a) arbitrates requests for the use of global bus 120 and W bus 180a; (b) controls all transfers between external memory 103 and the functional units of chip 100, and (c) controls transfers between QG registers ("QGMEM") 810 and SMEM 159. Figure 8 is a block diagram of memory controller 104. QGMEM 810 is a 128-bit register which is used for block transfer between 144-bit SMEM 159 and 32-bit global bus 120. Thus, for each transfer between QGMEM 810 and SMEM 159, four transfers between global bus 120 and QGMEM 801 would take place. A guard-bit mechanism, discussed below, is applied when transferring data between QGMEM 810 and SMEM 159.

As shown in Figure 8a, an arbitration circuit 801 receives requests from functional units of chip 100 for data transfer between external memory 103 and the requesting functional units. Data from external memory 103 are received into input buffer 811, which drives the received data onto global bus 120. The requesting functional units receive the requested data either over global bus 120, or over processor bus (i.e. W bus) 180a in the manner described below. Data to be written into external memory 103 are transferred from the functional units over either w bus 180a or global bus 120. Such data are received into a data buffer 812 and driven on to memory data bus 105a.

W bus 180a comprises a 36-bit data bus 180a-1 and a 6-bit address bus 180a-2. The address and data busses 180a-1 and 180a-2 are pipelined so that the address on address bus 180a-2 is associated with the data on data bus 180a-2 in the next cycle. The most significant bit of address bus 180a-2 indicates whether the operation reads from a register of a functional unit or writes to a register of a functional unit. The

remaining bits on address bus 180a-2 identify the source or destination register. Additional control signals on W bus 180a are: (a) isW_bsy (a signal indicating valid data in the isWrite Register 804), (b) Wr_isW (a signal enabling a transfer of the content of data bus 180a-1 into isWrite Register 804), (c) req_W5_stall (a signal requesting W bus 108a 5 cycles ahead), and (d) Ch1_busy (a signal to indicate that channel 1, which is RMEM 154, is busy).

In memory controller 104, a channel memory 802 and an address generation unit 805 control DMA transfers between functional units of chip 100 and external memory 103. In the present embodiment, channel memory has eight 32-bit registers or entries, corresponding to 8 assigned channels for DMA operations. To initiate a DMA access to external memory 103 or an internal control register, the requesting device generates an interrupt to have CPU 150 write, over W bus 180a, a request into the channel memory entry assigned to the requesting device. The portion of external memory 103 accessed by DMA can be either local (i.e. in the address space of the present chip) or remote (i.e. in the address space of another chip).

In the present embodiment, channel 0 is reserved for preforming refresh operations of external memory 103. Channel 1 allows single-datum transfer between external memory 103 and RMEM 154. Channel 2 is reserved for transfers between host interface 102 and either external memory 103 or internal control registers. Figures 8b and 8d provide the bit assignment diagrams for channel memory entries of channels 1 and 2 respectively. Channels 3-7 are respectively assigned to data transfers between either external memory 103, or internal control registers, and (a) video bus 107, (b) video bus 108, (c) VLC FIFO 703 of VLC 109 and VLD 110, (d) SMEM 159, and (e) instruction memory 152. Figure 8c provides the bit assignment diagrams of the channel memory entries of channels 0 and 3-7.

For all channel entries, bit 0 indicates whether the requested DMA access is a read access or a write access. In the channel memory entry of channel 1 (Figure 8b), bits 31:24 are used to specify ID of a "remote" chip, when the address space of the remote chip is accessed. If access to the address space of a remote chip is requested, bit 1 is also set. In the channel memory entry of channel 1, bit 23 indicates whether the DMA access is to external memory 103 or to a control register of either global bus 120 or W bus 180a. When the access is to a control register of W bus 180a, bit 21 is also set. For channels 0, 3-7, bits 31:23 provide a count indicating the number of 32-bit words to transfer. For channels 3 and 4 (video buses 107 and 108), the count is a multiple of 16. For channel 6 (SMEM 159), the count is a multiple of 4.

Referring back to Figure 8a, external DRAM controller 813 maps the addresses generated by address generation unit 805 into addresses in external memory 103. DRAM controller 813 provides conventional DRAM control signals to external memory 103. The output signals of DRAM controller 813 are provided on memory address bus 105b.

In this embodiment, a word in external memory 103 or on host bus 101 is 32-bit long. However, in most internal registers, and on W bus 180a, a data word is 36-bit long. To save the four bits not transferred to external memory 103, or host bus 101, a guard-bit register stores the data bits 35:32 that are driven onto global bus 120. For data received from a 32-bit data source, the "Inbit" field of the guard bit register supplies the missing four bits.

A priority interrupt encoding module 807 receives interrupt requests from functional units and generates interrupt vectors according to a priority scheme for CPU 150 to service. An interrupt is generated whenever a channel in channel memory 802 is empty and the channel's interrupt enable bit (stored in an interrupt control register) is set. In this embodiment, the interrupt vector is 4-bit wide to allow encoding of 16 levels of interrupt.

Transactions on global bus 120 are controlled by a state machine 804. Global bus 120, which is 32-bit wide, is multiplexed for address and data. Two single-bit signals GDATA and GVALID indicate respectively whether data or address is placed on global bus 120, and whether valid data or address is currently on global bus 120. Additional single-bit control signals on global bus 120 are IBreq (video input port requests access to external memory), OBreq (video output requests access to external memory), VCreq (VLC requests access to external memory), VDreq (VLD requests access to external memory), IBdmd (Video input is demanding access to external memory), and OBdmd (video output is demanding access to external memory).

During a valid address cycle, memory controller 104 drives an address onto global bus 120. In such an address, bit 6 (i.e. the seventh bit from the least significant end) of the 32-bit word is an "read or write" bit, and indicates whether the bus access reads from or write to global bus 120. The six bits to the right of the "read or write" bit constitute an address. By driving an address of a functional unit on to global bus 120, memory controller 104 selects the functional unit for the access. Once a functional unit is selected, the selection remains until a new address is driven by memory controller 104 on to the global bus. While selected, the functional unit drives output data or reads input data, according to the nature of the access,

until either the GVALID signal is deasserted, or the GDATA signal is negated. The negated GDATA signal signifies a new address cycle in the next system clock period.

An arbitration scheme allows arbitration circuit 801 to provide fairness between non-real time channels, such as SMEM 159, and real-time channels, such as video ports 107 and 108, or VLC 109. In general, a channel memory request from a functional unit is pending when (a) a valid entry of the functional unit is written in channel memory 802, (a) the mask bit (see below) of the functional unit in an enable register for the request is clear, and (c) the functional unit's request signal is asserted. For channels 3 and 7 (i.e. SMEM 159 and instruction memory 152), a request signal is not provided, and a valid entry in channel memory 802 suffices.

In this embodiment, the real-time channels have priority over non-real time channels. Arbitration is necessary when more than one request is pending, and occurs after memory controller 104 is idle or has just finishes servicing the last request. In this embodiment, each non-real time channel, other than RMEM, is provided with a mask bit which is set upon a completion of request, if another non-real time request is pending. All of the non-real time mask bits are cleared when no non-real time request is outstanding. Real time channels are not provided with mask bits. Thus, a real time channel request can always proceed, unless preempted by a higher priority request. DRAM refresh is the highest priority real time channel.

An exception to the rule that priority of a real time channel over a non-real time channel occurs when the mask bit for RMEM operation is clear and an RMEM operation (i.e. load or store operation) becomes pending. Under this exception, memory controller 104 allows an ongoing request to be interrupted in favor of the RMEM operation. If a second RMEM operation becomes pending prior to the completion of the first RMEM operation, the second RMEM operation is also allowed to proceed ahead of the interrupted request. Up to three such preemptive RMEM operations are allowed to proceed ahead of an interrupted request. Thereafter, memory controller 104 sets the mask bit for an RMEM operation, and the interrupted request is allowed to resume and proceed to completion.

IsWrite register 804 and isRead register 805 are registers provided to support store and load operations of internal registers (i.e. registers in RMEM 154) to and from external memory 103. During a load operation, CPU 150 writes over W bus 180a a request into channel 1 of channel memory 802. When memory controller 104 begins to service the requested load operation, memory controller 104 asserts the "req_W5_stall" signal to reserve five cycles ahead a slot for the use of W bus 180a. When the requested data is received from DRAM, the data is driven on to global bus 120. At the same time, channel memory 802 asserts the signal Rd_isR signal, which latches into isRead register 805 the data on global bus 120. In the following cycle, the content of the isRead register 805 is driven onto the W bus 180a and latched into the specified destination in RMEM 154 to complete the load operation.

In a store operation, data from RMEM 154 is driven onto W bus 180a, which is latched by IsWrite register 804. In the following cycle, CPU 150 writes a channel request into channel 1 in channel memory 802 over W bus 180a. Memory controller 104 asserts signal isW_Bsy to indicate valid data in isWrite register 804 and to prevent CPU 150 from overwriting isWrite register 804. When memory controller 104 is ready to service the store request, the isW_Bsy signal is deasserted and the content of isWrite register 804 is driven onto global bus 120 in the following cycle. The data is latched into output buffer 812 for storing into external memory 103 over memory data bus 105a.

The present embodiment supports up to a total of 8 megabytes of external DRAM. Figure 9a shows a configuration 900 in which external memory 103 is a 4-bank memory interfaced to chip 100. To support this configuration, chip 100 provides two "row address strobe" (RAS) signals 908 and 909, and two column address strobe (CAS) signals 906 and 907. RAS signals 908 and 909, CAS signals 906 and 907 are also respectively known as RAS_1 and RAS_0, and CAS_1 and CAS_0 signals.

Memory bus 105 comprises a 32-bit data bus 105a and an 11-bit address bus 105b. To support scan-line mode accesses, discussed below, two output terminals are provided in chip 100 for word address bit 1 (i.e. byte address 3, or A3). Thus, address bus 105b is effectively 10-bit wide. As shown in Figure 9a, four banks 901-904 of DRAM are configured such that bank 901 receives address strobe signals RAS0 and CAS0, bank 902 receives address strobe signals RAS_0 and CAS_1, bank 903 receives address strobe signals RAS_1 and CAS_1, bank 904 receives address strobe signals RAS_1 and CAS_0.

External memory 103 supports both interleaved and non-interleaved modes. In non-interleaved mode, only two banks of memory are accessed, using both RAS signals and one (CAS_0) CAS signal. Thus, in non-interleaved mode, banks 902 and 903 are not accessed. Under one mode of interleaved DRAM access, banks 0 and 2, both receiving the signal CAS_0, form an "even" memory bank, while banks 1 and 3, both receiving the signal CAS_1, form the "odd" memory bank. In the present embodiment, address bit 2, which is used to generate the signals CAS_0 and CAS_1, distinguishes between the odd and even banks.

Interleaved access to external memory 103 is desirable because of the efficiency inherent in overlapping memory cycles of the interleaved memory banks. However, the manner in which data is accessed determines whether such efficiency can be achieved. Generally speaking, with respect to the location of pixels on a video image, chip 100 fetches video data in two different orders: "scan-line" mode, or "reference mode". Under scan-line mode, the access pattern follows a line by line access of the pixels of a display. Under reference mode, pixels are accessed column by column. To support scan-line mode, each bank of memory is divided into two half-banks, each half-bank receiving independently the signal on one of chip 100's two terminals for word address bit 1. In scan-line mode, under certain conditions described below, these two terminals may carry different logic levels to result in a different word address being access in each half-bank.

Figure 9b is a timing diagram showing interleaved accesses to data in the odd and even banks of Figure 9a. In Figure 9b, two page mode read operations and two page mode write operations are performed in each of the odd and even banks. The protocol shown in Figure 9b is for reference mode access, and is not suitable for use under scan-line mode. This is because, under interleaved reference mode, the same column address is used to access both the even and odd banks. Consequently, as shown in Figure 9a, chip 100 generates a single address, which is latched by address latch 905, for both the odd and even banks. However, under interleaved scan-line mode, separate column addresses are generated for the even and odd banks.

In configuration 900, signal CAS_1 turns off address latch 905 to keep the column address stable for the odd memory bank. In Figure 9b, the bus name "Address" represents the signals on memory address bus 105b. The designation "RAr" "CAr12" and "CAr34" represents respectively (a) a row address, (b) a column address for data R1 and R2 and (c) a column address for data R3 and R4. The arrivals of the data signals at the even and odd banks are illustrated by the signals "DATA0" and "DATA1" respectively.

In the example illustrated by Figure 9b, the same column address is used to access data words R1 and R2 and a different column address is used to access data words R3 and R4. Column address CAr12 is latched two cycles apart into the even and odd banks at times t_1 and t_2, respectively. Likewise, column address CAR34 is latched into even and odd memory banks at times t_3 and t_4 respectively. The address of the destination, and data words R1, R2, R3 and R4 are driven onto global bus 120 (the signals represented by "GDATA") at consecutive cycles in Figure 9b.

Figure 9b also shows an interleaved write access, using the same column address "CAw23" (i.e. the column address for data W2 and W3), which is latched at times t_6 and t_7 (i.e. separated by two clock cycles), into the even and odd banks of configuration 900. Again, the protocol in Figure 9b is used under reference mode, but is not suitable for scan-line mode access.

Figure 9c is a timing diagram showing interleaved access of the memory system in configuration 900 under scan-line mode, where the column address for consecutive data words are different. In Figure 9c, the column addresses for data words R1-R4, represented by "CAr1", "CAr2", "CAr3" and "CAr4", are separately provided at least 4 clock cycles apart. Data words R1 and R3 are stored in the odd memory bank, and data words R2 and R4 are stored in the even memory bank. Both column address strobe signals CAS_0 and CAS_1 are asserted once every six clock cycles. The time period between assertions of the signals CAS_0 and CAS_1 is four clock cycles.

Memory controller 104 generates addresses for accesses to external memory 103. To efficiently support both the fetching of reference frames, during motion estimation, and the scan-line mode operation, during video data input and output, two pixel arrangements are used to stored video data in external memory 103. The first arrangement, which supports scan-line mode operation is shown in Figure 10a. The second arrangement, which supports reference frame fetching during motion estimation, is shown in Figure 10b.

Figure 10a shows an arrangement 1000a which supports scan-line mode operation. In the present embodiment, each access to external memory 103 fetches a 32-bit word comprising four pixels. In external memory 103, a 32-bit data word is used to store four pixels arranged in a "quad pel", i.e. the four pixels are arranged in a 2 X 2 pixel configuration on the screen. Under scan-line mode, however, the pixels desired are four adjacent pixels on the same scan line. Thus, under scan-line mode, the four pixels fetched are taken from two data words in external memory 103.

In Figure 10a, the pixels, each represented by a symbol Pxy, are labelled according to the positions they appear on a display screen, i.e. 'Pxy' is the label given to the pixel at row x and column y. Under the label Pxy of each pixel is a hexadecimal number which represents the byte address (offset from a base address) of the pixel as it is stored in external memory 103. For example, the quad pel comprising pixels P00, P01, P10, and P11 is stored at word address 0 (hexadecimal), which includes the byte addresses 0-3. As a matter of convention, in the following detailed description, the term "quad pel Pxy" is understood to

mean the quad pel in which the upper left pixel is labelled Pxy.

Figure 10a also illustrates a collective term for a number of pixels called a "tile". A "tile" comprises four quad pels arranged in a 2 X 2 configuration. For example, the square area defined by quad pels P00, P02, P20 and P22 is a tile. As a matter of convention, in the following detailed description, the term "tile Pxy" is understood to mean the tile in which the quad pel at its upper left hand corner is quad pel Pxy. As mentioned above, under scan-line mode access, four horizontally adjacent pixels are accessed at a time. Again, as a matter of convention, in the following discussion, the term "scan line Pxy" is understood to mean the group of four horizontally adjacent pixels which left most pixel is Pxy.

In arrangement 1000a, each tile is stored in four consecutive words of external memory 103. For example, tile P00 are stored consecutive memory words which addresses 0, 4, 8 and C (big Endian format). In addition, within each word is stored a quad pel. In the present embodiment, the odd memory bank has addresses which bit 2 has bit value '1' and the even memory bank has addresses which bit 2 has bit value '0'. Thus, for example, both quad pels P00 and P02 are stored in the even bank, and quad pels P20 and P22 are stored in the odd bank.

In arrangement 1000a, the order in which the upper and the lower halves of a quad pel is stored is determined by bit 3 of the memory address. By convention, the upper half of a quad pel refers to the two pixels of the quad pel occupying the "higher" screen positions. For example, since bit 3 of the word address (=0) of quad pel P00 has bit value '0', the upper halfword stores the lower half of quad pel P00 (i.e. pixels P10 and P11), and the lower halfword stores the upper half of quad pel P00 (i.e. pixels P00 and P01). As used here, the upper halfword refers to the half of the data word having the greater byte addresses. However, since bit 3 of the byte address (=8) of quad pel P02 has the bit value '1', the upper halfword (i.e. addresses A and B) stores the upper half of the quad pel P02 (i.e. pixels P02 and P03), while the lower half of quad pel P02 (i.e. P12 and P13) is stored in the lower halfword (addresses 8 and 9). As explained below, this alternative pattern of swapping the upper and lower halves of the quad pel every other memory word supports the scan-line access mode.

In addition, to support scan-line mode, the upper and lower halves of the memory word are independently addressed. Specifically, under scan-line mode, bit 3 in the column address provided to access each half of the memory word is different. This is accomplished by providing a different value on two word address bit 1 output terminals (i.e. A3) of chip 100. For example, when fetching the scan line P00, the upper halfword retrieves from address 8 (i.e. bit 3 of byte address 0 toggled) pixels P02 and P03, and the lower halfword retrieves from word address 0 pixels P00 and P01. In arrangement 1000a, both halfwords in each 4-pixel scan line fetch are retrieved from the same even or odd memory bank.

Memory controller 104 provides the address translation necessary to translate the address from CPU 150 ("logical address" or "LA") to the address actually provided to each halfword in each memory bank ("physical address" or "PA"). Since byte address bits PA[1:0] are not involved in addressing in external memory 103, which receives only word addresses, mapping between logical addresses and physical addresses in these bits are provided by byte swapping in memory controller 104.

Specifically, under arrangement 1000a, when a quad pel is fetched for a non-scan line access, only one address bit is translated to ensure the upper and lower halves of the quad pel are swapped when the logical byte address bit LA[3] is '1'. The mapping memory controller 104 generates maps the logical address to the the physical address according to the following equations:

$$PA[0] = LA[0]$$
$$PA[1] = LA[1] \veebar LA[3]$$
$$PA[9:2] = LA[9:2]$$

where PA[1] is bit 1 of the physical byte address, and LA[3] and LA[1] are the bits 3 and 1 of the logical byte address. The $\veebar$ operator is the "exclusive-OR" operator. In this instance, the physcical address provided to both halfwords of the memory bank addressed are the same.

The logical addresses of the pixels under scan-line mode are shown in Figure 10c. The logic circuit in memory controller 104 generates the physical address according to the following equations:

Thus, under scan-line mode, memory controller 104 (a) accesses (i) in an even scan line (i.e. scan line Pny, where n is even), the left half of the scan line in the

$$PA[0] = LA[0]$$
$$PA[1] = LA[2] \veebar LA[1]$$
$$PA[2] = LA[3]$$
$$PA[3] = LA[1]$$
$$PA[9:4] = LA[9:4]$$

lower halfword, and the right half of the scan line in an upper halfword; (ii) in an odd scan line (i.e. scan line Pny, where nis odd), the left half of the scan line in the upper halfword and the right half of the scan line in the lower halfword; (b) switches, every two scan lines, between accessing the odd memory bank to accessing the even memory bank; (c) accesses, for the right half of a scan line, a halfword which physical byte address is offset by 8 from the physical byte address of the halfword containing the left half of the scan line (i.e. different values for the two address bits A3 of chip 100).

Arrangement 1000b shown in Figure 10b supports reference fetch accesses. The logical addresses for a reference frame are shown in Figure 10d. Under this arrangement, a tile is fetched by fetching the four quad pels in the order of top-left, top-right, bottom-left and bottom-right. In fetching a reference macroblock, tiles are fetched column by column and, within a column, from top to bottom. For example, in Figure 10b, tile P00 is fetched in the order of quad pels P00, P02, P20 and P22. The reference frame is fetched by fetching tiles P00, P40, P80, PC0, P04, P44, P84, PC4 ... etc. To take advantage of the efficiencies of memory interleaving and page mode accesses, arrangement 1000b is arranged such that the top-left quad pel and the bottom-left quad pel are located in the even memory bank, and the top-right and bottom-right quad pels are located in the odd memory bank.

To minimize delay due to page crossings during a reference frame fetch, memory controller fetches all the tiles of the reference frame in the upper DRAM page before fetching the tiles in the lower DRAM page. Figure 10e illustrates a reference frame fetch which crosses a memory page boundary.

Figure 10e shows four tiles 1050a-1050d of a reference frame. In each quad pel of each tile, the hexadecimal numbers at the four corners of the quad pel are physical byte addresses at which the four pixels of the quad pel are stored. For example, the four pixels of quad pel 1 of tile 1050d are stored at physical byte addresses 7E, 7F, 7C and 7D. In Figure 10e, the DRAM page boundary is between the upper half-tile and the lower half-tile in each of the tiles 1050c and 1050d shown in Figure 10e. If a reference fetch starts at address 28, the page boundary is encountered after fetching the quad pel 1 of tile 1050c, which is located at physical byte address 3C. At that point, detecting the page boundary, memory controller 104 generates address 68 rather than x0 to fetch the remaining quad pels of the tiles in the upper DRAM page, rather than crossing over to the lower DRAM page. According to arrangement 1000b of Figure 10b, in a reference frame access, address 68 is in the same memory bank as address 38 and in the opposite memory bank of address 3C. Consequently, in making the jump from address 3C to address 68, interleaved access is not interrupted.

As mentioned above, data transfers between SMEM 159 and external memory 103 take place through QGMEM 810 and global bus 120. Figures 11a and 11b are timing diagrams showing respectively the data transfers from external memory 103 to SMEM 159, and from SMEM 159 to external memory 103. As mentioned above, the data bus portion of global bus 120 is 32-bit, and the interface between QGMEM 810 and SMEM 159 is 128-bit. A 2-bit signal bus Qptr is provided to indicate which of the four 32-bit words ("QG registers") in QGMEM 810 is the source or destination of the 32-bit data on global bus 120. A 1-bit signal "req_smem_stall" indicates two cycles ahead an impending access by QGMEM 810 to SMEM 159, to prevent CPU 150 from accessing SMEM 159 while the QGMEM access is performed.

As shown in Figure 11a, at cycles 1 and 2, a request for DMA data transfer is written into channel memory entry 6 to signal a data transfer from external memory 103 to the SMEM 159. As each 32-bit word is received on memory data bus 105a, memory controller 104 drives the data word onto global bus 120. For example, datum D0 is driven onto global bus 120 during cycles 5 and 6. In this example, the first 32-bit datum is scheduled to be written to the first of four QG registers of QGMEM 810. The destination in QGMEM 810 for datum D0 is indicated in cycles 3 and 4 in the 2-bit Qptr signal bus. The asserted "qgreq" signal enables data on global bus 120 to be written into QGMEM 810. Thus, datum D0 is written into QGMEM 810 during cycles 5 and 6. Datum D1 is likewise written into QG register 810 during cycles 7 and 8. A transfer between QGMEM 810 and SMEM 159 is signalled two cycles ahead by asserting "q_smem_stall", which is usually asserted in an external memory to SREM 159 transfer when QGMEM 810 holds three valid data not already written into SMEM 159, and the fourth datum is currently on global bus 120, e.g. in cycle 14. During cycle 15, all four QG registers of QGMEM 810 are written into SMEM 159.

Figure 11b shows a transfer between SMEM 159 to external memory 103. During cycles 1 and 2, a transfer request is written into channel memory entry 6 to signal a block memory transfer from SMEM 159 to external memory 103. In this example, the four QG registers of QGMEM 810 have been previously loaded from SMEM 159. The 2-bit QGptr signal selects which of the four QG registers of QGMEM 810 is active. While qgreq is asserted, the data in the 32-bit register of QGMEM 810 corresponding to the value of QGptr are driven onto global bus 120. In this example, data D0 and D1 are driven onto global bus 120 during cycles 5, 6, 7 and 8. A data transfer between QGMEM 810 and SMEM 159 is signalled three cycles ahead by asserting the signal "q_smem_stall", which is usually asserted in an SREM 159 to external memory transfer when QGMEM 810 holds only one datum not already written onto global bus 120, and one datum is currently on global bus 120, e.g. in cycle 11. During cycle 15, the four QG registers of QGMEM 810 are loaded with a 32-bit portion from a 144-bit word of SMEM 159.

To support reference fetch, the 2-bit Qptr signal bus does not always cycle through 0-3 to access all four 32-bit registers of QGMEM 810. Each of the four 32-bit registers of QGMEM 810 provides a "dirty bit" to indicate whether the 32-bit word is valid data. One example in which not all QG registers of QGMEM 810 contain valid data is found in a reference fetch where a page boundary is encountered. Under such condition, as mentioned above, the quad pels in the current page of memory is fetched prior any quad pel in a different page of memory is accessed. For example, referring to Figure 10e, instead of fetching the quad pel at addresses x0-x3 after the quad pel at addresses 3C to 3F are fetched, memory controller 140 next fetches the quad pel at 68 to 6B. In QGMEM 810, the dirty bits associated with the lower two 32-bit words (i.e. the QG registers containing the values of memory words at addresses 38-3B and 3C-3F) are set. When data words at addresses x0-x3 and x4-x7 are fetched, the dirty bits for the remaining two 32-bit words of QG register 810 are set.

CPU 150

As mentioned above, CPU 150 includes instruction memory 152, RMEM 154, byte multiplexor 155, ALU 156, MAC 158, and SMEM 159, which includes AMEM 160. CPU 150 is a pipelined processor. Figure 12 illustrates the pipeline stages of CPU 150. As shown in Figure 12, an instruction is fetched during stage 1201 from instruction cache 152. The instruction fetch during stage 1201 is completed during stage 1202. Further, during stage 1202, the instruction decode logic determines if a branch instruction is included as a minor instruction. If a branch instruction is included as a minor instruction, evaluation of the branch instruction is performed. During stage 1203, depending on the nature of the instruction, instruction decode, operand fetch from RMEM 154 and address generation for SMEM 159 can occur.

The decoded instruction to ALU 156 is executed during stage 1204, and the results written into RMEM 154 or PMEM 702 during stage 1205, unless the instruction requires use of multiplier 158. Multiplier 158 is a four-stage pipeline multiplier. A multiply instruction, such as required in DCT or IDCT operations, is performed in MAC 158 in 4 pipelined stages 1204-1207. The result of a multiplication in MAC 158 is written back at stage 1208.

During stage 1204, if the instruction requires data transfer between SMEM 159 and global bus 120, or requires data transfer between SMEM 159 and processor bus 180a, such data transfer is initiated during stage 1204. Data transfer between processor bus 180a and SMEM 159 are completed during stage 1205.

ALU 156 performs 32-bit, 18-bit and 9-bit arithmetic operations and 32-bit logic operations. Since the data path of ALU 156 is 36-bit wide, each 36-bit datum comprises either four 9-bit bytes, two 18-bit halfwords or a 36-bit word (including four guard bits, as explained above). A 36-bit word in CPU 150 can represent the following "extended precision" bytes or halfwords:

Byte[0] = x[35,31:24];
Byte[1] = x[34,23:16];
Byte[2] = x[33,15:8];
Byte[3] = x[32,7:0];
halfword[0] = x[35:34,31:16];
halfword[1] = x[33:32,15:0].

Since external memory 103 is 32-bit wide, load and stores from external memory 103 yields only 32-bit words, 16-bit halfwords and 8-bit bytes.

Each instruction of CPU 150 can contain, in addition to a major instruction, a minor instruction and a condition test. Operands of a major instruction can be specified by a 5-bit immediate value in the instruction, a 14-bit immediate value in the instruction, or references to registers in RMEM 154. A minor instruction can be (a) a load or store instruction to SMEM 159, (b) increments or decrement instruction to AMEM 706, (c) a major instruction modifier (also known as a "post-ALU" instruction), e.g. the "divide-by-

two" d2s instruction for dividing the result of an ALU operation by 2, or (d) a branch instruction. A condition test can be specified, if the major instruction's destination register is R0, or the destination register matches the second source register.

In this embodiment, a branch immediate instruction specifies a 9-bit jump target, which includes a 1-bit page change flag. The 1-bit page change flag indicates whether or not the jump is within the same bank of instruction memory 152. In this embodiment, IMEM 152 has four 256-word pages. A branch immediate instruction, other than a branch instruction in page 0, can have a jump target within its own page, or in page zero. However, a branch immediate instruction in page 0 can have a jump target within page 0 and page 1. Jump targets outside of the designated pages can be accomplished by an indirect branch instruction.

Figure 15a is a block diagram of arithmetic unit 750, including the three M-, W- and Z-bypass mechanisms 1402, 1401 and 1402. These bypass mechanisms allow the results of a previous instructions to be made available to a subsequent instruction without first being written back into the register files. As shown in Figure 15a, multiplexors 1543 and 1544 each select one of four data sources into the X and Y input terminals of ALU 156. The four data sources are the output data on the M-, W-, and Z-bypasses and the output of byte multiplexors 1541 and 1542. Multiplexor 1543 receives from byte multiplexor 1541 a 36-bit word comprising four 9-bit bytes designated bytes A0, A1, A2 and A3. Similarly, Multiplexor 1544 receives from byte multiplexor 1542 a 36-bit word comprising four 9-bit bytes B0, B1, B2 and B4. ALU 156 is an arithmetic logic unit capable of addition, subtraction and logical operations. The output data of ALU 156 can be provided to circuit 1410 for post-ALU operations. The output data from post-ALU operation circuit 1410 can be provided to MAC 158 for further computation involving a multiplication.

Figure 14a and 14b shows schematically the byte multiplexors 1541 and 1542 which multiplex source operends each fetched from QMEM 701 or RMEM 154. In Figures 14a and 14b, registers 1470 and 1471 reprsent two 36-bit source arguments each from RMEM 154 or QMEM 701 specified as source registers of an ALU instruction. The designations '0', '1', '2' and '3' shown in Figures 14a and 14b in each of registers 1470 and 1471 represent respectively the 9-bit bytes 0-3. In the applications of interest, bytes 0-3 represent, respectively, the upper-left, the upper-right, the lower-left and the lowr-right pixels of a quad pel. Each byte multiplexor 1451 and 1452 provide a 36-bit datum output, which includes four 9-bit bytes extracted from the the two 36-bit input data to the byte multiplexor. Figure 14a shows the four output bytes A0, A1, A2 and A3 of byte multiplexor 1451, and Figure 14b shows the four output bytes B0, B1, B2 and B3 of byte multiplexor 1452.

In byte multipexer 1452, each output byte is selected from one of the corresponding bytes of the source registers or zero. That is, for byte B*i*, byte multiplexer 1452 selects either byte *i* of register 1470 or byte *i* of register 1471 or zero. In byte multiplexer 1451, in addition to selecting corresponding bytes from registers 1470 and 1471, each output byte can be selected from two additional configurations, designated "h" and "v" in Figure 14a. Configuration "h" is designed, when registers 1470 and 1471 contain horizontally adjacent quad pels, to extract the quad pel formed by the right half of the quad pel in register 1470 and the left half of the quad pel in register 1471. Similarly, configuration "v" is designed, when two vertically adjacent quad pels are contained in registers 1470 and 1471, to extract the lower half of the quad pel in register 1470 and the upper half of the quad pel in register 1471. Such byte swapping allows various operations on quad pels to be performed efficiently. In the present embodiment, the following major instructions uses the byte multiplexors 1541 and 1542 to rearrange operands for ALU 156:

DMULH -	performs a dequantization multiplication (halfword multiplies) after unpacking the higher order two bytes of each source operand into two halfwords. (major instruction)
DMULL -	performs a dequantization multiplication (halfword multiplies) after unpacking the lower order two bytes of each source operand into two halfwords.
HOFF, VOFF -	extracts a shifted quad pel from two horizontally or vertically adjacent quad pels; four shift positions: 0, 0.5, 1.0 and 1.5 are available.
HSHRINK, VSHRINK -	performs horizontal and vertical 2:1 decimation of quad pel (i.e. half resolution), using adjacent quad pels.
PACK -	packs the four halfwords of two 36-bit words into the four bytes of a 36-bit word.
STAT1, STAT2 -	activity statistics instructions (see below)

Further, minor instructions OFFX, OFFY, SHX, SHY, and STAT each set the byte multiplexors 1541 and 1542 to the configuration used by the HOFF, VOFF, HSHRINK, VSHRINK, and STAT1 or STAT2 instructions respectively. In addition, two minor instructions UNPACKH and UNPACKL each set the byte multiplexors for unpacking bytes into halfwords used by the DMULH and DMULL instructions.

Figure 15d(i) illustrates the operations of the byte multiplexors 1541 and 1542, using one mode of the HOFF instruction. In Figure 15d(i), the input adjacent quad pels A and C are represented by circles. The quad pels A and C are fetched and presented to the byte multiplexors 1541 and 1542. Under this mode of instruction HOFF, all four byte positions of multiplexer 1541 are set to the "h" configuration, and multiplexor 1543 selects the output data of multiplexer 1541 for the X operand input terminals of ALU 156. From the above discussion, it is known that quad pel B is obtained by byte multiplexors 1541 selecting left and right halves of the input quad pels A and C, respectively. The filtered output for this mode of the HOFF instruction is obtained by summing quad pel A with quad pel B. Thus, byte multiplexor 1541 provides at the X operand input terminals of ALU 156 quad pel B, which is given by:

B[byte0] = A[byte1]
B[byte1] = C[byte0]
B[byte2] = A[byte3]
B[byte3] = C[byte2].

For the Y operand input terminals of ALU 156, all four byte positions of byte multiplexor 1542 are set to select quad pel A. The result of ALU 156 is a quad pel Z, given by summing quad pels A and B in four 9-bit additions:

Z[byte0] = A[byte0] + B[byte0];
Z[byte1] = A[byte1] + B[byte1];
Z[byte2] = A[byte2] + B[byte2];
Z[byte3] = A[byte3] + B[byte3];

After modification using a divide by two post-ALU operation, quad pel Z represents a quad pel located 1.5 pixels to the right of the input pixel C. Other modes of the HOFF instruction can be specified by setting two bits in ALU 156's configuration registers. The other modes of the HOFF instruction allow extraction quad pels located 0, 0.5, and 1.0 pixel positions from input pixel C, by providing, respectively, (i) quad pel C to the X input terminals of ALU 156 and four zero bytes in the Y input terminals of ALU 156; (ii) quad pel B (configuration "h") at the X input terminals of ALU 156, and quad pel C at the Y input terminals of ALU 156; and (iii) quad pel B (configuration "h") at the X input terminals of ALU 156, and four zero bytes at the Y input terminals of ALU 156.

An analogous example is illustrated in Figure 15d(ii) by the VOFF instruction. Under the VOFF instruction, the filtered quad pel Z is the sum of quad pels A and B, quad pel B being derived from input quad pel A and C using the byte multiplexor 1541 in the "v" configuration for all byte positions. In this instance, quad pel Z represents a quad pel located 1.5 pixels above quad pel C.

Applications for byte multiplexors 1541 and 1542 of ALU 156 are further illustrated in Figure 15d(iii) and 15d (iv) by one mode in each of the HSHRINK and VSHRINK instructions, respectively. As shown in the specified mode of the HSHRINK instruction of Figure 15d(iii), the HSHRINK instruction provides decimation in the horizontal direction by averaging horizontally adjacent pixels of the input quad pels A and B. Similarly, as shown in the specified mode of the VSHRINK instruction shown in Figure 15d(iv), the VSHRINK instruction provides decimation in the vertical direction by averaging vertically adjacent pixels of the input quad pels A and B. To achieve HSHRINK function in one instruction cycle, the quad pels A and B are presented to byte multiplexors 1541 and 1542. All four byte positions of byte multiplexor 1541 are set to the "h" configuration and multiplexor 1543 selects the output datum (i.e. quad pel "C") of byte multiplexor 1541 as X input operand to ALU 156. Quad pel C is derived from quad pels A and B according to:

C[byte 0] = A[byte 1]
C[byte 1] = B[byte 0]
C[byte 2] = A[byte 3]
C[byte 3] = B[byte 2].

Quad pel C is indicated in Figure 15d by the pixels marked "X". For the Y input operand of ALU 156, byte multiplexor 1542 selects a quad pel D, which is indicated in Figure 15d(iii) by the pixels marked "T". Quad pel D is achieved by setting byte positions 0 and 2 of multiplexor 1542 to select from quad pel A and byte positions 0 and 1 to select from quad pel B. Quad pel D is given by:

D[byte 0] = A[byte 0]
D[byte 1] = B[byte 1]
D[byte 2] = A[byte 2]
D[byte 3] = B[byte 3].

The decimated output is a quad pel Z, which is the result of summing Quad pels C and D in four 9-bit additions, in conjunction with a post-ALU divide by 2 operation. Quad pel Z represents a 2:1 decimation of quad pels A and B.

The operation of VSHRINK instruction is similar to the operation of the HSHRINK instruction.

A schmatic diagram of MAC 158 is shown in Figure 15b. MAC 158 is designed to efficiently implement various functions, including a weighted average ("alpha filter"). As shown in Figure 15b, MAC 158 receives two 36-bit input data, which are respectively labeled "X "and "Z". Input datum Z is taken from the output datum of ALU 156, which can be used to compute the sum or difference of two values. A multiplexer 1502 outputs a datum 1522, being one of the following values: the input datum Z, a factor alpha, or the sign of input datum Z (represented by 1 and -1, for datum Z being greater or equal to zero and less than zero, respectively). Another multiplexor 1501 selects as output datum 1521 either the input datum X or the input datum Z. Data 1521 and 1522 are provided to multiplier 1503 as input data. The output datum 1523 of the multiplier 1503 can be summed in adder 1506 with a datum 1524, which is the output datum of multiplexor 1504. Datum 1524 is one of the following: the output datum of accumulator 1505, a rounding factor for a quantization or dequantization multiplication step, or datum X. The output datum 1525 of adder 1506 is stored in accumulator 1505, if the instruction is a MAC instruction, or provided as a 36-bit output datum W, after shifted (i.e. scaled) and limited by scale and limit circuit 1508.

Multiplier 1503 comprises a 24-bit X 18-bit multiplier, an 18-bit X 18-bit multiplier and two 9-bit by 9-bit multipliers. Each of these multipliers can be implemented by conventional Booth multipliers. Thus, in the present embodiment, multiplier 1503 can provide one of the following groups of multiplication: (i) a 24-bit X 18-bit ("word mode"); (ii) two 18-bit X 18-bit multiplications ("halfword mode"), and (iii) four 9-bit X 9-bit multiplications ("byte mode"). Corresponding word, halfword and byte mode additions are also provided in adder 1506.

The efficiency of MAC 158 is illustrated by an example of alpha filtering in a mixing filter which is used in combining two fields in a deinterlacing operation. Figure 15c(i) shows a filter coefficient "alpha" as a function of an absolute difference between input values A and B. As applied to the deinterlacing operation, A and B denote the values of corresponding pixels (luma or chroma) in the odd and even fields of an image. In this filter, the deinterlaced image has a combined pixel value obtained by (i) equally weighting the values of A and B, when the difference between A and B does not exceed a first threshold T1; (ii) according value B a variable weight between 0.5 and 1.0, when the difference between A and B is between the first threshold T1 and a second threshold T2; and (iii) selecting value B when the difference between A and B is greater than the second threshold T2. Physically, averaging corresponding pixels using equal weights is appropriate only if an object formed by these pixels is relatively stationary between the fields (i.e. as provided by a small difference x-y). If an object moves rapidly between the fields, the corresponding pixels would have a large difference. Thus, when a large difference is seen, a larger weight should be accorded to the more recent image.

In the mixing filter illustrated in the Figure 15c(i), the difference x-y between corresponding chromas (x, y) in the odd and even fields are computed to determine the value a of alpha (scaled by 256 to allow integer multiplication). The value a of alpha is provided by specifying two parameters m and n. Specifically,

$$a = limit(127, 2*m*|x-y| + 16*(n+1), 255)$$

Figure 15c(ii) shows a circuit 1550 for computing the value a of alpha in this embodiment. In circuit 1550, circiut 1551 computes the 8-bit (unsigned) absolute difference of an 9-bit difference A-B (corresponding to the difference x-y). A shifter circuit 1552 shifts to the left the absolute difference of a number of bit positions specified by a 2-bit value. This shifting operation is equivalent to multiplying the absolute difference obtained in circuit 1551 by the aforementioned parameter m. The allowable values of m are 2, 4, 8, and 16. The shifted absolute difference is then added in circuit 1553 to one of seven values of the aforementioned parameter n selected by a 3-bit value. The allowable values of n are 16, 32, 48, 64, 80, 96, 116, 128. These values of n can be achieved by incrementing the 3-bit value by 1 and left shifting by 4 bit positions. In this embodiment, only the most significant 8 bits of the sum are retained. A limiter circuit 1554 limits the output value of alpha to between 128 and 256. The output of limiter 1554 is inverted to obtain an approximate value of negative alpha, which is provided to output bus 1522 (Figure 15b), when selected by multiplexer 1502.

The values of alpha corresponding to various values of m and n are shown in Figure 15c(iii).

This value a and the difference x-y are provided to multiplier 1503 as input data 1522 and 1521 respectively. Multiplier 1503 is programmed to right shift by 8 bits (divide by 256) to scale of the value a of alpha. The value x is provided as input datum X to MAC 158 and passed through multiplexor 1504 to adder 1506 as input 1524 to be summed with the output datum 1523 of multiplier 1503.

Thus, the equation:

$$w = x - a(x-y) = ay + (1-a)x$$

which is the basic alpha-filtering equation, is achieved in one MAC latency period. Further, since the 36-bit input data x and y may be a quad pel, alpha filtering of four pixels can be performed simultaneously under byte mode operations.

Since the value of a is limited to between 0.5 and 1, the thresholds T1 and T2 are given by the following equations:

$$T1(n,m) = \frac{64-8(n+1)}{m}$$

$$T2(n,m) = \frac{128-8(n+1)}{m}$$

Another example of alpha filtering is an adaptive temporal noise filter which blends a pixel of a previous frame with the corresponding pixel of the current frame. One implementation of the temporal noise filter is provided by the equation:

$$Y_{t+1} = aY_t + (1-a)X_{t+1} = X_{t+1} + a(Y_t - X_{t+1})$$

where X_{t+1}, Y_{t+1}, and Y_t are respectively the input pixel value for time t+1, the filtered pixel value for time t+1, and the filtered pixel value for time t. The alpha a in this equation can also be a non-linear alpha, similar to the alpha a of the mixing filter discussed above. Thus, the temporal noise filter can be implemented in the same manner as the mixed filter discussed above. Physically, the temporal noise filter eliminates sudden jumps in the pixel values between frames. The temporal noise filter can be used in decompression to reduce noise generated by the coding process. The temporal filter can also be used during compression to reduce source noise.

The STAT1 and STAT2 instructions each provide a measure of the "activity" of adjacent pixels, using both byte multiplexors 1541 and 1542, and MAC 158. Figure 15e shows, the pixels of two quad pels A and B used in either a STAT1 or a STAT2 instruction. In Figure 15e, each pixel is represented by a square, and a thick line joining two pixels represents a difference computed between the pixels. Byte multiplexors 1541 and 1542 are used to configure the X and Y input data to ALU 156, such that:

X[byte0] = A[byte1]; Y[byte0] = A[byte0];
X[byte1] = A[byte3]; Y[byte1] = A[byte1];
X[byte2] = B[byte0]; Y[byte2] = B[byte2];
X[byte3] = B[byte2]; Y[byte3] = B[byte3];

Thus, in a STAT1 instruction, a byte mode difference operation in ALU 156 computes simultaneously in the four bytes of output datum Z the differences of the adjacent pixels in each of the quad pels A and B shown in Figure 15e:

Z[byte0] = A[byte1] - A[byte0];
Z[byte1] = A[byte3] - A[byte1];
Z[byte2] = B[byte0] - B[byte2];
Z[byte3] = B[byte2] - B[byte3].

The datum Z is passed to MAC 158, which multiplies the appropriate sign to each byte of Z to obtain the absolute value of the difference computed in ALU 156 between the adjacent pixels connected by the lines of Figure 15e. Thus, four absolute differences between adjacent pixels are computed in a STAT1 instruction.

Alternatively, instead of the absolute difference computed in a STAT1 instruction, in a STAT2 instruction, multiplier 1503 squares each byte of the datum Z using byte mode multiplies, appropriately setting multiplexors 1503 and 1501 to provide the Z datum at both terminals 1521 and 1522 of multiplier 1503. Thus, four square errors between adjacent pixels are computed under a STAT2 instruction.

In either STAT1 or STAT2 instructions, the absolute differences or the square errors computed are accumulated in accumulator 1505. Consequently, multiple calls to STAT1 or STAT2 can be used to compute the activities of an area of an image. Specifically, as shown in Figure 15f, in one embodiment of

the present invention, a measure of activity is computed by accumulating over a macroblock (16 X 16 pixels) of luminance data absolute differences or square errors, using repeated calls to either a STAT1 or STAT2 instruction. The measure of activity is a metric for determining quantization step sizes. Hence, adaptive control of quantization step sizes based on an activity measure can be implemented to increase the compression ratio.

The choice of quantization constants affect the compression ratio, the quality of the resulting picture, as well as the rate at which the encoder can process the incoming video signals. For intra-coded blocks (i.e. I-Picture), the following activity statistics are computed: (a) the sum of the absolute values of the AC coefficients of in each of the four 8 X 8 blocks of the macroblock, (b) the maximum AC coefficient of each of the four 8 X 8 blocks of the macroblock, (c) the average of the four DC coefficients of the macroblock, and (d) the variance of the four DC coefficients of the macroblock. For non-intra coded blocks, the activity statistics computed are (a) as shown above, the sum of absolute differences between the luminance of adjacent pixels (STAT2), (b) the difference between the greatest and the smallest luminance value of the block, (c) the average of the four DC coefficients of the macroblock, and (d) the variance of the four DC coefficients of the macroblock.

One choice for the energy function is the sum of the squares of the filtered pixel values. However, a non-linearity is introduced by the sum of squares approach. Another choice for the energy function is a counting function that counts the number of filtered pixels each having an absolute value above a preset threshold. This latter energy function is linear.

For video signals originating from a telecin converter[2], a large compression ratio can be realized by eliminating redundancy inherent in such video signals. In such video signals, a high likelihood exists that adjacent fields of such video signals are identical. To identify such redundancy, in this embodiment, a vertical [1, -1] filter (the instruction FILM), which is implemented by byte multiplexors 1541 and 1542 aligning the corresponding pixels values in the vertical direction is provided. MAC 158 computes an "energy" function of the filtered image. The pair of fields resulting in a low energy function is a candidate for field elimination.

In the present embodiment, a fast zero-lookahead circuit 1300, shown in Figure 13a, is provided for arithmetic unit 750. Zero-lookahead circuit detects a zero-result condition for an arithmetic operation, such as an "add" operation involving two operands. Circuit 1300 comprises two types of circuits, labelled 1301 ("generator circuit") and 1302 ("propagator circuit"), and schematic represented in Figure 13a by a square and a rectangle respectively.

In circuit 1300, there are 32 generator circuits and 31 propagator circuits. As shown in Figure 13b, each generator circuit comprises a NOR gate 1301a, an AND gate 1301b, and an exclusive-OR gate 1301c. Each of logic gates 1301a-1301c receives as input 1-bit operands "a" and "b". The operands a and b of these logic gates 1301a-1301c are corresponding bits from the input operands of a 2-operand operation in arithmetic unit 750.

The generator circuit 1301 each generates three signals P', Z+ and Z-, corresponding respectively to signals representing a "zero-propagator", a "small zero" and a "big zero".[3]These output signals P', Z+ and Z-are combined in a propagator circuit 1302 shown in Figure 13b. As shown in Figure 13b, propagator circuit 1302 provides signals P', Z+ and Z-. The signals from each propagator circuit of zero lookahead circuit 1300 are combined with corresponding signals from another propagator circuit in a binary tree of propagator circuits. As shown in Figure 13a, in the propagator circuit at the root of the binary tree of propagator circuits, indicated by reference numeral 1304, the signals Z+ and Z- of propagator circuit are input to an OR gate 1303 to generate the zero condition.

Compared to conventional zero-detection circuits, zero-lookahead circuit 1300 detects a zero result in a very small number of gate delays.

The present embodiment provides support for DCT and IDCT computation by "butterfly" instructions. The present embodiment implements the following equation:

[2] A telecin converter converts frames of a motion picture, which is played at 24 frames per second, into video signals, which are played at 30 frames a second and comprising in each frame odd and even fields. The conversion is achieved by duplicating movie frames into odd and even fields of the video signal according to the sequence 2:3:2:3.... However, since the video signals are often edited after the telecin conversion, redundancy cannot be eliminated merely eliminating duplicated frames according to the sequence.

[3] A "zero-propagator" indicates a zero condition caused by a carry from the next lower order bit. A "small zero" indicates a zero condition cause by the sum of two zero operands. A "big zero" indicates a zero condition resulting from at least one non-zero operand.

$$BFLY(a,b,c,p,d,m,t,sav) = \begin{array}{l}\{p=(a+b)/c;\\ c=((a-b)*\cos(m)-t/d;\\ acc=sav\}\end{array}$$

Quantization, during encoding, and dequantization, during decoding are also supported in ALU 150.

The Motion Estimator

Motion estimator unit 111 is a pipelined coprocessor for computing motion vectors during encoding. Figure 16a is a block diagram of the motion estimator 111. At any given time, the macroblocks of pixels to be coded are referred to as "current" macroblocks and the macroblocks of pixels relative to which the current macroblocks are to be coded is known as the "reference frame". The reference frame encompasses macroblocks which are within the range of allowable motion vectors and which are earlier or later in time than the current macroblocks.

As shown in Figure 16a, overall control for motion estimator 111 is provided by motion estimator control unit 1613. In addition, subpel filter 1606 is controlled by subpel control logic 1607, register file 1610 is controlled by register file control unit 1614, and matcher 1608 is controlled by matcher control unit 1609.

Read and write address generations for window memory 705, which is a 48 X 128-bit SRAM, are independently provided by read address generator 1602 and write address generator 1601. A test address generator 1604 is provided to for accessing window memory 705 for test purposes. Multiplexor 1603 is provided to enable a test access. Internally, as discussed in the following, window memory 705 is divided into two banks with an addressing mechanism provided to allow efficient retrieval of pairs of quad pels from a tile. In this embodiment, motion estimation is provided for both P- (predictive) frames and B-(bidirectional) frames, completed by either a 2-stage or a 3-stage motion estimation process, each stage using a different resolution. A subpel filter 1606, controlled by subpel filter control 1607, allows calculation of pixel values at half-pixel locations.

In the implementation shown in Figure 16a, matcher 1608, which comprises 16 difference units, computes a "partial score" for each of eight motion vector candidates. These partial scores for the motion vectors evaluated are accumulated in the accumulators 1610. When these motion vectors are evaluated with respect to all pixels in a macroblock, the least of these partial scores becomes the current completed score for the macroblock. This current completed score is then compared to the best motion vector computed for the current macroblock using other refrence frame macroblocks. If the current completed score is lower than the best completed score of the previous best motion vector, the current completed score becomes the best completed score and the current motion vector becomes the best motion vector. Interrupts to CPU 150 are generated by interrupt generator 1612 when matcher 1608 arrives at the current completed score when the requested search area is fully searched.

Figure 16b is a data and control flow diagram of motion estimator 111. As shown in Figure 16b, current macroblocks and macroblocks in the reference frame are fetched at the rate of 32 bits every 64 ns from external memory 103 and into SMEM 159. In turn, the current and reference macroblocks are fetched at the rate of 128 bits every 32 ns into window memory 705. Every 16 ns, two 32-bit words, each containing four pixels, are fetched from window memory 705 into the subpel filter and associated registers. The subpel filter provides every 16 ns a quad pel and a 3 X 3 pixel reference area for evaluation of sixteen absolute differences in matcher 1608. These absolute differences are used to evaluate the scores of the eight motion vectors. The best score are temporarily stored in a minimization register within comparator 1611. Comparator 1611 updates the best score in the minimization register, if necessary, every 16 ns. Control of the data flow is provided by control unit 1613.

Window memory 705, which is shown in Figure 16c, comprises an even bank 705a and an odd bank 705b, each bank being a 48 X 64-bit SRAM with an input port receiving output data from SMEM 159 over output busses 751a and 180b. The even and odd banks of window memory 705 output data onto 64-bit output port 1541a or 1541b, respectively. Registers 1557a and 1557b each receive 64-bit data from the respective one of even memory bank 705a and odd memory bank 705b. Registers 1557a and 1557b are clocked at a 30 Mhz clock. Multiplexors 1558 select from the contents of registers 1557a and 1557b a 64-bit word, as the output of window memory 705. Register 1559 receives this 64-bit word at a 60 Mhz clock rate.

Each 64-bit word in window memory 705 represents a "vertical" half-tile (i.e. a 2 X 4 pixel area). Window memory 705 stores both current macroblocks and reference macroblocks used in motion estimation. As shown below, matcher 1608 evaluates motion vectors by matching a 2 X 8 pixel area of a current

macroblock against a 4 X 12 pixel area of one or more reference macroblocks. In this embodiment, the 2 X 8 pixel area of a current macroblock are fetched as two vertically adjacent vertical half-tiles. Reference macroblocks, however, are fetched as "horizontal" half-tiles (i.e. 4 X 2 pixel reference areas). To support efficient fetching of 2 X 8 pixel areas of a marcoblock, vertically adjacent vertical half-tiles are stored in alternate banks of window memory 705, so as to take advantage of 2-bank access. When fetching of a horizontal half-tile of a reference macroblock, two vertical half-tiles are fetched. Thus, to take advantage of memory interleaving, these vertical half-tiles are preferably stored in alternate memory banks. Figure 16d shows an example of how the vertical half-tiles of a macroblock can be stored alternately in even ("E") and odd ("O") memory banks 705a and 705b. The arrangement shown in Figure 16d allows a 2 X 8 pixel areas of a current macroblock to be fetched by accessing alternatively odd memory bank 705b and even memory bank 705a. In addition, to fetch an upper or lower horizontal half-tile, even memory bank 705a and odd memory bank 705b are accessed together, and multiplexors 1558 are set to select, for output to register 1559 as a 64-bit output datum, a 32-bit halfword from register 1557a of even memroy bank 705a and a 32-bit halfword from register 1557b.

The present embodiment can be programmed to implement a hierarchical motion estimation algorithm. In this hierarchical motion estimation algorithm, the desired motion vector is estimated in a first stage using a lower resolution and the estimation is refined in one or more subsequent stages using higher resolutions. The present embodiment can be programmed to execute, for example, a 2-stage, a 3-stage, or other motion estimation algorithms. Regardless of the motion estimation algorithm employed, motion vectors for either the P (i.e. predictive) type or B (i.e. bidirectional) type frame can be computed.

A 2-stage motion estimation algorithm is illustrated in Figure 17. As shown in Figure 17, input video data is received and, if necessary, resampled and deinterlaced in steps 1701 and 1702 horizontally, vertically and temporally to a desired resolution, such as 352 X 240 X 60, or 352 X 240 X 30 (i.e. 352 pixels horizontally, 240 pixels vertically, and either 60 or 30 frames per second). The input video data is stored as current macroblocks in external memory 103 temporarily for motion estimation. In step 1703, the current macroblocks are decimated to provide a lower resolution. For example, a 16 X 16 full resolution macroblock can be decimated to a 8 X 8 macroblock covering the same spatial area of the image (quarter-resolution).

Only luminance data are used in motion estimations. In the first stage of the 2-stage motion estimation, represented by step 1704, the low resolution current macroblock is compared to a correspondingly decimated reference frame to obtain a first estimate of the motion vector. In the present embodiment, the motion vector positions evaluated in this first stage can range, in full resolution units of pixels, (a) for P frames, ± 46 horizontally and ± 22 vertically; and (b) for B frames, ± 30 horizontally and ± 14 vertically. This approach is found to be suitable for P frames within three frames of each other.

The motion vector estimated in the first stage is then refined in step 1705 by searching over a (3/2, 3/2) area around the motion vector evaluated in Stage 1. The second stage motion vector is then passed to VLC 109 for encoding in a variable-length code.

The reference frame macroblocks (P or B frames) are resampled in step 1706 to half-pel positions. Half-pel positions are called for in the MPEG standard. Step 1707 combines, in a B frame, the forward and backward reference macroblocks. The current macroblock is then subtracted from the corresponding pixels in the resampled reference frame macroblocks in step 1708 to yield an error macroblock for DCT in step 1709. Quantizations of the DCT coefficients are achieved in step 1710. Since quantization in the present embodiment is adaptive, the quantization step-sizes and constants are also stored alongside the motion vector and the error macroblock in the variable-length code stream. The quantized coefficients are both forwarded to VLC 109 for variable-length code encoding, and also fed back to reconstruct reference macroblocks to be used in subsequent motion estimation. These reconstructed reference macroblocks are reconstructed by dequantization (step 1712), inverse discrete cosine transform (step 1713), and added back to the current macroblock.

Blocks can be encoded as intra, forward, backward or average. The decision to choose the encoding mode is achieved by selecting the mode which yields the smallest mean square error, as computed by summing the values of entries in the resulting the error macroblock. According to the relative preference for the encoding mode, a different bias is added to each mean square error computed. For example, if average is determined to be the preferred encoding mode for a given application, a larger bias is given the corresponding mean square error. A particularly attractive encoding outcome is the zero-delta outcome. In a zero-delta outcome, the motion vector for the current block is the same as the motion vector of the previous block. A zero-delta outcome is attractive because it can be represented by a 2-bit differential motion vector. To enhance the possibility of a zero-delta outcome in each encoding mode, in addition to the first bias added to provide a preference for the encoding mode, a different second bias value is added to the mean square error of the encoding mode. In general, the first and second bias for each encoding mode are

determined empirically in each application.

Figures 18a shows a decimated macroblock and the reference frame macroblocks within the range of the first stage motion vector under a B frame encoding mode. In Figure 18a, a decimated macroblock (1/4 resolution) 1801 is shown within the range 1802 of a motion vector having an origin at the upper left corner of macroblock 1801. Figure 18b shows a decimated macroblock and the reference frame macroblock within the range of the first stage motion vector under a P frame encoding mode. In Figure 18b, the decimated macroblock 1805 is shown within the range 1806 of a motion vector having an origin at the upper left corner of macroblock 1805.

In the second stage of motion estimation, full resolution is used in both P frame and B frame encoding. The range of the motion vector computed in the second stage of the two-stage motion estimation is 1.5 pels. Figure 18c shows a full resolution macroblock and the range 1811 of the motion vector of this second stage of motion estimation of both the P and B frames. To achieve efficient use of window memory 705, in a B frame motion estimation, a 4 X 1 region ("strip") of current macroblocks is evaluated with respect to a 2 X 3 macroblock region of the reference frame. The locations 1820 and 1821 of the current and the reference regions, respectively, are shown in Figure 18d. To minimize the number of times data is loaded from external memory 103, the evaluation of motion vectors covering the reference macroblocks and the current macroblocks in window memory 705 are completed before a new strip of current macroblocks and reference memory are loaded. In the configuration shown in Figure 18d, a new current macroblock (macroblock 1825) and a new slice (1 X 3) of reference macroblocks (i.e. the 1 X 3 macroblocks indicated in dotted lines by reference numeral 1822) are brought in when evaluation of the leftmost current macroblock (1820a) of 4 X 1 macroblock strip 1820 is complete. The loading of the new current macroblock and the new reference frame macroblocks is referred to as a "context switch." At this context switch, the leftmost current macroblock has completed its evaluation over the entire range of a motion vector, the remaining current macroblocks, from left to right, have completed effectively 3/4, 1/2 and 1/4 of the evaluation over the entire range of a motion vector.

In a first stage P frame motion estimation, since the search range is larger than that of the corresponding B frame motion estimation, a 2 X 4 reference macroblock region and a 6 X 1 strip of current macroblocks form the context for the motion estimation. Figure 18e show a 6 X 1 strip 1830 of current macroblocks and a 2 X 4 region 1831 of the reference macroblocks forming the context for a P frame motion estimation. In this embodiment, for a P frame estimation, only one-half of the 6 X 1 region of current macroblocks, i.e. a 3 X 1 region of current macroblocks, is stored in window memory 705. Thus, in a P frame estimation, the 2 X 4 region, e.g. region 1831, is first evaluated against the left half of the 6 X 1 region (e.g. region 1830), and then evaluated against the right half of the 6 X 1 region before a new current macroblock and a new 1 X 4 reference frame region are brought into window memory 705.

For the second stage motion estimation, a 4 X 4 tile region (i.e. 16 X 16 pixels), forming a full resolution current macroblock, and a 5 X 5 tile region of the reference macroblocks covering the range of the second stage motion estimation are stored in window memory 705. The reference macroblocks are filtered in the subpel filter 1606 to provide the pixel values at half-pel locations. Figure 18f shows both a 4 X 4 tile current macroblock 1840 and a 5 X 5 tile reference region 1841.

As mentioned above, the present embodiment also performs 3-stage motion estimation. The first stage for a P or a B frame motion estimation under a 3-stage motion estimation is identical to the first stage of a B frame motion estimation under a 2-stage motion estimation. In the present embodiment, the range of the motion vectors for a first stage motion estimation (both P and B frames) is, in full resolution, ± 124 in the horizontal direction, and ± 60 in the vertical direction.

The second stage of the 3-stage motion estimation, however, is performed using half-resolution current and reference macroblocks. These half-resolution macroblocks are achieved by a 2:1 vertical decimation of the full resolution macroblocks. In the present embodiment, the range of motion vectors for this second stage motion estimation is ± 6 in the horizontal direction and ± 6 in the vertical direction. During the second stage of motion estimation, a half-resolution current macroblock and a 2 X 2 region of half-resolution macroblocks are stored in window memory 705.

The third stage of motion estimation in the 3-stage motion estimation is identical to the second stage of a 2-stage motion estimation.

In the present embodiment, matcher 1608 matches a "slice" -- a 2 X 8 pixels configuration -- of current pixels (luma) against a 3 X 11 pixel reference area to evaluate eight candidate motion vectors for the slice's macroblock. The 3 X 11 pixel reference area is obtained by resampling a 4 X 12 pixel reference area horizontally and vertically using subpel filter 1606. As explained below, the 2 X 8 slice is further broken down into four 2 X 2 pixel areas, each of which is matched, in 2 phases, against two 3 X 3 pixel reference areas within the 3 X 11 pixel reference area. The eight motion vectors evaluated is referred to as a "patch"

of motion vectors. The patch of eight vectors comprises the motion vectors (0,0), (0,1), (0,2), (0,3), (1,0), (1,1), (1,2) and (1,3). In this embodiment, eight bytes of data are fetched at a time from window memory 705 to register file 1610, which forms a pipeline for providing data to subpel filter 1606 and matcher 1608. The control of motion estimation is provided by a state counter. Figure 18g shows the fields of the state counter 1890 for motion estimation in this embodiment. As shown in Figure 18g, the fields of state counter 1890 are (a) 1-bit flag Fx indicating whether horizontal filtering of the reference pixels is required, (b) a 1-bit flag Fy indicating whether vertical filtering of the reference pixels is required, (c) a 3-bit counter CURX indicating which of the current macroblocks in the 4X1 or 6X1 strip of current marcoblocks is being evaluated, (d) a 2-bit counter PatchX indicating the horizontal position of the patch of motion vectors being evaluated, e) a 3-bit counter PatchY indicating the vertical position of the patch of motion vectors being evaluated, (f) a 4-bit counter SLICE indicating which one of the sixteen slices of a macroblock is being evaluated, and (g) a 3-bit counter PEL indicating one of the eight phases of matcher 1608.

The fields FY, FX, CURX, PatchX, and PatchY are programmable. The fields FY and FX enables filtering subpel filter 1606 in the indicated direction. Each of the counters CURX, PatchX, PatchY, SLICE, and PEL counts from an initial value (INIT) to a maximum value (WRAP) before "wrapping around" to the INIT value again. When a WRAP value is reached, a "carry" is generated to the next higher counter, i.e. the next higher counter is incremented. For example, when PEL reaches its WRAP value, SLICE is incremented. When CURX reaches its WRAP value, a new current macroblock and new reference macroblocks are brought into window memory 705.

The range of motion vectors to be searched can be restricted by specifying four "search parameters" Mx_{min},My_{min}, Mx_{max}, and My_{max}. In addition, the frame boundary, i.e. the boundary of the image defined by the reference macroblocks, restricts the range of searchable motion vectors. Both the search parameters and the frame boundary affect the INIT and WRAP values of state counter 1890. In this embodiment, the search parameters are user programmable to trade-off search area achievable to encoding performance.

In the present embodiment, when some but not all motion vectors are outside of the frame boundary, the scores of the patch are still evaluated by matcher 1608. However, the scores of these invalid motion vectors are not used by comparator 1611 to evaluate the best scores for the macroblock. Figure 18h shows the four possible ways a patch can cross a reference frame boundary. In Figure 18h, the dark color pel or subpel positions indicate the positions of valid motion vectors and the light color pel or subpel positions indicate the positions of invalid motion vectors. If a patch lies entirely outside the reference frame, the patch is not evaluated. The process of invalidating scores or skipping patches is referred to as "clipping." Figure 18i shows the twelve possible ways the reference frame boundary can intersect the reference and current macroblocks in window memory 705 under the first stage motion estimation for B-frames. For example, in Figure 18i, configuration 8 corresponds to the situation when the upper horizontal boundary of the reference frame touches the top rows of pixels for macroblocks a and b, and the right boundary of the reference frame is between reference frame macroblocks a and b. Figure 18j shows, for each of the 12 cases shown in Figure 18i, the INIT and WRAP values for each of the fields CURX, PatchX, and PatchY in state counter 1890. The valid values for fields SLICE and PEL are 0-3 and 0-7 respectively. Figure 18k shows the twenty possible ways a reference frame boundary can intersect the current and reference macroblocks in window memory 705 under the first stage of a P frame 2-stage motion estimation. Figure 18l shows, for each of the twenty cases shown in Figure 18k, the corresponding INIT and WRAP values for each of the fields of state counter 1890. Likewise, Figures 18m-1 and 18m-2 show the clipping of motion vectors with respect to the reference frame boundary for either the second stage of a 2-stage motion estimation, or the third stage of a 3-stage motion estimation. Figure 18n provides the INIT and WRAP values for state counter 1890 corresponding to the reference frame boundary clipping shown in Figures 18m-1 and 18m-2.

The basic algorithm of matcher 1608 is illustrated by Figures 19a-19c. Matcher 1608 receives a 2 X 8 slice of current pixels and a 4 X 12 area of reference pixels over eight clock cycles. As illustrated by Figure 19b, the area of reference pixels are provided to matcher 1608 as half-tiles r0, r1, r2, r3, r4 and r5. Subpel filter 1606 can be programmed to sub-sample the reference area using a two-tap 1-1 filter in either the vertical or the horizontal direction, or both (i.e. the neighboring pixels are averaged vertically, as well as horizontally). The resulting 3 X 11 pixel filtered reference area is provided as five 3 X 3 pixel overlapping reference areas. As shown in Figure 19a, each 3 X 3 reference area is offset from each of its neighboring 3 X 3 reference area by a distance of two pixels. Alternatively, the 1-1 filter in either direction can be turned off. When the 1-1 filter in either direction is turned off, the 3 X 11 pixel reference area is obtained by discarding a pixel in the direction in which averaging is skipped.

In matcher 1608, the 2 X 8 slice of current pixels is divided into four 2 X 2 pixel areas C1, C1', C2 and C2'. Each of the four 2 X 2 areas of current pixels is scored against one or two of the five 3 X 3 reference areas. For each 2 X 2 pixel current area and 3 X 3 pixel reference area matched, four motion vectors are

evaluated. These motion vectors are indicated in Figure 19b by the "X" markings in the 3 X 3 reference area. These motion vectors have an origin in the 2 X 2 current area indicated by "X" marking.

Referring back to Figure 19a, in cycle 0, 2 X 2 pixel area 1901 is matched in matcher 1608 against 3 X 3 reference area 1921 to evaluate motion vectors (0,0), (1,0), (0,1) and (1,1). In cycle 1, the 3 X 3 reference area 1921 is replaced by reference area 1922 and the motion vectors (0,2), (1,2), (0,3) and (1,3) are evaluated. In cycle 2 and subsequent even cycles 4 and 6, the 2 X 2 current pixel area is successively replaced by 2 X 2 current pixel areas 1902, 1903 and 1904. In each of the even cycles, motion vectors (0,0), (1,0), (0,1) and (1,1) are evaluated against 3 X 3 reference pixel areas 1922, 1923 and 1924. In cycle 3 and subsequent odd cycles 5 and 7, the 3 X 3 reference pixel area is successively replaced by 3 X 3 reference pixel areas 1922, 1923 and 1924. In each of the odd cycles, the motion vectors (0,2), (1,2), (0,3) and (1,3) are evaluated.

Matcher 1608 evaluates the four motion vectors in each cycle by computing sixteen absolute differences. The computation of these sixteen absolute differences is illustrated in Figure 19c. Matcher 1608 comprises four rows of four absolute difference circuits. To illustrate the motion vector evaluation process, the 2 X 2 current pixels and the 3 X 3 reference pixels are labelled (0-3) and (0-5 and a-c) respectively. As shown in Figure 19c, the four rows of matcher 1608 computes the four absolute differences between the pixels in (a) current quad pel 0 and reference quad pel 0; (b) current quad pel 0 and reference quad pel 1; (c) current quad pel 0 and reference quad pel 2; and (d) current quad pel 0 and reference quad pel 3, respectively. At the end of each cycle, the four absolute differences of each row are summed to provide the "score" for a motion vector. The sums of absolute differences in the four rows of difference circuits in matcher 1608 represent the scores of the motion vectors (0,0), (1,0), (0,1) and (1,1) during even cycles, and the scores of the motion vectors (0,2), (1,2), (0,3) and (1,3) during odd cycles. The four evaluations of each motion vector are summed over the macroblock to provide the final score for the motion vector. The motion vector with the minimum score for the macroblock is selected as the motion vector for the macroblock.

As discussed above, 64 bits of pixel data are fetched from window memory 705. Pipeline registers in subpel filter 1606 are used in motion estimator 111. The pipeline is shown in Figure 19d. In Figure 19d, the data flow through the input of motion estimator 111, register 1930, register 1931, register 1932, and register 1935 are shown on the right hand side as time sequences of half-pixel data. For example, as shown in Figure 19d, the sequence in which the 2 X 8 slice of current pixels and the 4 X 12 reference frame pixels arriving at the motion estimator unit 111 is r0, r1, r2, c1, c2, r3, r4 and r5. (The 2 X 2 pixel areas c1 and c1', c2 and c2' are fetched together).

At every clock cycle, a 64-bit datum is fetched from window memory 705. Quad pel c1 is extracted from half-tile c1 and provided to the register 1937. In this embodiment, to provide the reference half-tiles r0 and r3 to matcher 1606 in time, reference areas r0 and r3 bypass register 1930 and join the pipeline at register 1931. Reference area r0 of the next reference area used for evaluation of the next patch of motion vectors is latched into register 1931 ahead of reference area r5 used for evaluation of the current patch of motion vectors. Also, reference area r3 for evaluation of the current patch of motion vectors is latched into register 1931 prior to quad pel C2. Thus, a reordering of the reference half-tiles is accomplished at register 1931.

The filtered reference areas r0-r5 pass through register 1932 for vertical filtering and pass through register 1933 for horizontal filtering. Quad pel c1' and quad pel c2 are extracted from the output terminals of register 1931 to be provided to register 1937 at the second and the fourth cycles of the evaluation of the slice. Quad pel c2' passes through register 1935 and 1936 to be provided to register 1937 at the fifth cycle of the evaluation of the slice. Reference area r0 is reordered to follow the reference area r5 in the evaluation of the previous patch. The reference areas r0-r5 are latched in order into registers 1933 and 1938 for matcher 1606.

VLC 109 and VLD 110

VLC 109 encodes 8 X 8 blocks of quantized AC coefficients into variable length codes with zero-runlength and non-zero AC level information. These variable length codes are packed into 16-bit halfwords and written into VLC FIFO 703, which is a 32-bit wide 16-deep FIFO Memory. Once VLC FIFO 703 is 50% full, an interrupt is generated to memory controller 104, which transfers these variable length codes from VLC FIFO 703 under DMA mode. Each such DMA transfer transfers eight 32-bit words.

Figures 20a and 20b form a block diagram of VLC 109. As shown in Figure 20a, Zmem 704 receives from processor bus 108a 36-bit words. Zmem 704, includes two FIFO memories, which are implemented as a 16 X 36 bits dual port SRAM and a 64 X 9 bits dual port SRAM, for DCT and IDCT coefficients during encoding and decoding respectively. The two ports of Zmem 704 are: (a) a 36-bit port, which receives data

words from processor bus 108a during encoding, and (b) a 9-bit read port, which provides data to a zero-packer circuit 2010 during encoding.

Zmem controller 2001 generates the read and write addresses ("zra" and "zwa") and the control signals of Zmem 704. The Zmem write enable signal "zwen" is generated by Zmem controller 2001 when a write address "zwa" is provided during a write access. Within Zmem controller 2001, a binary decoder and a "zig-zag" order decoder are provided respectively for accessing the 36-bit port and the 9-bit port respectively. During encoding, the binary decoder accesses the Zigzag memory 704 in binary order to allow the 8 X 8 blocks of DCT coefficients to be received into Zmem 704 as a series of quad pels. For zero packing operations during encoding, the zig-zag order decoder accesses Zig-zag memory 704 in zig-zag order. The start of a 8 X 8 block is signalled by Zcontroller 2001 receiving the "zzrunen" signal and completes when the "zzdone" signal is received. When VLC FIFO 703 is full, indicated by signal "ffull" or, for any reason, the "haltn" signal is asserted by the host computer, the VLC pipeline is stalled by Zmem controller 2001 asserting the control signal "zstall".

Zero packer circuit 2010 comprises programmable adaptive threshold circuit 2006 which sets an AC coefficient to zero when (i) the AC coefficient is less than a user programmable threshold and (ii) the immediately preceding and the immediately following AC coefficients are zero. When a negative or a negative non-intra AC coefficient is received in zero packer circuit 2010, incrementer 2004 increments the AC coefficient by 1. This increment step is provided to complete a previous quantization step. The AC coefficients immediately preceding and immediate following the current AC coefficient received at adaptive threshold circuit 2006 are held at registers 2005 and 2007. If the current AC coefficient is less than a predetermined threshold stored in the VLC control register (not shown), and the preceding and following AC coefficients are zero, the current AC coefficient is set to zero. By setting the current AC coefficient to zero when the immediately preceding and the immediately following AC coefficients are zero, a longer zero run is created, at the expense of one sub-threshold non-zero coefficient. In the present embodiment, this adaptive threshold can be set to any value between 0-3. In addition, to preserve the values of lower frequency AC coefficients, the user can also enable adaptive threshold filtering for AC coefficients beginning at the 5th or the 14th AC coefficient of the 8 X 8 block.

Zero packer 2009 provides as output data a pair of values, representing the length of a run of zeroes, and a non-zero AC coefficient. The output data of zero packer 2009 are provided to a read-only memory (rom) address generator 2021 (Figure 20b), which generates addresses for looking up MPEG variable length codes in rom 2022. In this embodiment, not all combinations of runlength-AC value are mapped into variable length codes, the unmapped combinations are provided as 20-bit or 28-bit fixed length "escape" values by fixed length code generator 2025. The present embodiment can generate non-MPEG fixed length codes using non-MPEG code circuit 2024. Framing information in the variable length code stream are provided by packing circuit 2025.

MPEG rom 2022 generates a 6-bit non-zero code and a 4-bit length code. The final variable length code is provided by barrel shifter 2041, which zero-stuffs the 6-bit non-zero code according to the value of the 4-bit length code. Barrel shifter control logic 2026 controls both barrel shifter 2041 and barrel shifter 2029, code generator 2025, non-MPEG code circuit 2024 and packing circuit 2026.

The variable length codes, whether from MPEG rom 2022, fixed length code generator 2025, non-MPEG code circuit 2024 or packing circuit 2025, are shifted by barrel shifter 2029 into a 16-bit halfword, until all bits in the halfword are used. The number of bits used in the halfword in Barrel shifter 2029 is maintained by adder 2027. 16-bit outputs of barrel shifter 2029 are written into VLC FIFO 703 under the control of FIFO controller 2035. VLC FIFO 703, which is implemented as a 16 X 32-bit FIFO, receives a bit stream of 16-bit halfwords and is read by controller 104 over processor bus 108a as 32-bit words. FIFO controller 2035 sends a DMA request to memory controller 104 by asserting signal VC_req when VLC FIFO 703 2037 contains 8 or more 32-bit words. A stall condition (signal "ffull" asserted) for VLC 109 is generated when address 'a' (hexadecimal) is exceeded. The stall condition prevents loss of data due to an overflow of VLC FIFO 703.

Decoding by VLD 110 can be achieve by a decoder such as discussed in the MPEG decoder of the aforementioned Copending Application.

Conclusion

The present embodiment provides a high performance video signal encoder/decoder on a single integrated circuit. However, the principles, algorithms and architecture described above are applicable to other implementations, such as a multi-chip implementation, or a system level implementation. Further, although the present invention is illustrated by an implementation under the MPEG standard, the present

invention may be used for encoding video signals under other video encoding standards.

The above detailed description is provided to illustrate the specific embodiment of the present invention and is not intended to be limiting. Many variations and modifications are possible within the scope of the present invention. The present invention is set forth in the following claims.

Claims

1. A structure for encoding digitized video signals representing a series of frames of images, said digitized video signals being stored in an external memory system, said structure comprising:
   a first and a second video ports, each video port being configurable to be either an input port or an output port for video signals;
   a host bus interface circuit for interfacing with an external host computer;
   a scratch-pad memory for storing a portion of said series of frames of images;
   a processor for arithmetic and logic operations, wherein said processor computing coefficients of a discrete cosine transform of said portion of said series of frames of images, and for applying a quantization step for said coefficients to obtained quantized coefficients under a lossy compression algorithm;
   a motion estimation unit for matching objects in motion between said frames of images, said motion estimation unit providing as data output motion vectors representing said motion of said objects in motion between said frames of images;
   a variable-length coding unit for applying an entropy coding scheme on said quantized coefficients and said motion vectors to represent said video signals;
   a global bus accessible by said first and second video port, said host bus interface, said scratch-pad memory, said processor, said motion estimation unit, and said variable-length coding unit, said global bus providing data transfer among said first and second video port, said host bus interface, said scratch-pad memory, said processor, said motion estimation unit, and said variable-length coding unit;
   a processor bus having a higher bandwidth than said global bus for providing data transfer among said processor, said scratch-pad memory, and said variable-length coding unit; and
   a memory controller for (a) controlling data transfers between said external memory and said structure, and (b) for controlling the uses of said global bus and said processor bus.

2. A structure as in Claim 1, wherein said processor comprises:
   an instruction memory for storing instructions executable by said processor;
   a register file including a predetermined number of registers for storing operands;
   an arithmetic and logic unit for providing arithmetic and logic operations for operands in said register file; and
   a multiplication unit for performing multiplication operations among said operands and a result of said arithmetic and logic operations.

3. A structure as in Claim 1, wherein said motion estimation unit comprises:
   a window memory for storing a second portion of said series of frames of images, said second portion being a subset of said portion of said series of frames of images stored in said scratch-pad memory, said second portion of said series of frames of images including video data from a current frame and video data from a reference frame; and
   a matcher for matching said video data from said current frame and said video data from said reference frame to evaluate a predetermined number of motion vectors.

4. A structure as in Claim 1, wherein said first video port comprises a decimation filter for reducing the resolution of said video signals.

5. A system comprising a first and a second structures, each structure being a structure as recited in Claim 1, wherein said first video port of said first structure and said first video port of said second structure are connected to receive said video signals, and said second video port of said first structure and said second video port of said second structure are connected to pass said video data between said first structure and said second structure.

6. An interface for receiving digitized video signals, said digitized signals including samples of a luminance component and first and second chrominance components provided to said interface in pixel

interleaved order, said interface comprising:

a memory divided in groups of regions, each group of regions having a first region, a second region and a third region for storing said samples of said luminance component and said first and second chrominance components respectively;

a counter for maintaining a count of said digitized video signals, said counter being incremented as each sample arrives at said interface; and

address generator for generating an address for storing in said memory each of said samples of digitized video samples in accordance with said count, such that a sample of said luminance component is stored in said first region, a sample of said first chrominance component is stored in said second region and a sample of said second chrominance component is stored in said third region.

7. A synchronizer circuit for synchronizing a first and a second clock signals, comprising:

first means for detecting a transition, said first means detects a transition of said second clock signal between a first and a second transitions of said first clock signal, said first and second transitions of said first clock signal being successive transitions;

second means for detecting a transition, said second means detecting a transition of said second clock signal between said second transition and a third transition of said first clock signal, said second and third transitions of said first clock signal being successive transitions; and

means for outputting a detected transition of said first and second means at a fourth transition of said first clock signal, said fourth transition being a transition of said first clock signal subsequent to said third transition of said first clock signal.

8. A memory structure, comprising:

a plurality of memory cells organized as an s X s matrix of addressable units; and

means for generating any one of 2s addresses for accessing said addressable units, wherein s of said 2s addresses access s rows of said matrix, and the remaining s addresses access s columns of said matrix.

9. A central processing unit, comprising:

a data memory having a plurality of data words, each data word having a word width of n*m bits, where n and m are integers;

a first set of n registers for storing n data words, each data word having a width of m bits, said n registers structured such that (i) for input purpose, said first set of n registers receives an n*m bit data word from said data memory simultaneously as a single n*m-bit register, and (ii) for output purpose, each of said n registers is addressed independently;

an arithmetic and logic unit receiving a plurality of m-bit operands from said first set of n registers and providing as a result of an operation an m-bit result; and

a second set of n registers for storing n data words, each data word having a width of m bits, said second set of n registers structured such that (i) for input purpose, each of said n registers is addressed independently for receiving said m-bit result from an operation of said arithmetic unit; and (ii) for output purpose, said second set of n registers output an n*m bit data word to said data memory simultaneously as a single n*m-bit register.

10. A memory controller for a processor having a plurality of functional units, comprising:

a first interface adapted for controlling access to an external memory system;

a second interface adapted for controlling a first internal bus, said first internal bus being m-bit wide, m being an integer;

a third interface adapted for controlling a second internal bus, said second internal bus being n*m-bit wide, n being an integer;

an arbitration unit for receiving data transfer requests from said functional units and for granting use of said first and second internal busses to a selected one of said functional units; and

a direct memory access unit for controlling, over said first, second and third interfaces, data transfer among said selected functional unit, said first and second internal busses and said data memory.

11. A method for accessing pixels of an image in scan-line order, comprising the steps of:

dividing said image into tiles, each tile being four adjacent quad pels in a 2 X 2 configuration, each quad pel being four pixels in a 2 X 2 configuration;

providing a memory including a plurality of data words, wherein each data word of said memory being formed by two independently addressable halfwords, and each of said halfword having the capacity of storing two pixels of a quad pel;

for each tile, storing said tile in said memory, such that (i) each data word in said memory contains video data corresponding to a quad pel of said image, each pair of horizontally adjacent pixels of said quad pel being stored in the same halfword; and

accessing said memory to retrieve a scan-line element of four pixels by providing first and second addresses to access each of said independently addressable halfwords.

12. A method for storing pixel data for scan-line access, said scan-line access provided for retrieving a "scan line" element, being four pixels in a scan line of a video image, comprising the steps of:

providing a memory having odd and even memory banks, and in which each memory word of said odd and even memory banks comprises independently addressable upper and lower halfwords;

storing (i) in an even scan line, the left half of a scan line element in a lower halfword, and the right half of said scan line element in an upper halfword; and (ii) in an odd scan line, the left half of a scan line element in an upper halfword and the right half of a scan line element in a lower halfword; and

switching, every two scan lines, between storing scan line elements in the odd memory bank to storing scan line elements in the even memory bank.

13. A memory structure comprising:

a memory divided into a first half and a second half for providing a 2m-bit output datum, said 2m-bit output datum being formed by concatenating a first datum and a second m-bit datum, said first m-bit datum being provided from said first half of said memory by activating, in response to a first address, one of a first set of word lines, and said second m-bit datum being provided from said second half of said memory by activating, in response to a second address, one of a second set of word line; and

an address generator for generating said first and second address, said first and second address being constrained to be identical except for one bit.

14. A structure comprising:

an arithmetic and logic unit receiving first and second operands, each operand including a predetermined number of data elements, said arithmetic logic unit performing simultaneously arithmetic and logic operations between data elements of said first operand and data elements of said second operand, each of said operation involving one data element of said first operand and a corresponding data element of said second operand;

a first set of multiplexor for rearranging, prior to providing said first operand to said arithmetic and logic unit, the order of said data elements in said first operand; and

a second set of multiplexor for rearranging, prior to providing said second operand to said arithmetic and logic unit, the order of said data elements in said second operand.

15. A non-linear filter comprising:

means for setting a first threshold value T_1;

means for setting a second threshold value T_2;

means, receiving first and second operands x and y, for providing an absolute difference between x and y;

means, receiving said absolute difference and said first and second threshold values, for providing a weighting factor a equal to (i) when said when said absolute difference is less than T_1, a predetermined weight less than 1.0, (ii) when said absolute difference is between T_1 and T_2, a value between said predetermined weight and 1.0, said value being proportional to the said absolute difference, and (iii) when said absolute difference is greater than T_2, 1.0; and

means for providing a filter output, said filter output having the value x + a(y-x).

16. A method for deinterlacing a digitized video signal, said video signal comprising pixels from a first field and a second field of an image, said method comprising the steps of:

for each pixel x in said first field of said image: (i) identifying the corresponding pixel y in said second field of said image;

(ii) computing an absolute difference between x and y;

(iii) determining a weight a equalling (a) 0.5, when said absolute difference is less than a first

threshold value T_1, (b) 1.0, when said absolute difference is greater than a second threshold value T_2, and (c) a value proportional to said absolute difference; and

(iv) providing as a pixel of a deinterlaced image a pixel z having the value x + a(y-x).

17. A method for providing a temporal noise filter for a video signal, said video signal comprising pixels of successive frames of images displayable on a screen, said method comprising the steps of:

for position x in a screen, receiving a stream of pixel values x_0, x_1, ..., x_T, corresponding to values of the pixel at said position x at time points 0, 1, ..., T, wherein said time points correspond to arrivals of said successive frames of images; and

providing as an initial filter output value of said temporal noise filter y_0 the value x_0;

thereafter, for each time point t:

(i) computing an absolute difference between y_{t-1}, being the filter output value of said temporal noise filter at time point t-1, and x_t, being the current value of pixel x at said time point t;

(ii) determining a weight a equalling (a) 0.5, when said absolute difference is less than a first threshold value T_1, (b) 1.0, when said absolute difference is greater than a second threshold value T_2, and (c) a value proportional to said absolute difference; and

(iii) providing as filter output value of temporal noise filter a value y_t having the value $x_t + a(y_{t-1} - x_{t-1})$.

18. A method for scene analysis as a step in applying adaptive control technique in an image processing method, said image including a plurality of macroblocks, each macroblock a plurality of quad pels, being 2 X 2 configurations of pixels, said scene analysis method comprising the steps of:

for each quad pel in each macroblock:

(i) computing simultaneously first and second absolute differences, said first absolute difference being an absolute difference between a first pixel within said quad pel and a second pixel within said quad pel, said second absolute difference being an absolute difference between said second pixel and a third pixel of said quad pel; and

(ii) accumulating said first and second absolute differences in first and second accumulated sums; and

applying said adaptive control technique using said first and second accumulated sums as activity parameters.

19. A method for eliminating redundant fields in an video signal to improve a data compression ratio, each field comprises a plurality of quad pels, each quad pel being a configuration of 2 X 2 pixels, said method comprising:

for each quad pel in a first field:

(i) computing a first, a second, a third and a fourth differences between pixels in said quad pel and corresponding pixels of a corresponding quad pel in a second field; and

(ii) providing a count equal to the number of said first, second, third and fourth differences exceeding in magnitude a predetermined threshold value;

accumulating said count over all quad pels in said first field; and

eliminating said second field when said accumulated count exceeds a second predetermined threshold value.

20. A zero-lookahead circuit, comprising:

a plurality of zero generator circuits, each zero generator circuit receiving as input 1-bit signals a and b, and providing as output signals P, Z+ and Z- representing, respectively, whether the values of said signals a and b are not the same, the values of said signals a and b are equal to '1', and the values of said signals a and b are equal to '0'; and

a plurality of zero propagator circuits, each of said propagator circuits receiving as input signals (i) P_1, $Z+_1$, and $Z-_1$, being a first of said P, Z and Z- signals, and (ii) P_2, $Z+_2$, and $Z-_2$, being a second set and of said P, Z+ and Z- signals, and providing as output signals a third set of P, Z and Z- signals in accordance with the logic equations:

$P = P_1$ and P_2;

$Z- = Z-_1$ and $Z-_2$;

and $Z+ = (Z+_1$ and $P_2)$ or $(Z+_2$ and $Z-_1)$;

wherein said plurality of zero propagator circuits are connected in a tree configuration, having a leaf level receiving inputs from said plurality of zero generator circuits; and

an OR gate connected to the zero propagator circuit at the root of said tree configuration of zero propagating circuits, said OR gate receiving as input signals said Z+ and Z-signal providing output signal Z, representing whether a zero is detected.

21. A structure for performing motion estimation in the compression of video data, said video data comprising macroblocks of pixels in a current frame and macroblocks of pixels in a reference frame, said structure comprising:

a memory for storing said macroblocks of said current frame and said macroblocks of said reference frame;

a filter receiving a first group of pixels from said memory for resampling said first group of pixels, said first group of pixels being pixels from said macroblocks of said reference frame; and

a matcher receiving said resampled first group of pixels and a second group of pixels, said matcher matching said second group of pixels to said first group of pixels, for deriving a set of scores each corresponding to one of a predetermined group of motion vectors, said second group of pixels being pixels from a macroblock of a current frame and each of said scores being a measure of the differences between said second group of pixels and said first group of pixels under a corresponding motion vector within said predetermined group; and

means receiving said set of scores for selecting, among said predetermined group of motion vectors, a motion vector for said macroblock of said current frame.

22. A method for performing motion estimation for a video signal, said video signal comprising a first group of pixels from a current frame and a second group of pixels in a reference frame, said method comprising:

resampling said first and second groups of pixels to obtain a third group of pixels and a fourth group of pixels, said third and fourth groups of pixels being representations of said video signal at a first reduced resolution;

performing a first reduced resolution motion estimation based on a said third and fourth groups of pixels to obtain a first motion vector;

performing a second motion estimation using said first group of pixels, translated by said first motion vector, and a subset of said second group of pixels to obtain an incremental motion vector, said subset of said second group of pixels being pixels within a predetermined distance of the target position of said first motion vector; and

providing as output a motion vector equalling the sum of said first motion vector and said incremental motion vector.

23. A structure for encoding by motion vectors a current frame of video data using a reference frame of video data, each of said current and reference frames being divided into rows and columns of macroblocks, said macroblocks of said current frames being designated "current macroblocks" and said macroblocks of said reference frame being designated "reference macroblocks", each marcoblock representing an area of pixels in the corresponding frame, said structure comprising:

a memory circuit for storing (a) a plurality of adjacent current macroblocks from a row j of current macroblocks, said plurality of said adjacent current macroblocks being designated $C_{j,p}$, $C_{j,p+1}$, ..., $C_{j,p+n-1}$ in the order along one direction of said row of macroblocks; and (b) a plurality of adjacent reference macroblocks from a first column i of reference macroblocks, said plurality of reference macroblocks being designated $R_{q,i}$, $R_{q+1,i}$, ..., $R_{q+m-1,i}$, said plurality of adjacent reference macroblocks being reference macroblocks within the range of said motion vectors, each of said current macroblocks being substantially equidistance from said $R_{q,i}$ and $Rq+_{m-1,i}$ reference macroblocks;

means, evaluating each of said plurality of adjacent current macroblocks against each of said plurality of adjacent reference macroblocks under said motion vectors, for selecting a motion vector best representing the best match between each of said current macroblock and a corresponding one of said reference macroblocks; and

means for replacing (a) the current macroblock $C_{j,p}$ with a current macroblock $C_{j,p+n}$, said current macroblock $C_{j,p+n}$ being the current macroblock adjacent said macroblock $C_{j,p+n-1}$ in said direction; and (b) said first column of adjacent reference macroblocks $R_{q,i}$, $R_{q+1,i}$, ..., $R_{q+m-1,i}$ with a second column of adjacent reference macroblocks $R_{q,i+1}$, $R_{q+1,i+1}$, ..., $R_{q+m-1,i+1}$, said second column being adjacent said first column in said direction.

24. An adaptive thresholding circuit receiving a first value, a second value and a third value, comprising:

first, second and third registers connected in a pipeline configuration, said first, second and third registers holding respectively said first, second and third values; and

means for setting the content of said second register to zero when (i) said first and third values are zero, and (ii) said second value is less than a predetermined threshold value.

25. A method for encoding digitized video signals representing a series of frames of images, said digitized video signals being stored in an external memory system, said method comprising the steps of:

providing a first and a second video ports, each video port being configurable to be either an input port or an output port for video signals;

using a host bus interface circuit to interface with an external host computer;

storing a portion of said series of frames of images in a scratch-pad memory;

providing a processor for arithmetic and logic operations, wherein said processor computing coefficients of a discrete cosine transform of said portion of said series of frames of images, and for applying a quantization step for said coefficients to obtained quantized coefficients under a lossy compression algorithm;

matching objects in motion between said frames of images using a motion estimation unit, said motion estimation unit providing as data output motion vectors representing said motion of said objects in motion between said frames of images;

applying in a variable-length coding unit an entropy coding scheme on said quantized coefficients and said motion vectors to represent said video signals;

providing a global bus accessible by said first and second video port, said host bus interface, said scratch-pad memory, said processor, said motion estimation unit, and said variable-length coding unit, said global bus providing data transfer among said first and second video port, said host bus interface, said scratch-pad memory, said processor, said motion estimation unit, and said variable-length coding unit;

providing a processor bus having a higher bandwidth than said global bus for providing data transfer among said processor, said scratch-pad memory, and said variable-length coding unit; and

providing a memory controller for (a) controlling data transfers between said external memory and said structure, and (b) for controlling the uses of said global bus and said processor bus.

26. A method for providing an interface for receiving digitized video signals, said digitized signals including samples of a luminance component and first and second chrominance components provided to said interface in pixel interleaved order, said method comprising the steps of:

dividing a memory into groups of regions, each group of regions having a first region, a second region and a third region for storing said samples of said luminance component and said first and second chrominance components respectively;

maintaining a count of said digitized video signals, said count being incremented as each sample arrives at said interface; and

generating an address for storing in said memory each of said samples of digitized video samples in accordance with said count, such that a sample of said luminance component is stored in said first region, a sample of said first chrominance component is stored in said second region and a sample of said second chrominance component is stored in said third region.

27. A method for synchronizing a first and a second clock signals, comprising:

a first step for detecting a transition of said second clock signal between a first and a second transitions of said first clock signal, said first and second transitions of said first clock signal being successive transitions;

a second step for detecting a transition of said second clock signal between said second transition and a third transition of said first clock signal, said second and third transitions of said first clock signal being successive transitions; and

the step of outputting a detected transition of said first and second steps at a fourth transition of said first clock signal, said fourth transition being a transition of said first clock signal subsequent to said third transition of said first clock signal.

28. A method for accessing matrix data in either column or row order, comprising the steps of:

providing a plurality of memory cells organized as an s X s matrix of addressable units; and

generating any one of 2s addresses for accessing said addressable units, wherein s of said 2s

addresses access s rows of said matrix, and the remaining s addresses access s columns of said matrix.

29. A method for providing a high performance central processing unit, comprising:

providing a data memory having a plurality of data words, each data word having a word width of n*m bits, where n and m are integers;

providing a first set of n registers for storing n data words, each data word having a width of m bits, said n registers structured such that (i) for input purpose, said first set of n registers receives an n*m bit data word from said data memory simultaneously as a single n*m-bit register, and (ii) for output purpose, each of said n registers is addressed independently;

providing an arithmetic and logic unit receiving a plurality of m-bit operands from said first set of n registers and providing as a result of an operation an m-bit result; and

providing a second set of n registers for storing n data words, each data word having a width of m bits, said second set of n registers structured such that (i) for input purpose, each of said n registers is addressed independently for receiving said m-bit result from an operation of said arithmetic unit; and (ii) for output purpose, said second set of n registers output an n*m bit data word to said data memory simultaneously as a single n*m-bitregister.

30. A method for providing a memory controller for a processor having a plurality of functional units, comprising:

controlling, in a first interface, access to an external memory system;

controlling, in a second interface, a first internal bus, said first internal bus being m-bit wide, m being an integer;

controlling, in a third interface, a second internal bus, said second internal bus being n*m-bit wide, n being an integer;

providing an arbitration unit for receiving data transfer requests from said functional units and for granting use of said first and second internal busses to a selected one of said functional units; and

in a direct memory access unit, controlling data transfer among said selected functional unit, said first and second internal busses and said data memory, over said first, second and third interfaces.

31. A method for organizing a memory structure for accessing image data, comprising the steps of:

providing a memory divided into a first half and a second half for providing a 2m-bit output datum, said 2m-bit output datum being formed by concatenating a first datum and a second m-bit datum, said first m-bit datum being provided from said first half of said memory by activating, in response to a first address, one of a first set of word lines, and said second m-bit datum being provided from said second half of said memory by activating, in response to a second address, one of a second set of word line; and

generating said first and second address, said first and second address being constrained to be identical except for one bit.

32. A method for flexible rearrangement of operands, comprising the steps of:

providing an arithmetic and logic unit receiving first and second operands, each operand including a predetermined number of data elements, said arithmetic logic unit performing simultaneously arithmetic and logic operations between data elements of said first operand and data elements of said second operand, each of said operation involving one data element of said first operand and a corresponding data element of said second operand;

rearranging in a first set of multiplexor, prior to providing said first operand to said arithmetic and logic unit, the order of said data elements in said first operand; and

rearranging in a second set of multiplexor, prior to providing said second operand to said arithmetic and logic unit, the order of said data elements in said second operand.

33. A method for providing a non-linear filter comprising, the steps of:

setting a first threshold value T_1;

setting a second threshold value T_2;

receiving first and second operands x and y to provide an absolute difference between x and y;

receiving said absolute difference and said first and second threshold values to provide a weighting factor a equal to (i) when said when said absolute difference is less than T_1, a predetermined weight less than 1.0, (ii) when said absolute difference is between T_1 and T_2, a value between said

predetermined weight and 1.0, said value being proportional to the said absolute difference, and (iii) when said absolute difference is greater than T_2, 1.0; and

providing a filter output having the value x + a(y-x).

34. A structure for deinterlacing a digitized video signal, said video signal comprising pixels from a first field and a second field of an image, said structure comprising:

for each pixel x in said first field of said image: (i) a circuit for identifying the corresponding pixel y in said second field of said image;

(ii) a circuit for computing an absolute difference between x and y;

(iii) a circuit for determining a weight a equalling (a) 0.5, when said absolute difference is less than a first threshold value T_1, (b) 1.0, when said absolute difference is greater than a second threshold value T_2, and (c) a value proportional to said absolute difference; and

(iv) a circuit for providing as a pixel of a deinterlaced image a pixel z having the value x + a(y-x).

35. A circuit for a temporal noise filter for a video signal, said video signal comprising pixels of successive frames of images displayable on a screen, said circuit comprising:

a circuit for, for position x in a screen, receiving a stream of pixel values x_0, x_1, ..., x_T, corresponding to values of the pixel at said position x at time points 0, 1, ..., T, wherein said time points correspond to arrivals of said successive frames of images; and

a circuit for providing as an initial filter output value of said temporal noise filter y_0 the value x_0;

a circuit for, for each time point t:

(i) computing an absolute difference between y_{t-1}, being the filter output value of said temporal noise filter at time point t-1, and x_t, being the current value of pixel x at said time point t;

(ii) determining a weight a equalling (a) 0.5, when said absolute difference is less than a first threshold value T_1, (b) 1.0, when said absolute difference is greater than a second threshold value T_2, and (c) a value proportional to said absolute difference; and

(iii) providing as filter output value of temporal noise filter a value y_t having the value $x_t + a(y_{t-1}-x_{t-1})$.

36. A circuit for scene analysis used to apply adaptive control technique in an image processing method, said image including a plurality of macroblocks, each macroblock a plurality of quad pels, being 2 X 2 configurations of pixels, said circuit for scene analysis comprises:

a circuit for, for each quad pel in each macroblock:

(i) computing simultaneously first and second absolute differences, said first absolute difference being an absolute difference between a first pixel within said quad pel and a second pixel within said quad pel, said second absolute difference being an absolute difference between said second pixel and a third pixel of said quad pel; and

(ii) accumulating said first and second absolute differences in first and second accumulated sums; and

means for applying said adaptive control technique using said first and second accumulated sums as activity parameters.

37. A structure for eliminating redundant fields in an video signal to improve a data compression ratio, each field comprises a plurality of quad pels, each quad pel being a configuration of 2 X 2 pixels, said structure comprising:

means, for each quad pel in a first field, for:

(i) computing a first, a second, a third and a fourth differences between pixels in said quad pel and corresponding pixels of a corresponding quad pel in a second field; and

(ii) providing a count equal to the number of said first, second, third and fourth differences exceeding in magnitude a predetermined threshold value; means for accumulating said count over all quad pels in said first field; and

means for eliminating said second field when said accumulated count exceeds a second predetermined threshold value.

38. A method for zero-lookahead, comprising the steps of:

providing a plurality of zero generator circuits, each zero generator circuit receiving as input 1-bit signals a and b, and providing as output signals P, Z+ and Z- representing, respectively, whether the values of said signals a and b are not the same, the values of said signals a and b are equal to '1', and

the values of said signals a and b are equal to '0'; and

providing a plurality of zero propagator circuits, each of said propagator circuits receiving as input signals (i) P_1, $Z+_1$, and $Z-_1$, being a first of said P, Z and Z- signals, and (ii) P_2, $Z+_2$, and $Z-_2$, being a second set and of said P, Z+ and Z- signals, and providing as output signals a third set of P, Z and Z- signals in accordance with the logic equations:

$P = P_1$ and P_2;
$Z- = Z-_1$ and $Z-_2$;
and $Z+ = (Z+_1$ and $P_2)$ or $(Z+_2$ and $Z-_{1})$;

wherein said plurality of zero propagator circuits are connected in a tree configuration, having a leaf level receiving inputs from said plurality of zero generator circuits; and

providing an OR gate connected to the zero propagator circuit at the root of said tree configuration of zero propagating circuits, said OR gate receiving as input signals said Z+ and Z-signal providing output signal Z, representing whether a zero is detected.

39. A method for performing motion estimation in the compression of video data, said video data comprising macroblocks of pixels in a current frame and macroblocks of pixels in a reference frame, said method comprising teh steps of:

storing in a memory said macroblocks of said current frame and said macroblocks of said reference frame;

receiving in a filter a first group of pixels from said memory for resampling said first group of pixels, said first group of pixels being pixels from said macroblocks of said reference frame; and

receiving in a matcher said resampled first group of pixels and a second group of pixels, said matcher matching said second group of pixels to said first group of pixels, for deriving a set of scores each corresponding to one of a predetermined group of motion vectors, said second group of pixels being pixels from a macroblock of a current frame and each of said scores being a measure of the differences between said second group of pixels and said first group of pixels under a corresponding motion vector within said predetermined group; and

selecting among said predetermined group of motion vectors, a motion vector for said macroblock of said current frame.

40. A structure for performing motion estimation for a video signal, said video signal comprising a first group of pixels from a current frame and a second group of pixels in a reference frame, said structure comprising:

means for resampling said first and second groups of pixels to obtain a third group of pixels and a fourth group of pixels, said third and fourth groups of pixels being representations of said video signal at a first reduced resolution;

means for performing a first reduced resolution motion estimation based on a said third and fourth groups of pixels to obtain a first motion vector;

means for performing a second motion estimation using said first group of pixels, translated by said first motion vector, and a subset of said second group of pixels to obtain an incremental motion vector, said subset of said second group of pixels being pixels within a predetermined distance of the target position of said first motion vector; and

means for providing as output a motion vector equalling the sum of said first motion vector and said incremental motion vector.

41. A method for encoding by motion vectors a current frame of video data using a reference frame of video data, each of said current and reference frames being divided into rows and columns of macroblocks, said macroblocks of said current frames being designated "current macroblocks" and said macroblocks of said reference frame being designated "reference macroblocks", each marcoblock representing an area of pixels in the corresponding frame, said method comprising the steps of:

storing in a memory circuit (a) a plurality of adjacent current macroblocks from a row j of current macroblocks, said plurality of said adjacent current macroblocks being designated $C_{j,p}$, $C_{j,p+1}$, ..., $C_{j,p+n-1}$ in the order along one direction of said row of macroblocks; and (b) a plurality of adjacent reference macroblocks from a first column i of reference macroblocks, said plurality of reference macroblocks being designated $R_{q,i}$, $R_{q+1,i}$, ..., $R_{q+m-1,i}$, said plurality of adjacent reference macroblocks being reference macroblocks within the range of said motion vectors, each of said current macroblocks

being substantially equidistance from said $R_{q,i}$ and $Rq + _{m-1,i}$ reference macroblocks;

evaluating each of said plurality of adjacent current macroblocks against each of said plurality of adjacent reference macroblocks under said motion vectors to select a motion vector best representing the best match between each of said current macroblock and a corresponding one of said reference macroblocks; and

replacing (a) the current macroblock $C_{j,p}$ with a current macroblock $C_{j,p+n}$, said current macroblock $C_{j,p+n}$ being the current macroblock adjacent said macroblock $C_{j,p+n-1}$ in said direction; and (b) said first column of adjacent reference macroblocks $R_{q,i}$, $R_{q+1,i}$, ..., $R_{q+m-1,i}$ with a second column of adjacent reference macroblocks $R_{q,i+1}$, $R_{q+1,i+1}$, ..., $R_{q+m-1,i+1}$, said second column being adjacent said first column in said direction.

42. A method for adaptive thresholding using a first value, a second value and a third value, comprising the steps of:

storing said first, second and third values in a first, a second and a third registers connected in a pipeline configuration; and

setting the content of said second register to zero when (i) said first and third values are zero, and (ii) said second value is less than a predetermined threshold value.

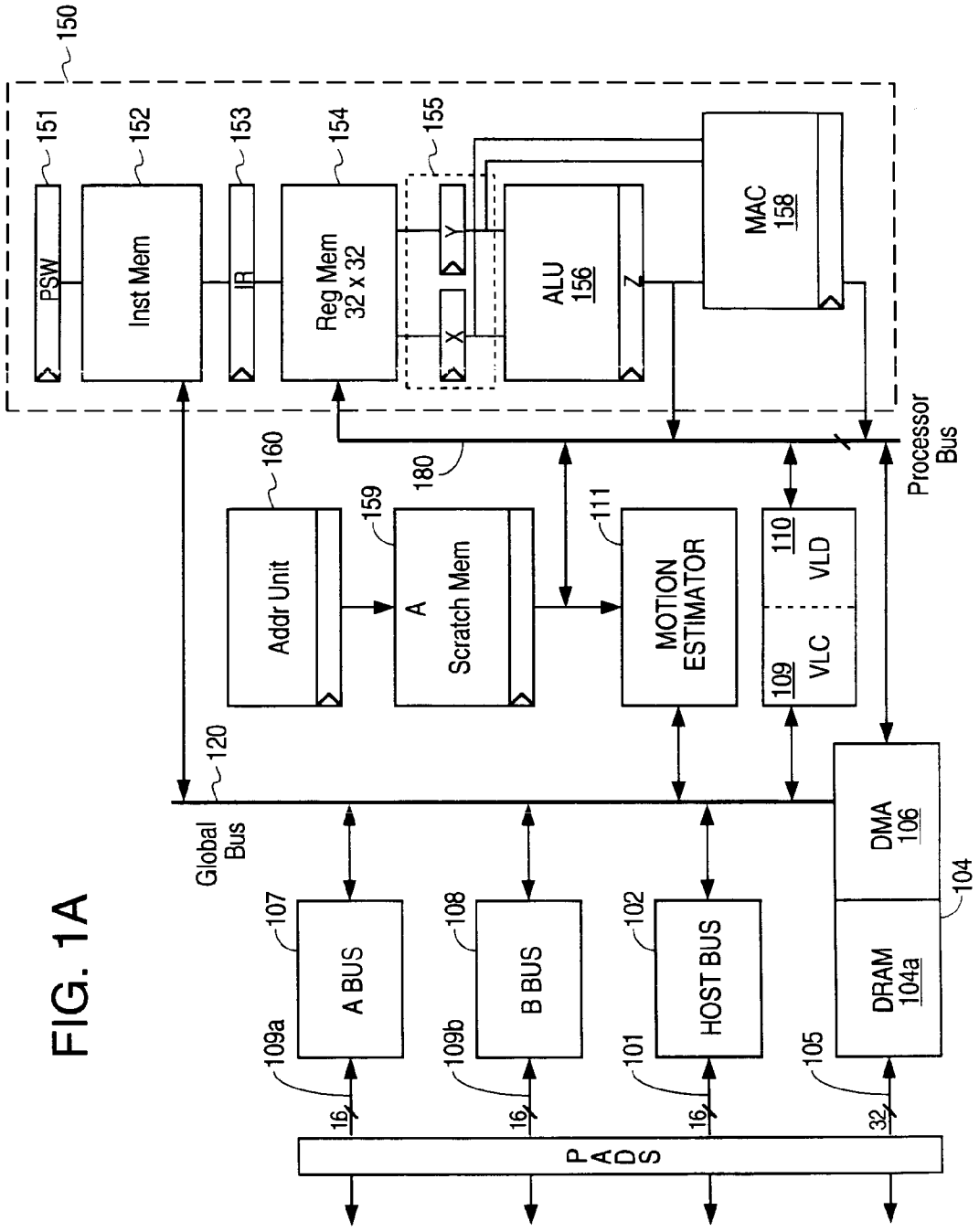

150
151
PSW
152
Inst Mem
153
IR
154
Reg Mem
32 x 32
155
Y
X
ALU
156
Z
MAC
158
Processor
Bus
180
160
Addr Unit
159
A
Scratch Mem
111
MOTION
ESTIMATOR
110
VLD
109
VLC
120
Global
Bus
DMA
106
104
DRAM
104a
107
A BUS
108
B BUS
102
HOST BUS
109a
109b
101
105
16
16
16
32
P
A
D
S

FIG. 1A

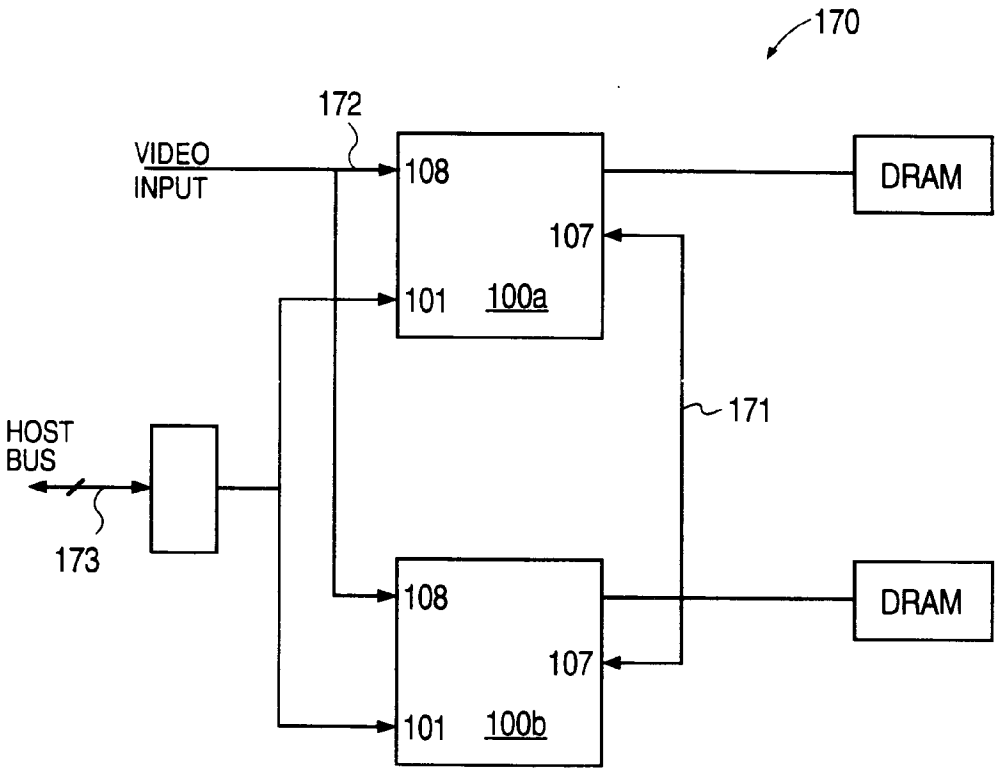

170
172
VIDEO
INPUT
108
107
101
100a
DRAM
171
HOST
BUS
173
108
107
101
100b
DRAM

FIG. 1B

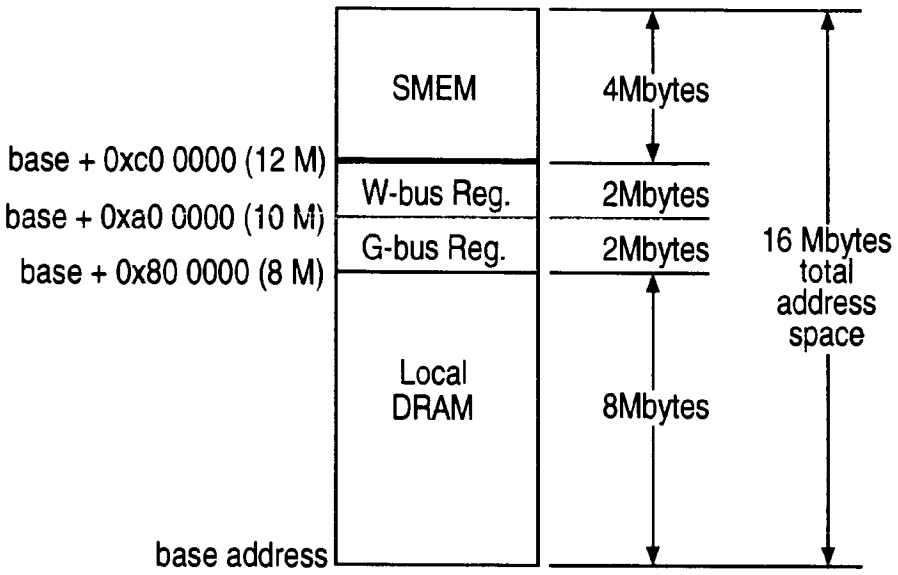

SMEM
4Mbytes
base + 0xc0 0000 (12 M)
W-bus Reg.
2Mbytes
base + 0xa0 0000 (10 M)
G-bus Reg.
2Mbytes
base + 0x80 0000 (8 M)
16 Mbytes total address space
Local DRAM
8Mbytes
base address

FIG. 1C

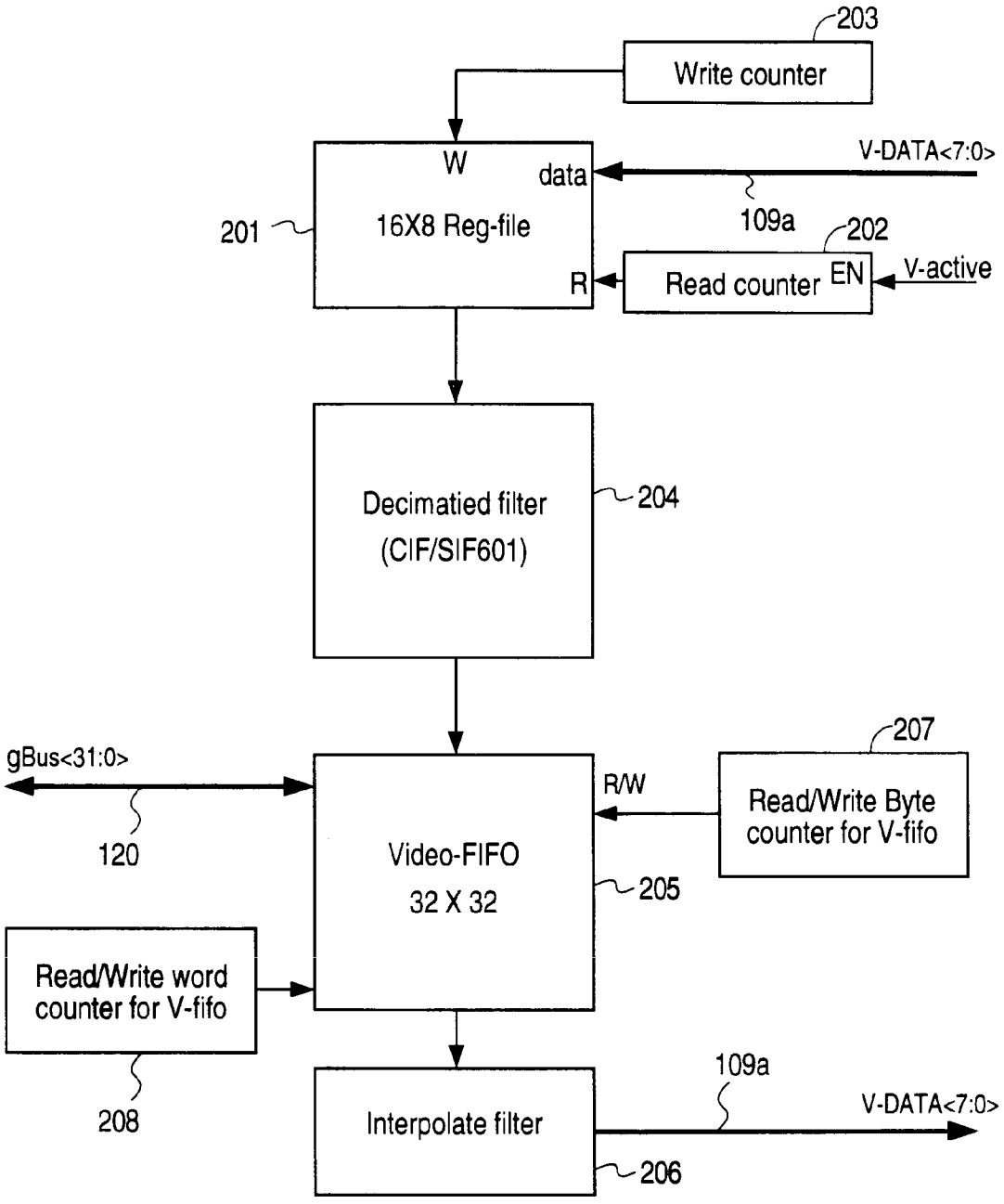

203
Write counter
W
data
V-DATA<7:0>
201
16X8 Reg-file
109a
202
R
Read counter
EN
V-active
Decimatied filter
(CIF/SIF601)
204
gBus<31:0>
120
207
R/W
Read/Write Byte
counter for V-fifo
Video-FIFO
32 X 32
205
Read/Write word
counter for V-fifo
208
109a
Interpolate filter
V-DATA<7:0>
206

FIG. 2

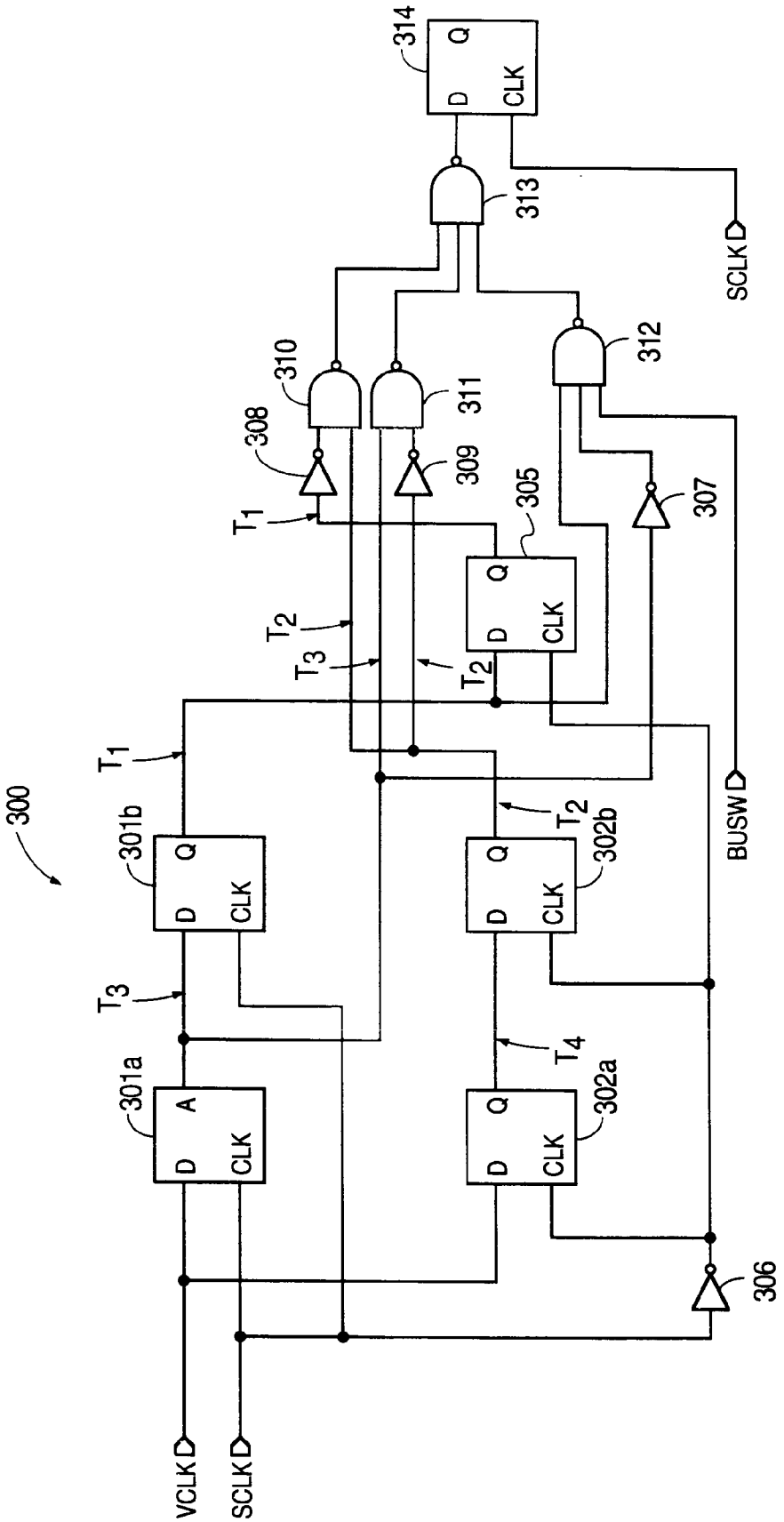

300
301a
301b
302a
302b
305
306
307
308
309
310
311
312
313
314
A
D
Q
CLK
T1
T2
T3
T4
VCLK D
SCLK D
BUSW D

FIG. 3A

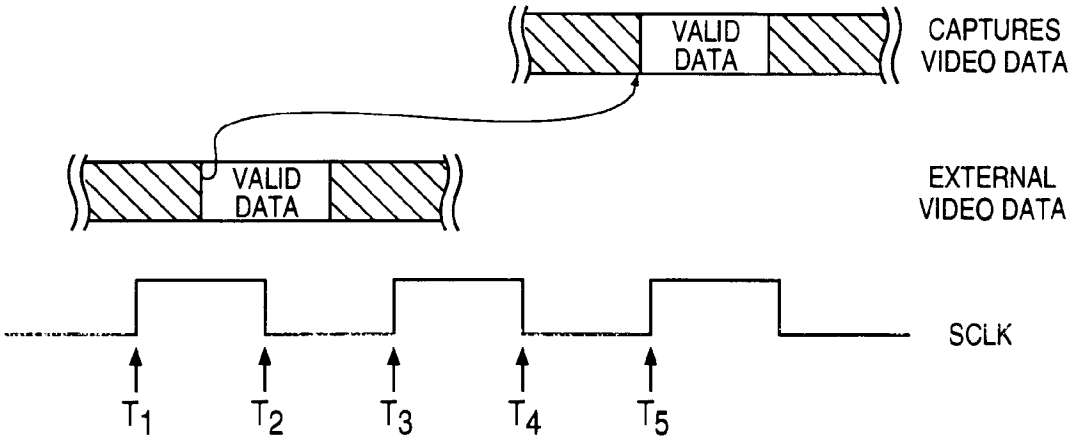

VALID DATA
CAPTURES VIDEO DATA
VALID DATA
EXTERNAL VIDEO DATA
SCLK
T1
T2
T3
T4
T5

FIG. 3B

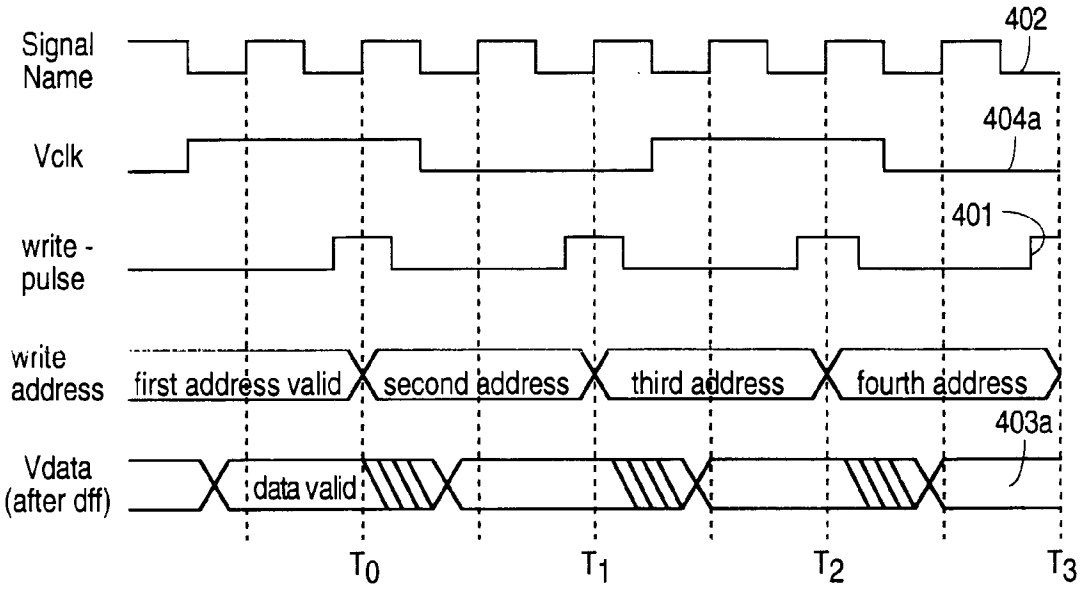

Signal Name
Vclk
write - pulse
write address
Vdata (after dff)
first address valid
second address
third address
fourth address
data valid
402
404a
401
403a
T0
T1
T2
T3

FIG. 4A

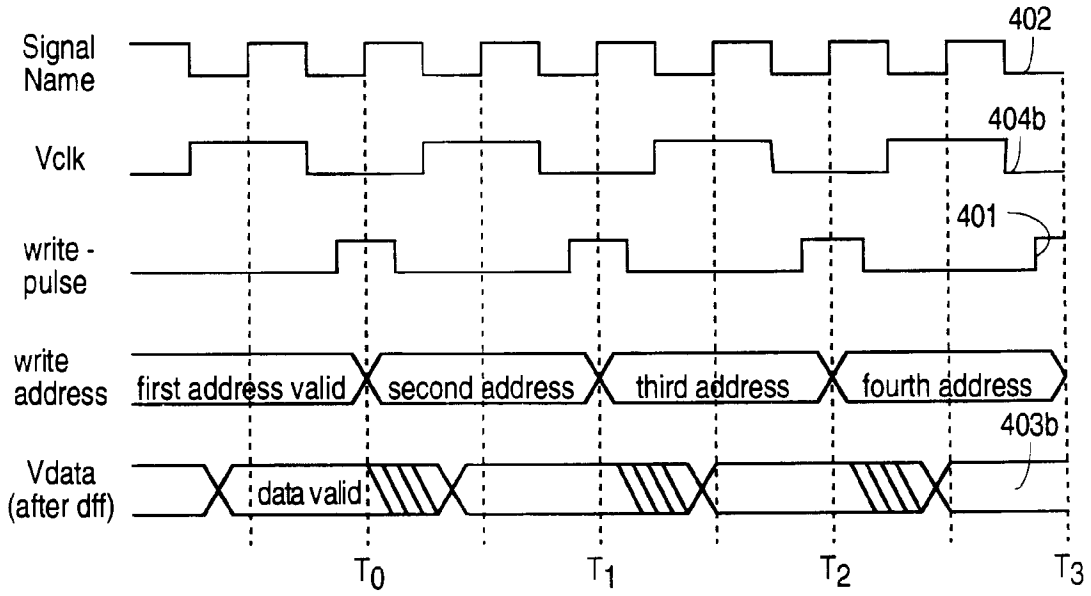

Signal Name
Vclk
write - pulse
write address
Vdata (after dff)
first address valid
second address
third address
fourth address
data valid
402
404b
401
403b
T0
T1
T2
T3

FIG. 4B

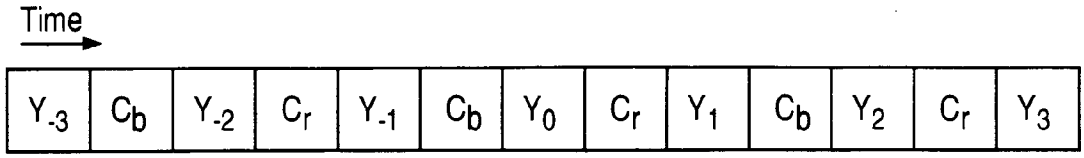


FIG. 5A

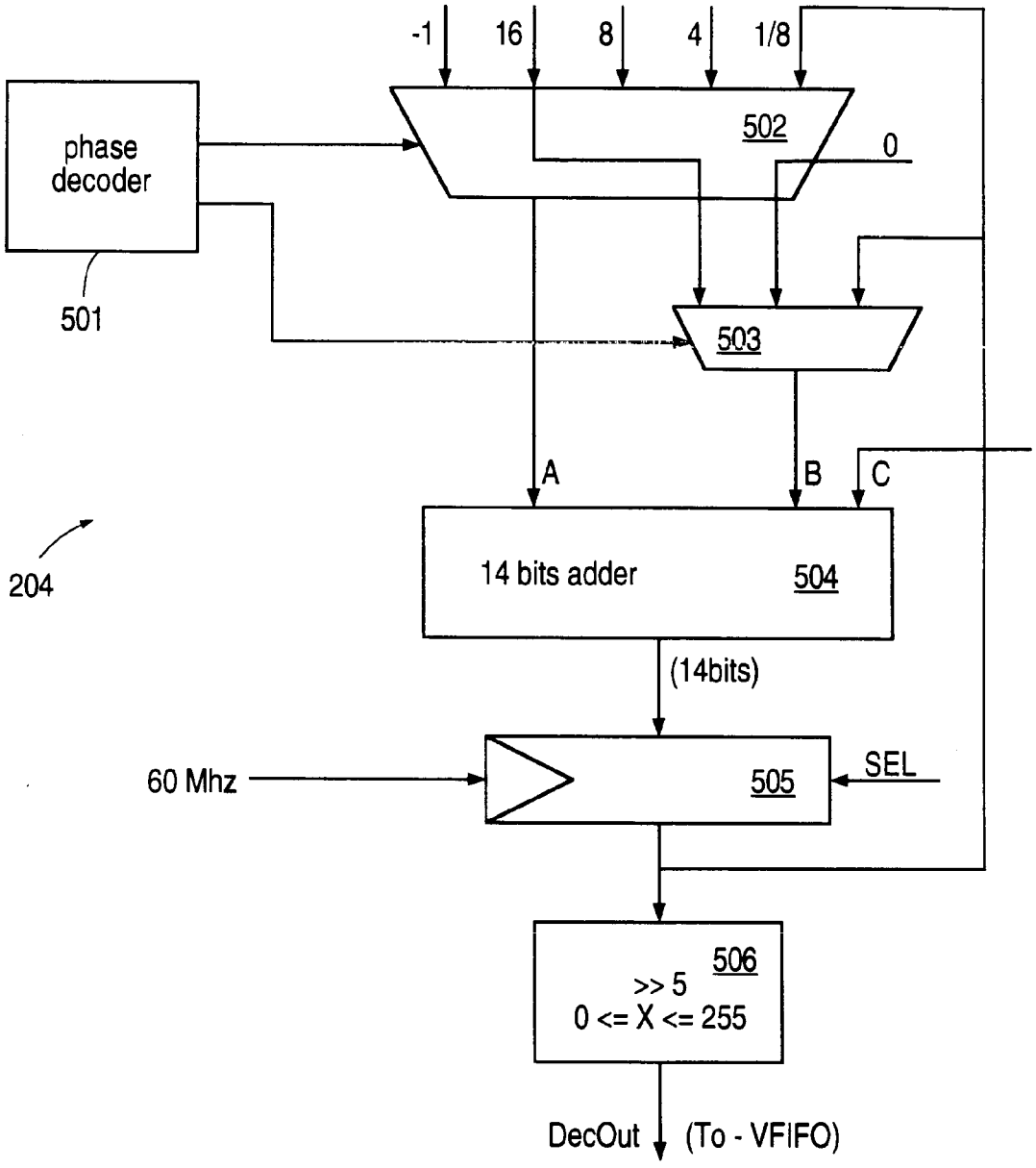

-1
16
8
4
1/8
502
0
phase decoder
501
503
A
B
C
204
14 bits adder
504
(14bits)
60 Mhz
505
SEL
506
>> 5
0 <= X <= 255
DecOut
(To - VFIFO)

FIG. 5B

	phase-0	phase-1	phase-2	phase-3	phase-4	phase-5	phase-6	phase-7
ROUT	D0	D1	B0	B1		A	C0	C1
Ain	16D0+R	16D1+R	8B0	8B1	Sum/8	16A+R	-C0	-C1
Bin	0	Sum	0	Sum	Sum	Sum	Sum	Sum
Cin	0	0	0	0	0	1	1	1
Dec	0	Sum/32	0	0	0	0	0	Sum/32

LUMA DATA :

DecOut = -1/32 C0+ 9/32B0 + 1/2A + 9/32 B1 -1/32C1

CHROMA DATA;

DecOut = 1/2 D0 + 1/2D1

* Rounding = 15 ;

FIG. 5C

EP 0 639 032 A2

	phase-0	phase-1	phase-2	phase-3	phase-4	phase-5	phase-6	phase-7
ROUT	D	A	B0	B1				
Ain	16D+R	8A	4B0	4B1				
Bin	16D+R	16A+R	Sum	Sum				
Cin	0	1	0	0				
Dec	Sum/32			Sum/32				

LUMA DATA :

DecOut = 1/8B0 + 3/4A + 1/8B1

CHROMA DATA

DecOut = D

FIG. 5D

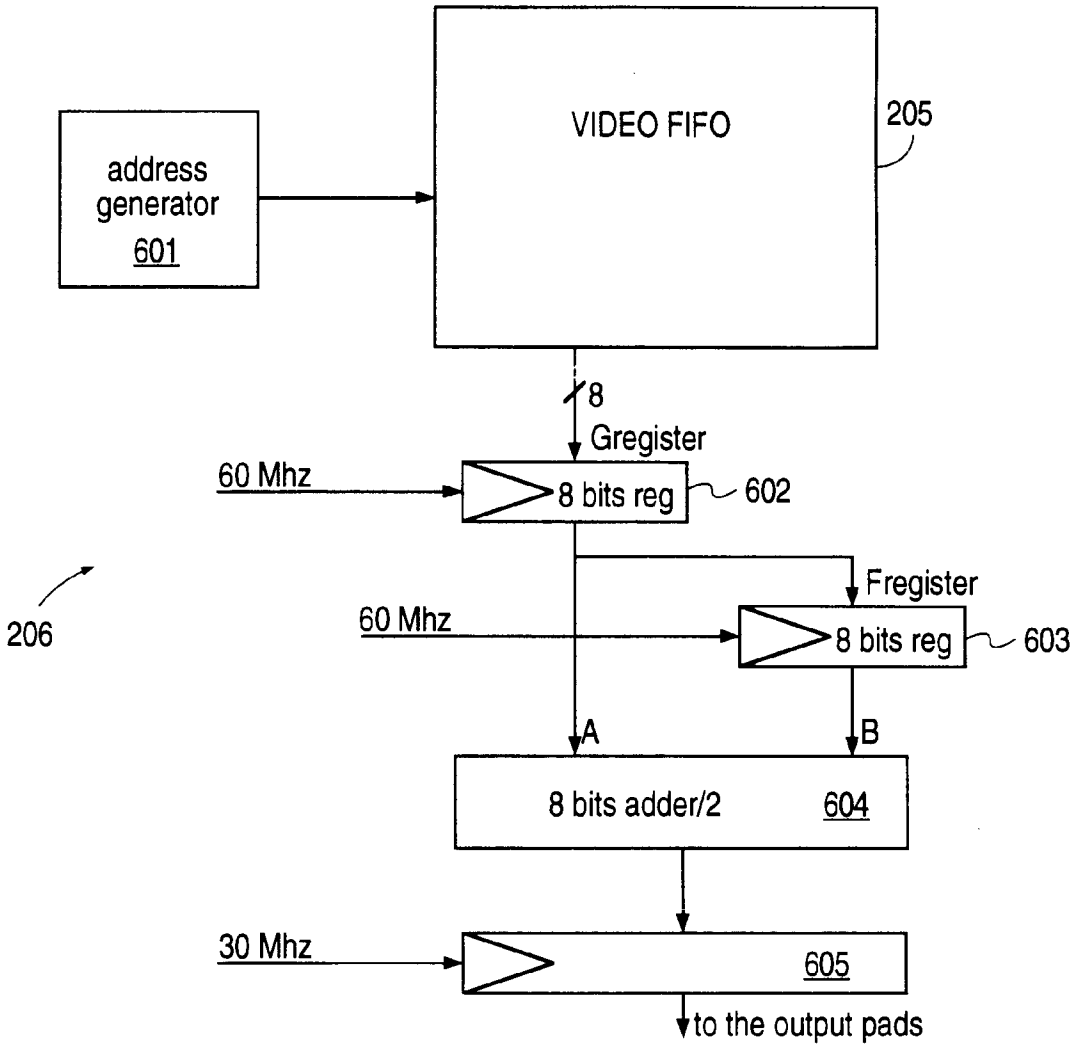

VIDEO FIFO
205
address generator
601
8
Gregister
60 Mhz
8 bits reg
602
206
Fregister
60 Mhz
8 bits reg
603
A
B
8 bits adder/2
604
30 Mhz
605
to the output pads

FIG. 6A

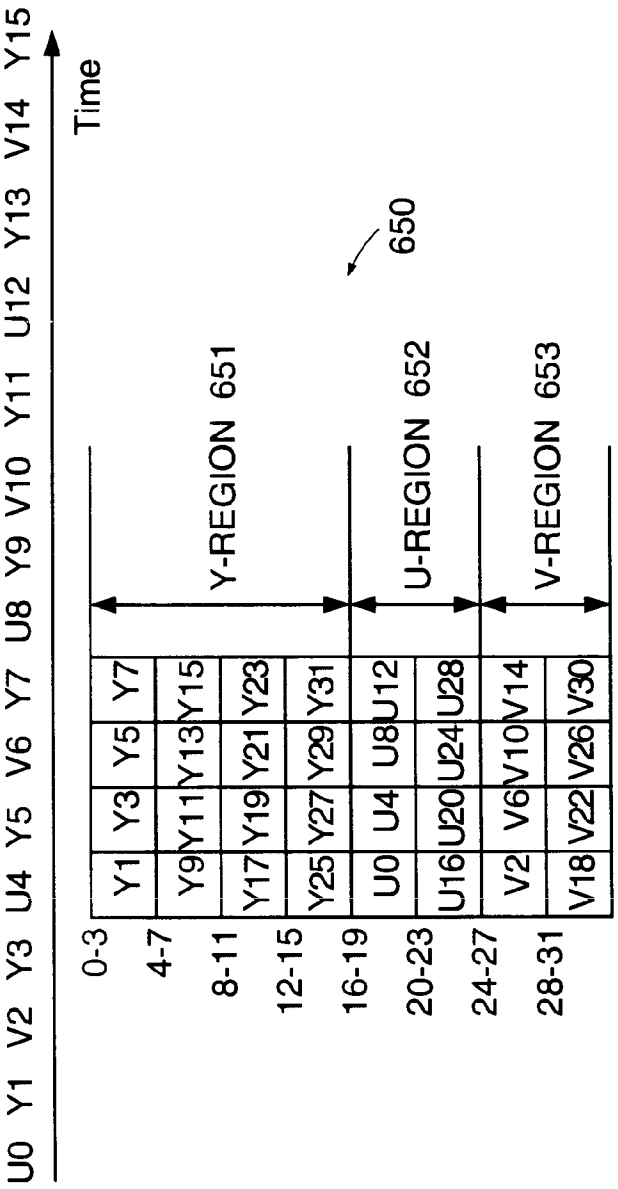

U0 Y1 V2 Y3 U4 Y5 V6 Y7 U8 Y9 V10 Y11 U12 Y13 V14 Y15
Time
654
650
Y-REGION 651
U-REGION 652
V-REGION 653
0-3
4-7
8-11
12-15
16-19
20-23
24-27
28-31
Y1 Y3 Y5 Y7
Y9 Y11 Y13 Y15
Y17 Y19 Y21 Y23
Y25 Y27 Y29 Y31
U0 U4 U8 U12
U16 U20 U24 U28
V2 V6 V10 V14
V18 V22 V26 V30

FIG. 6B

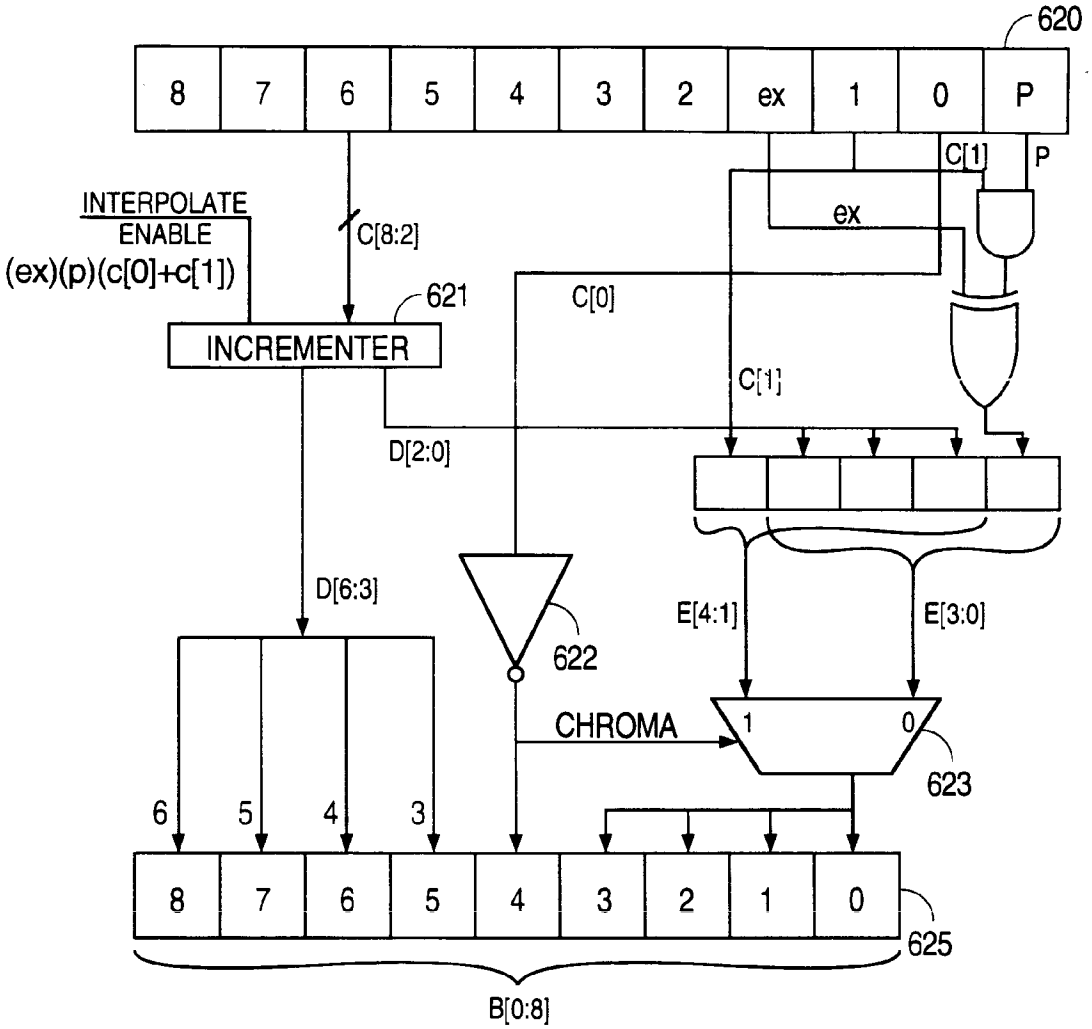
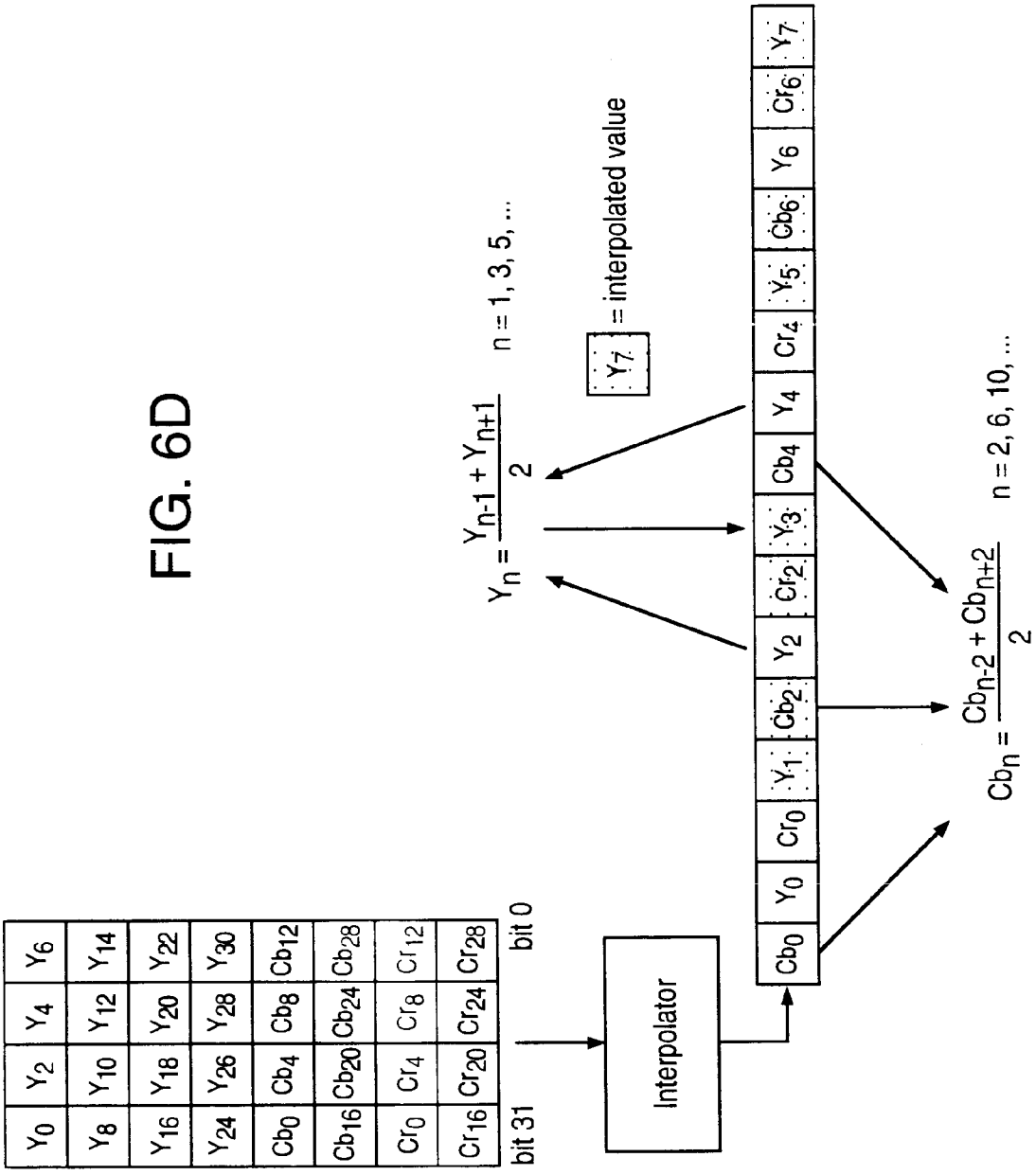

620
8
7
6
5
4
3
2
ex
1
0
P
C[1]
P
ex
INTERPOLATE
ENABLE
(ex)(p)(c[0]+c[1])
C[8:2]
621
INCREMENTER
C[0]
C[1]
D[2:0]
D[6:3]
622
E[4:1]
E[3:0]
CHROMA
1
0
623
6
5
4
3
8
7
6
5
4
3
2
1
0
625
B[0:8]

FIG. 6C

FIG. 6D


Y0 Y2 Y4 Y6
Y8 Y10 Y12 Y14
Y16 Y18 Y20 Y22
Y24 Y26 Y28 Y30
Cb0 Cb4 Cb8 Cb12
Cb16 Cb20 Cb24 Cb28
Cr0 Cr4 Cr8 Cr12
Cr16 Cr20 Cr24 Cr28
bit 31
bit 0
Interpolator
Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3 Cb4 Y4 Cr4 Y5 Cb6 Y6 Cr6 Y7
Yn = (Yn-1 + Yn+1)/2
n = 1, 3, 5, ...
Y7 = interpolated value
Cbn = (Cbn-2 + Cbn+2)/2
n = 2, 6, 10, ...

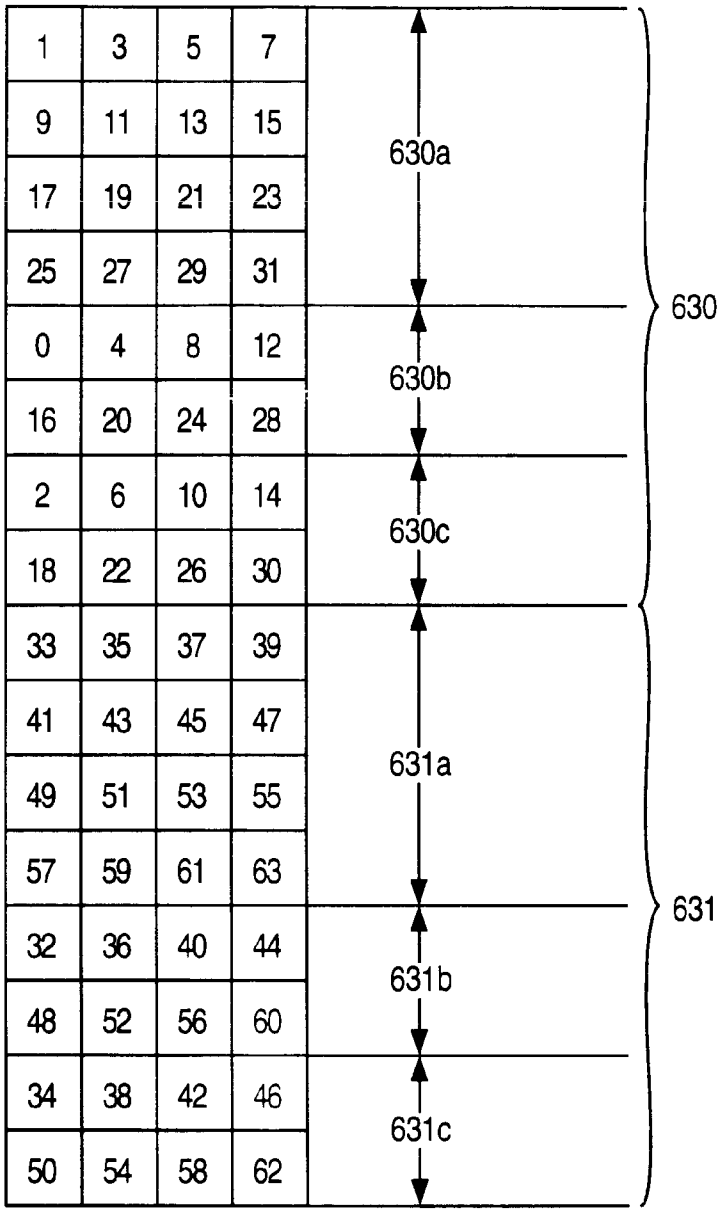

1 3 5 7
9 11 13 15
17 19 21 23
25 27 29 31
630a
0 4 8 12
16 20 24 28
630b
2 6 10 14
18 22 26 30
630c
630
33 35 37 39
41 43 45 47
49 51 53 55
57 59 61 63
631a
32 36 40 44
48 52 56 60
631b
34 38 42 46
50 54 58 62
631c
631

FIG. 6E

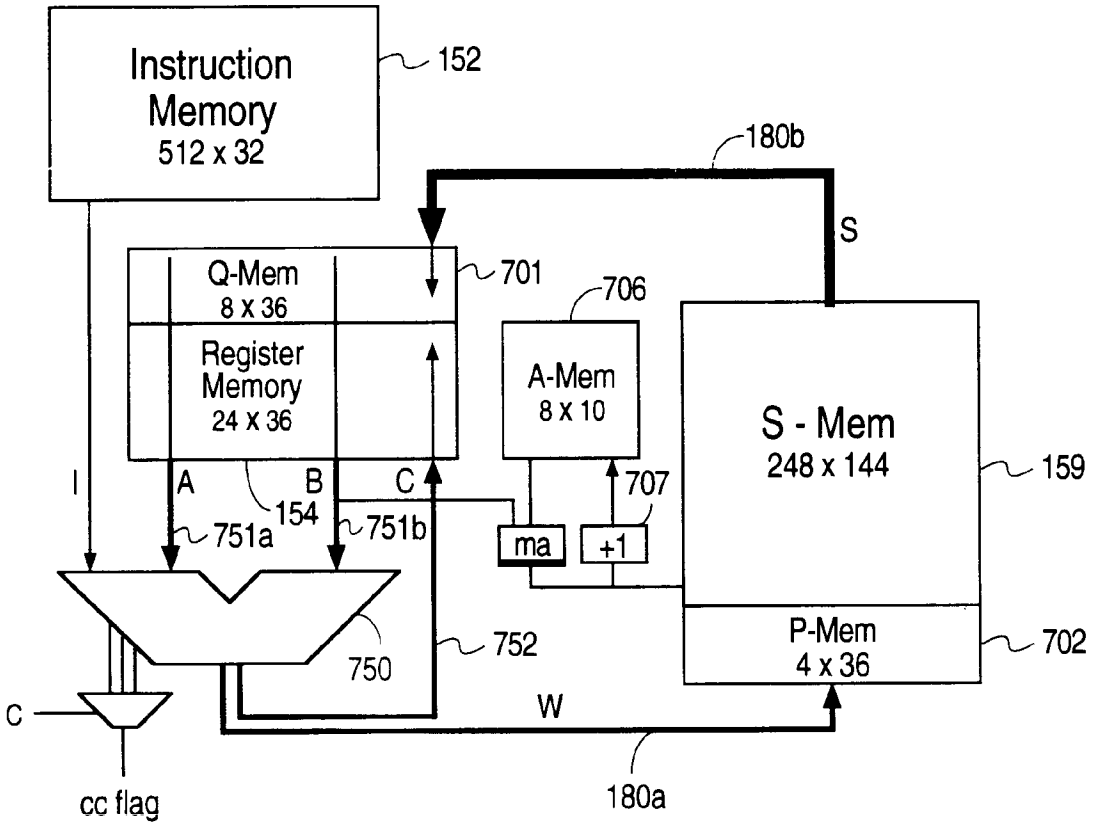

Instruction Memory
512 x 32
152
180b
S
Q-Mem
8 x 36
Register Memory
24 x 36
701
706
A-Mem
8 x 10
S - Mem
248 x 144
159
I
A
B
C
154
751a
751b
707
ma
+1
750
752
P-Mem
4 x 36
702
C
W
cc flag
180a

FIG. 7A

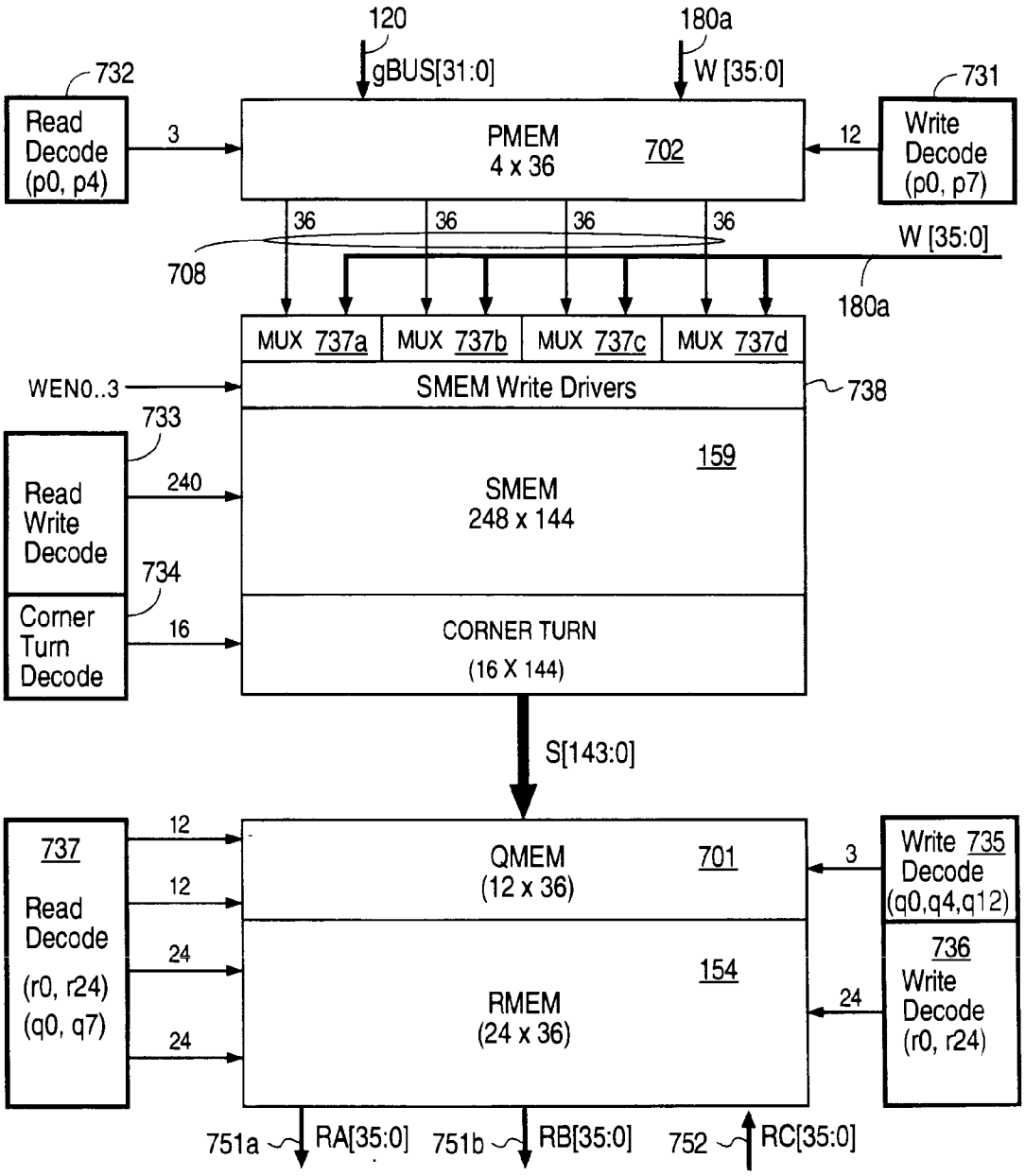

120
gBUS[31:0]
180a
W [35:0]
732
Read Decode (p0, p4)
3
PMEM 4 x 36
702
12
731
Write Decode (p0, p7)
36
36
36
36
708
W [35:0]
180a
MUX 737a
MUX 737b
MUX 737c
MUX 737d
WEN0..3
SMEM Write Drivers
738
733
Read Write Decode
240
159
SMEM 248 x 144
734
Corner Turn Decode
16
CORNER TURN (16 X 144)
S[143:0]
737
Read Decode (r0, r24) (q0, q7)
12
12
24
24
QMEM (12 x 36)
701
RMEM (24 x 36)
154
3
Write 735 Decode (q0,q4,q12)
736
Write Decode (r0, r24)
24
751a
RA[35:0]
751b
RB[35:0]
752
RC[35:0]

FIG. 7B

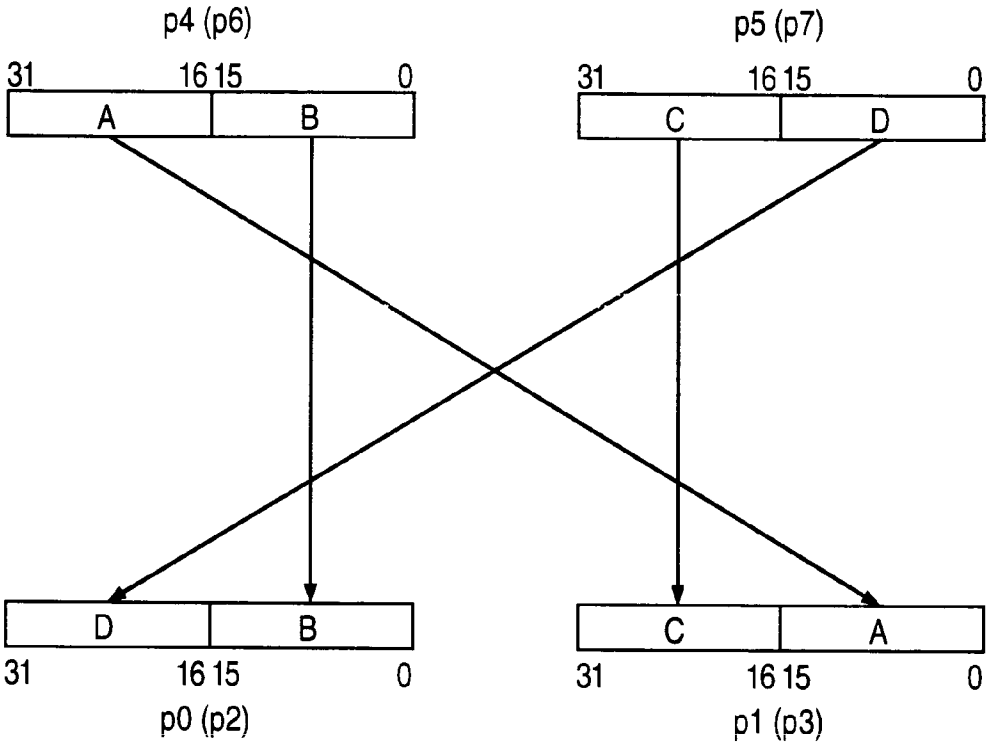

p4 (p6)
31
16 15
0
A
B
p5 (p7)
31
16 15
0
C
D
D
B
31
16 15
0
p0 (p2)
C
A
31
16 15
0
p1 (p3)

FIG. 7C

Alias Address			Physical Address		
Decimal	Word	Byte	Decimal	Word	Byte
992, 993	3e0, 3e1	f80, f84	960,961	3c0,3c1	f00, f04
994, 995	3e2, 3e3	f88, f8c	968, 969	3c8, 3c9	f20, f24
996, 997	3e4, 3e5	f90, f94	976, 977	3d0, 3d1	f40, f44
998, 999	3e6, 3e7	f98, f9c	984, 985	3d8, 3d9	f60, f64
1000, 1001	3e8, 3e9	fa0, fa4	962, 963	3c2, 3c3	f08, f0c
1002, 1003	3ea, 3eb	fa8, fac	970, 971	3ca, 3cb	f28, f2c
1004, 1005	3ec, 3ed	fb0, fb4	978, 979	3d2, 3d3	f48, f4c
1006, 1007	3ee, 3ef	fb8, fbc	986, 987	3da, 3db	f68, f6c
1008, 1009	3f0, 3f1	fc0, fc4	964, 965	3c4, 3c5	f10, f14
1010, 1011	3f2, 3f3	fc8, fcc	972, 973	3cc, 3cd	f30, f34
1012, 1013	3f4, 3f5	fd0, fd4	980, 981	3d4, 3d5	f50, f54
1014, 1015	3f6, 3f7	fd8, fdc	988, 989	3dc, 3dd	f70, f74
1016, 1017	3f8, 3f9	fe0, fe4	966, 967	3c6, 3c7	f18, f1c
1018, 1019	3fa, 3fb	fe8, fec	974, 975	3ce, 3cf	f38, f3c
1020, 1021	3fc, 3fd	ff0, ff4	982, 983	3d6, 3d7	f58, f5c
1022, 1023	3fe, 3ff	ff8, ffc	990, 991	3de, 3df	f78, f7c

FIG. 7D

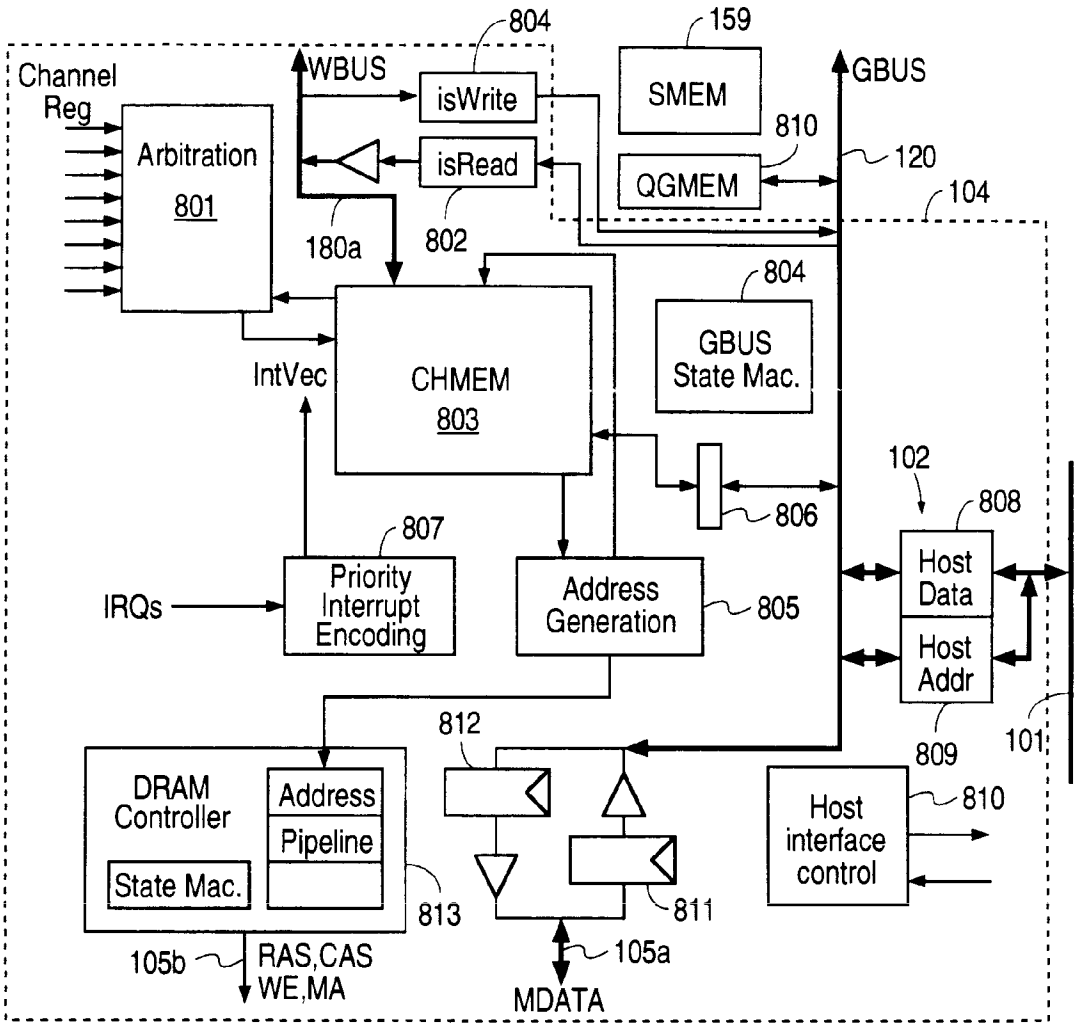

Channel
Reg
Arbitration
801
WBUS
804
isWrite
isRead
802
180a
159
SMEM
GBUS
810
QGMEM
120
104
804
GBUS
State Mac.
IntVec
CHMEM
803
102
806
808
807
Priority
Interrupt
Encoding
IRQs
Address
Generation
805
Host
Data
Host
Addr
809
101
812
DRAM
Controller
Address
Pipeline
State Mac.
813
811
Host
interface
control
810
105b
RAS,CAS
WE,MA
105a
MDATA

FIG. 8A

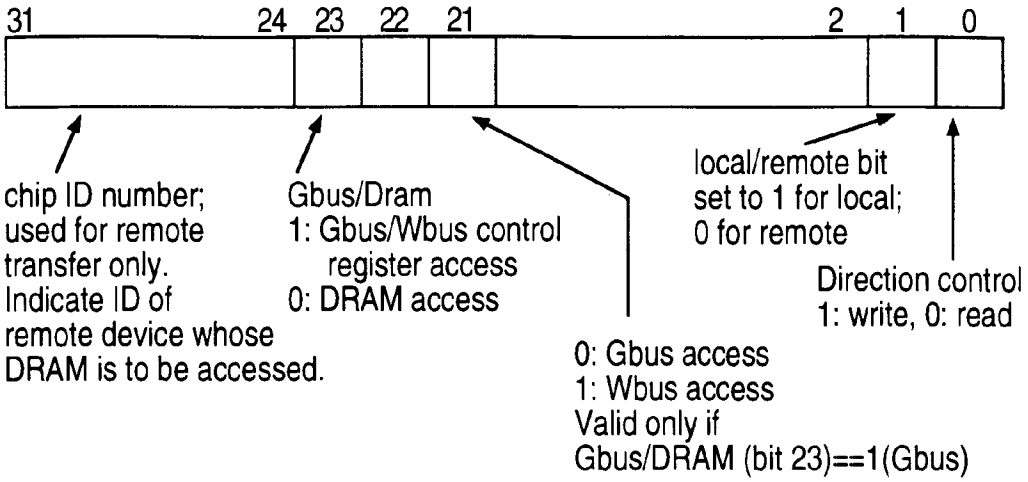


FIG. 8B

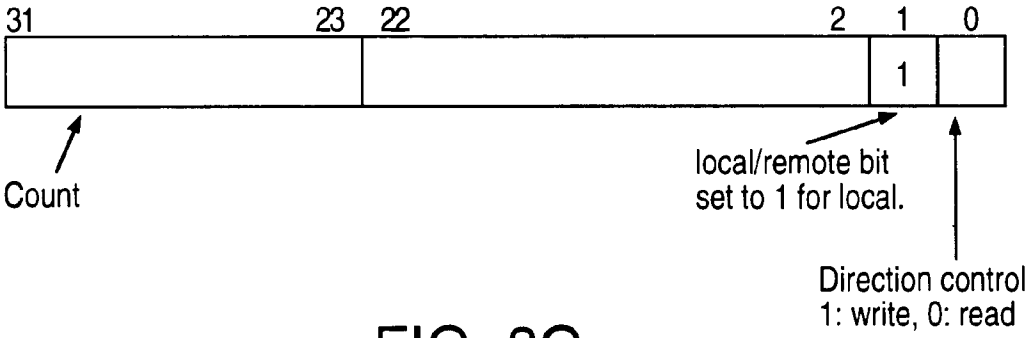


FIG. 8C

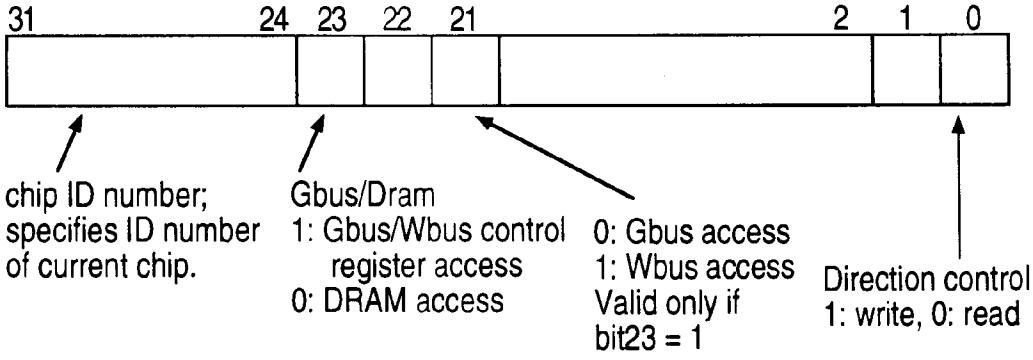


FIG. 8D

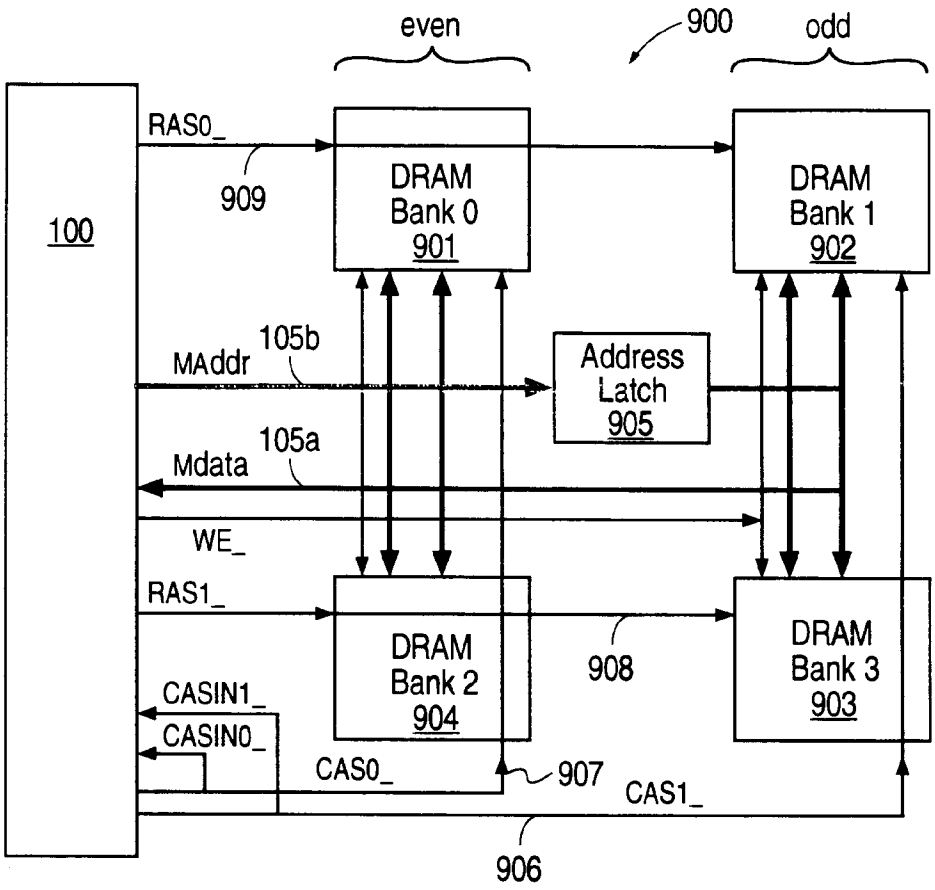

even
900
odd
100
RAS0_
909
DRAM
Bank 0
901
DRAM
Bank 1
902
105b
MAddr
Address
Latch
905
105a
Mdata
WE_
RAS1_
DRAM
Bank 2
904
908
DRAM
Bank 3
903
CASIN1_
CASIN0_
CAS0_
907
CAS1_
906

FIG. 9A

FIG. 9B

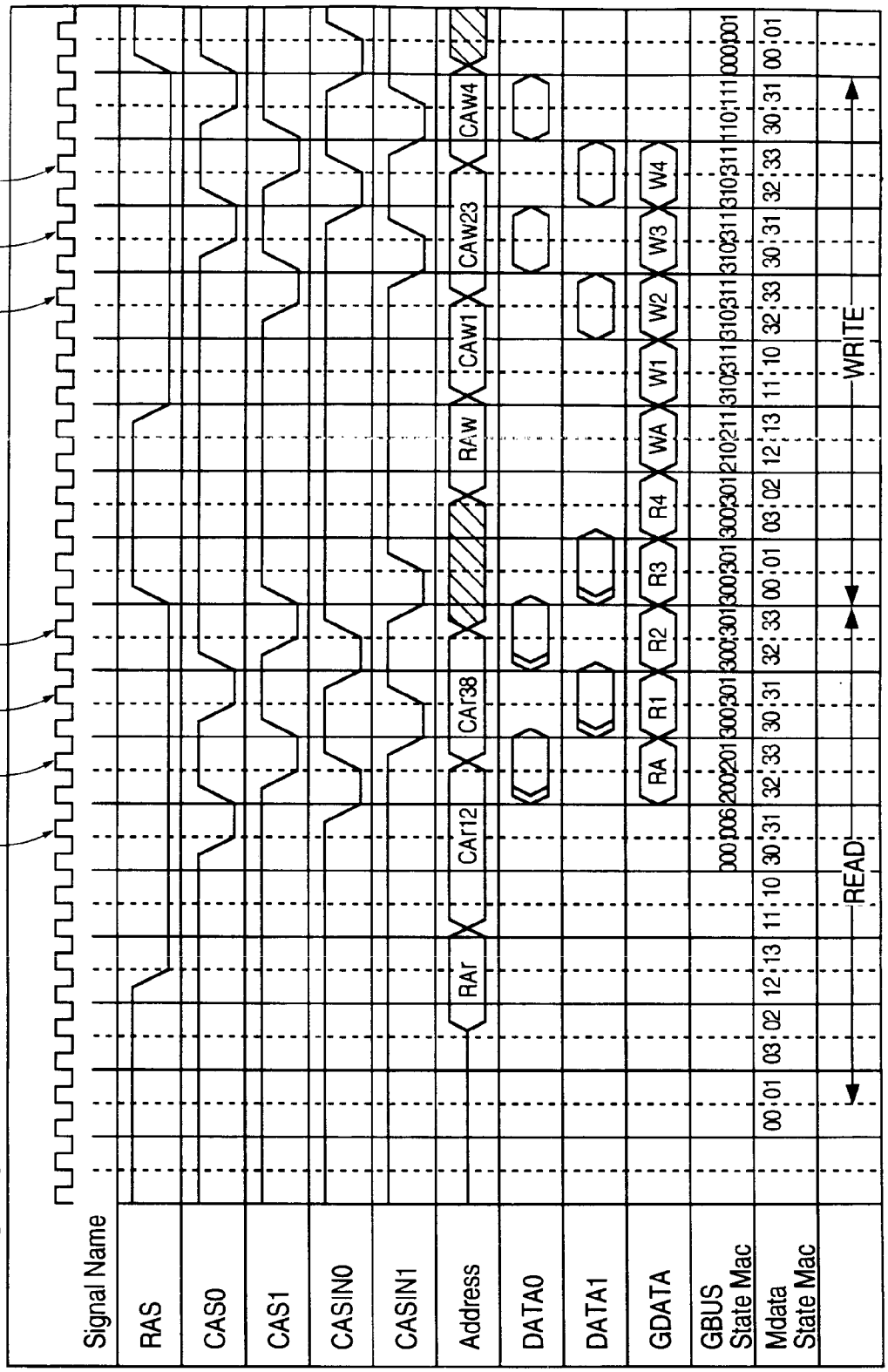
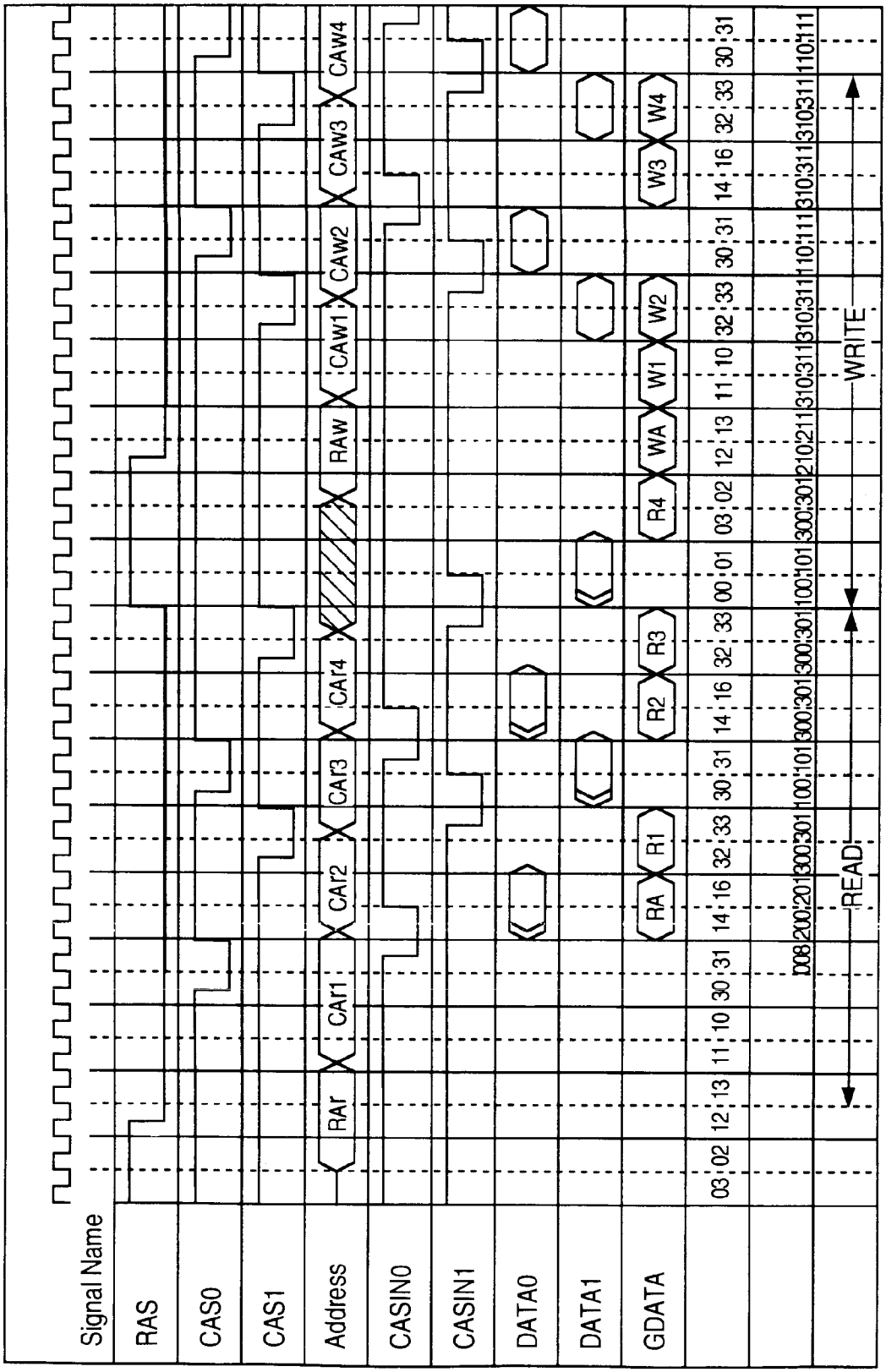

Signal Name
RAS
CAS0
CAS1
CAS\N0
CAS\N1
Address
DATA0
DATA1
GDATA
GBUS State Mac
Mdata State Mac
t1
t2
t3
t4
t5
t6
t7
RAr
CAr12
CAr38
RAW
CAW1
CAW23
CAW4
RA
R1
R2
R3
R4
WA
W1
W2
W3
W4
READ
WRITE

FIG. 9C


Signal Name
RAS
CAS0
CAS1
Address
CASIN0
CASIN1
DATA0
DATA1
GDATA
RAr
CAr1
CAr2
CAr3
CAr4
RAw
CAW1
CAW2
CAW3
CAW4
RA
R1
R2
R3
R4
WA
W1
W2
W3
W4
READ
WRITE

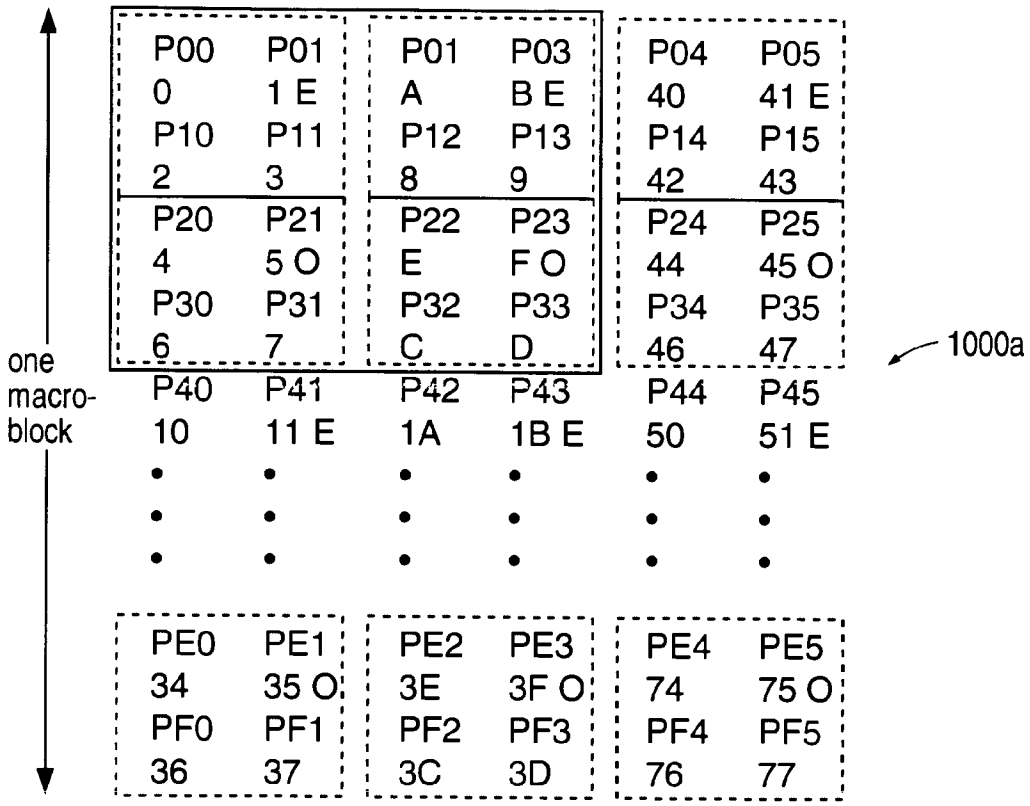

P00 P01 P01 P03 P04 P05
0 1 E A B E 40 41 E
P10 P11 P12 P13 P14 P15
2 3 8 9 42 43
P20 P21 P22 P23 P24 P25
4 5 O E F O 44 45 O
P30 P31 P32 P33 P34 P35
6 7 C D 46 47
P40 P41 P42 P43 P44 P45
10 11 E 1A 1B E 50 51 E
PE0 PE1 PE2 PE3 PE4 PE5
34 35 O 3E 3F O 74 75 O
PF0 PF1 PF2 PF3 PF4 PF5
36 37 3C 3D 76 77
one macro-block
1000a

FIG. 10A

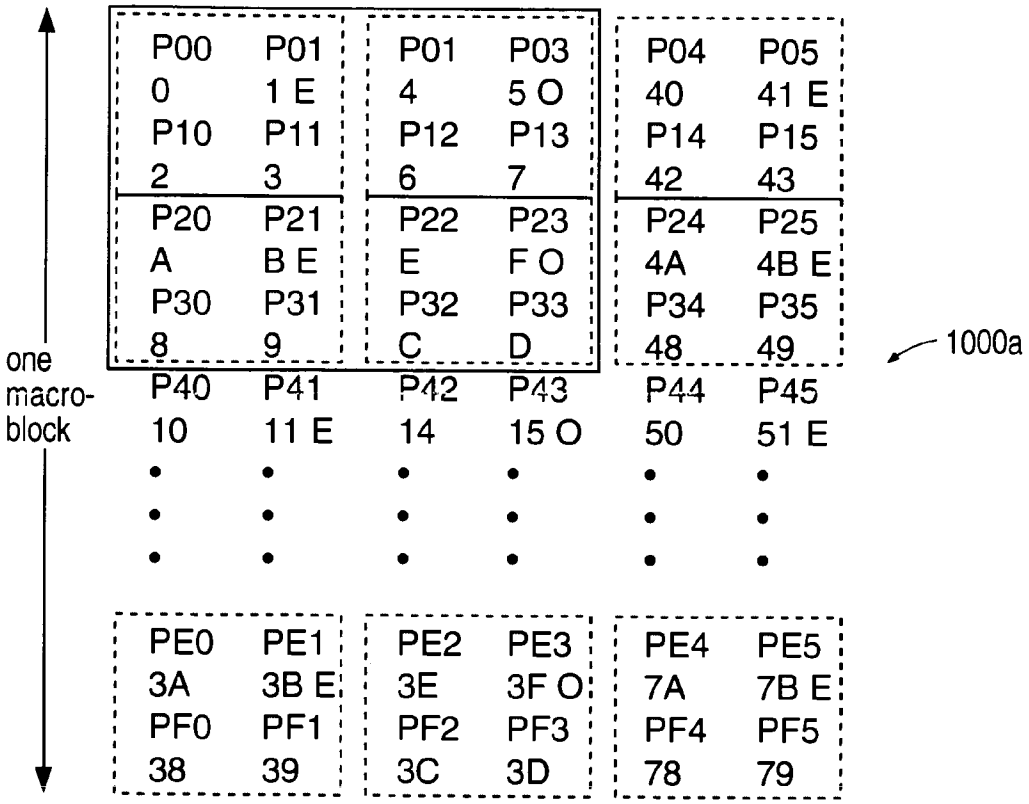

P00 P01 P01 P03 P04 P05
0 1 E 4 5 O 40 41 E
P10 P11 P12 P13 P14 P15
2 3 6 7 42 43
P20 P21 P22 P23 P24 P25
A B E E F O 4A 4B E
P30 P31 P32 P33 P34 P35
8 9 C D 48 49
P40 P41 P42 P43 P44 P45
10 11 E 14 15 O 50 51 E
PE0 PE1 PE2 PE3 PE4 PE5
3A 3B E 3E 3F O 7A 7B E
PF0 PF1 PF2 PF3 PF4 PF5
38 39 3C 3D 78 79
one macro-block
1000a

FIG. 10B

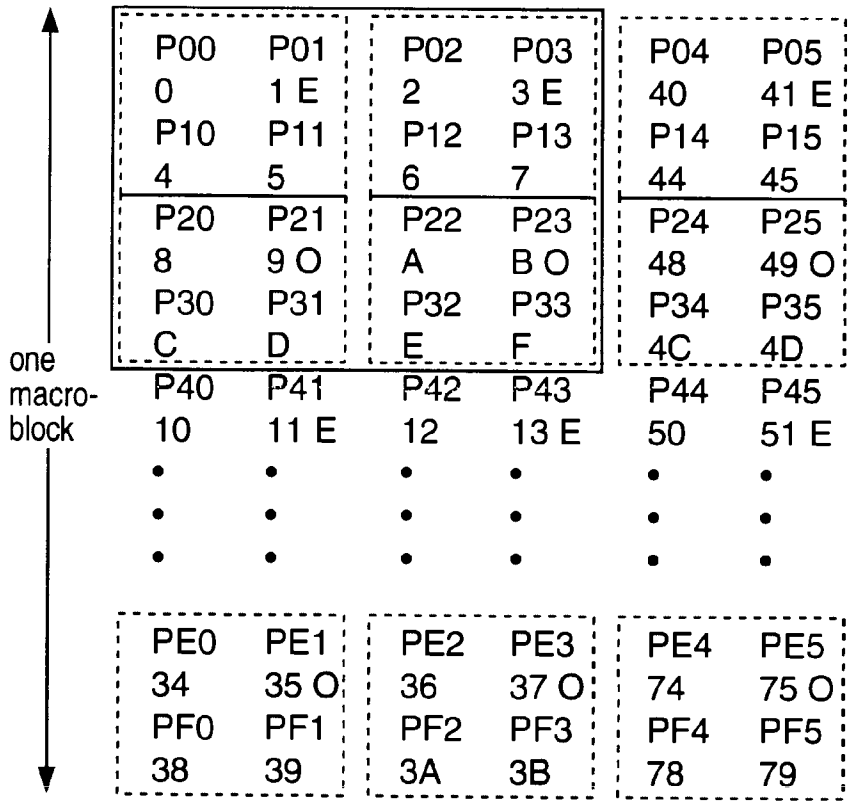

one macro-block
P00 P01 P02 P03 P04 P05
0 1 E 2 3 E 40 41 E
P10 P11 P12 P13 P14 P15
4 5 6 7 44 45
P20 P21 P22 P23 P24 P25
8 9 O A B O 48 49 O
P30 P31 P32 P33 P34 P35
C D E F 4C 4D
P40 P41 P42 P43 P44 P45
10 11 E 12 13 E 50 51 E
PE0 PE1 PE2 PE3 PE4 PE5
34 35 O 36 37 O 74 75 O
PF0 PF1 PF2 PF3 PF4 PF5
38 39 3A 3B 78 79

FIG. 10C

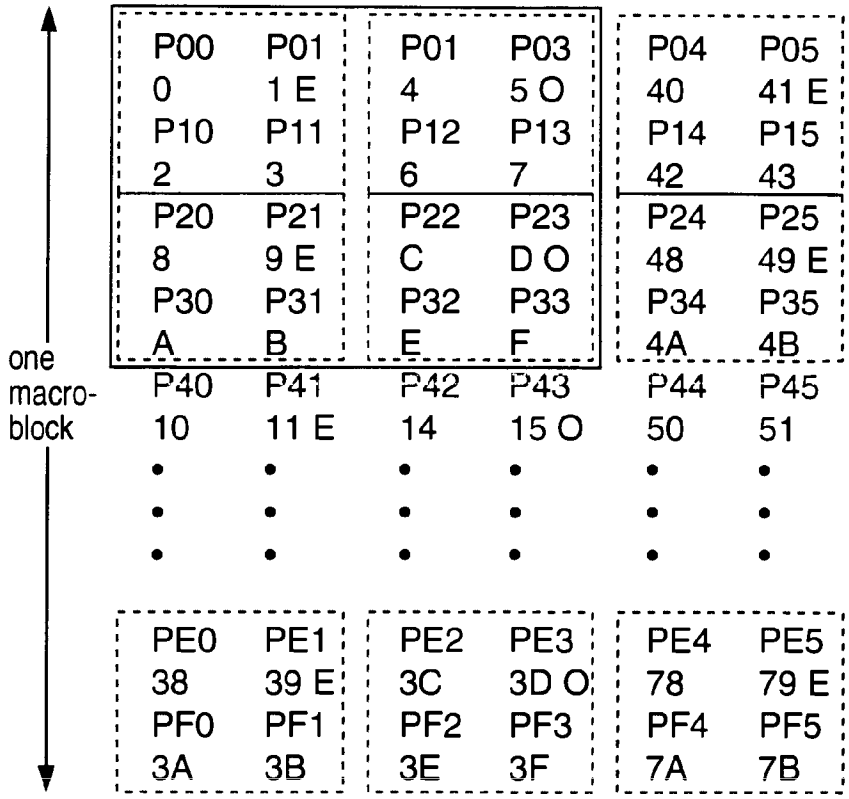

one
macro-
block
P00 P01 P01 P03 P04 P05
0 1 E 4 5 O 40 41 E
P10 P11 P12 P13 P14 P15
2 3 6 7 42 43
P20 P21 P22 P23 P24 P25
8 9 E C D O 48 49 E
P30 P31 P32 P33 P34 P35
A B E F 4A 4B
P40 P41 P42 P43 P44 P45
10 11 E 14 15 O 50 51
PE0 PE1 PE2 PE3 PE4 PE5
38 39 E 3C 3D O 78 79 E
PF0 PF1 PF2 PF3 PF4 PF5
3A 3B 3E 3F 7A 7B

FIG. 10D

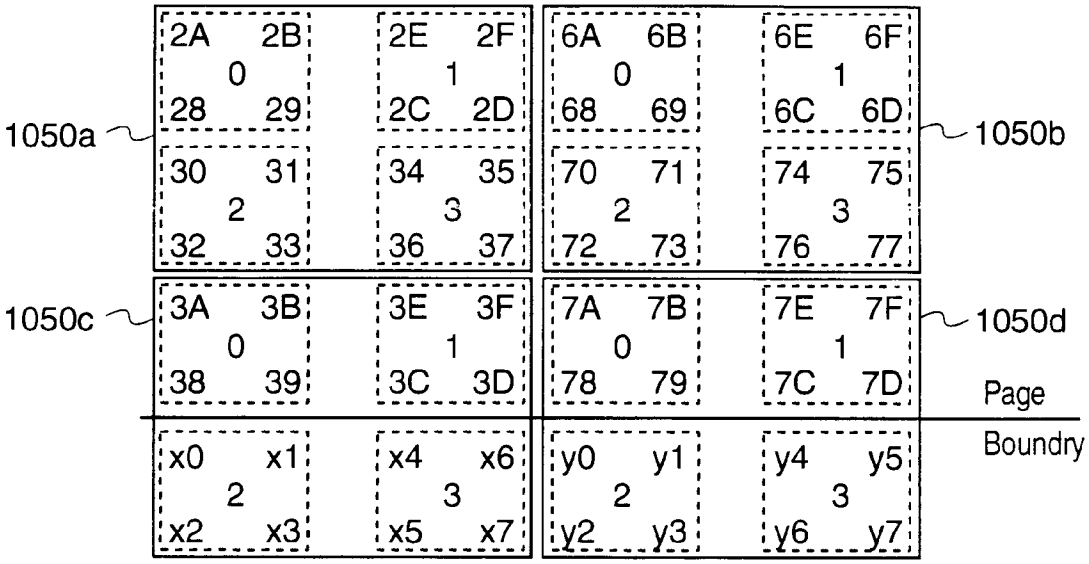

2A 2B
0
28 29
2E 2F
1
2C 2D
6A 6B
0
68 69
6E 6F
1
6C 6D
1050a
1050b
30 31
2
32 33
34 35
3
36 37
70 71
2
72 73
74 75
3
76 77
1050c
3A 3B
0
38 39
3E 3F
1
3C 3D
7A 7B
0
78 79
7E 7F
1
7C 7D
1050d
Page
Boundry
x0 x1
2
x2 x3
x4 x6
3
x5 x7
y0 y1
2
y2 y3
y4 y5
3
y6 y7

FIG. 10E

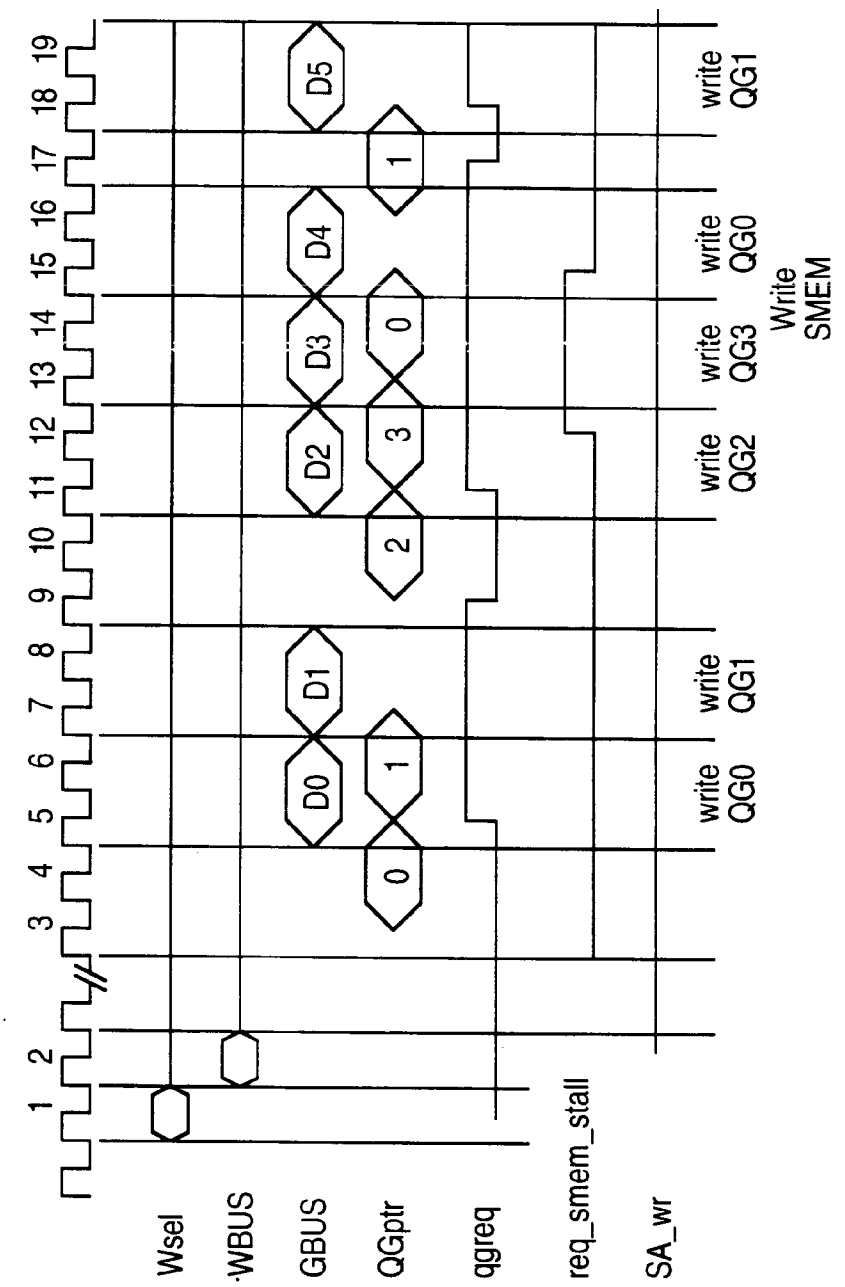

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
Wsel
WBUS
GBUS
QGptr
qgreq
req_smem_stall
SA_wr
D0
D1
D2
D3
D4
D5
0
1
2
3
0
1
write QG0
write QG1
write QG2
write QG3
write QG0
write QG1
Write SMEM

FIG. 11A

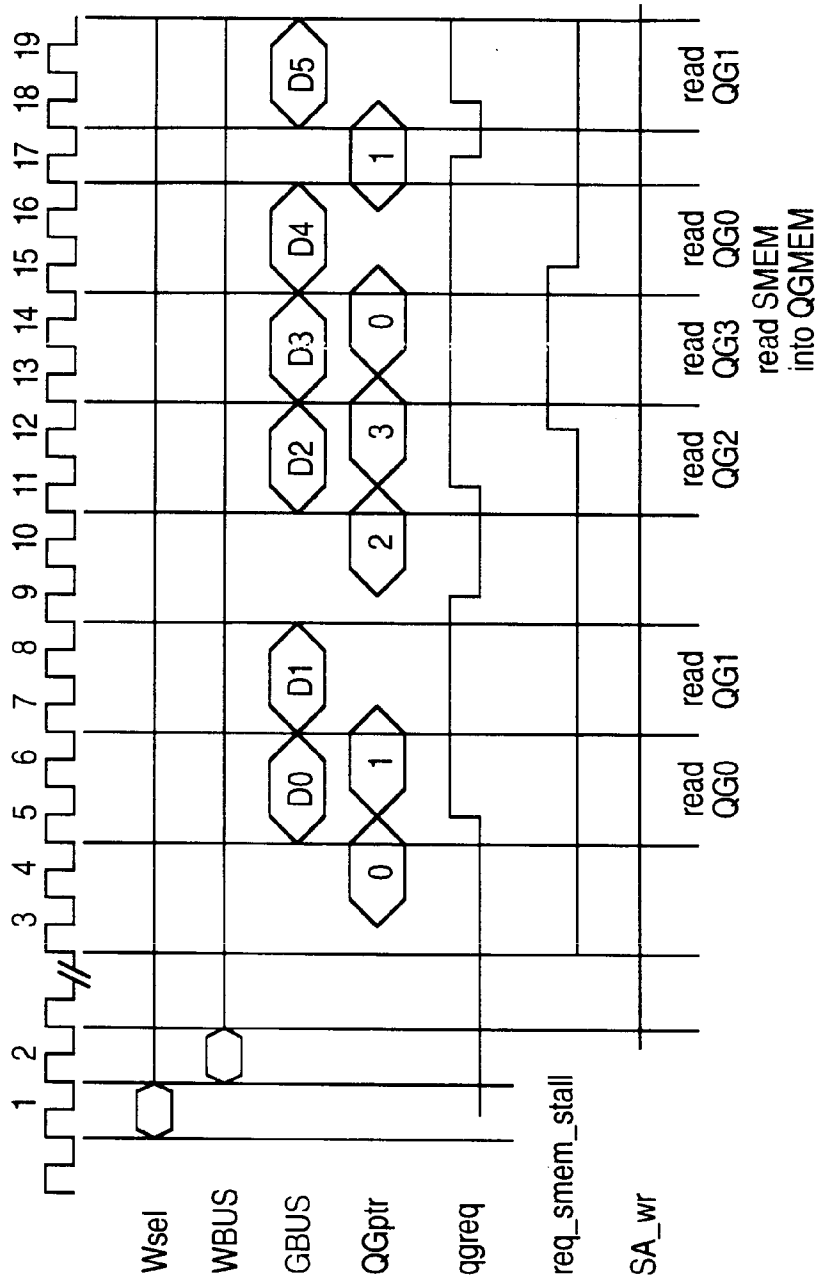

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
Wsel
WBUS
GBUS
QGptr
qgreq
req_smem_stall
SA_wr
D0
D1
D2
D3
D4
D5
0
1
2
3
0
1
read QG0
read QG1
read QG2
read QG3
read QG0
read QG1
read SMEM into QGMEM

FIG. 11B

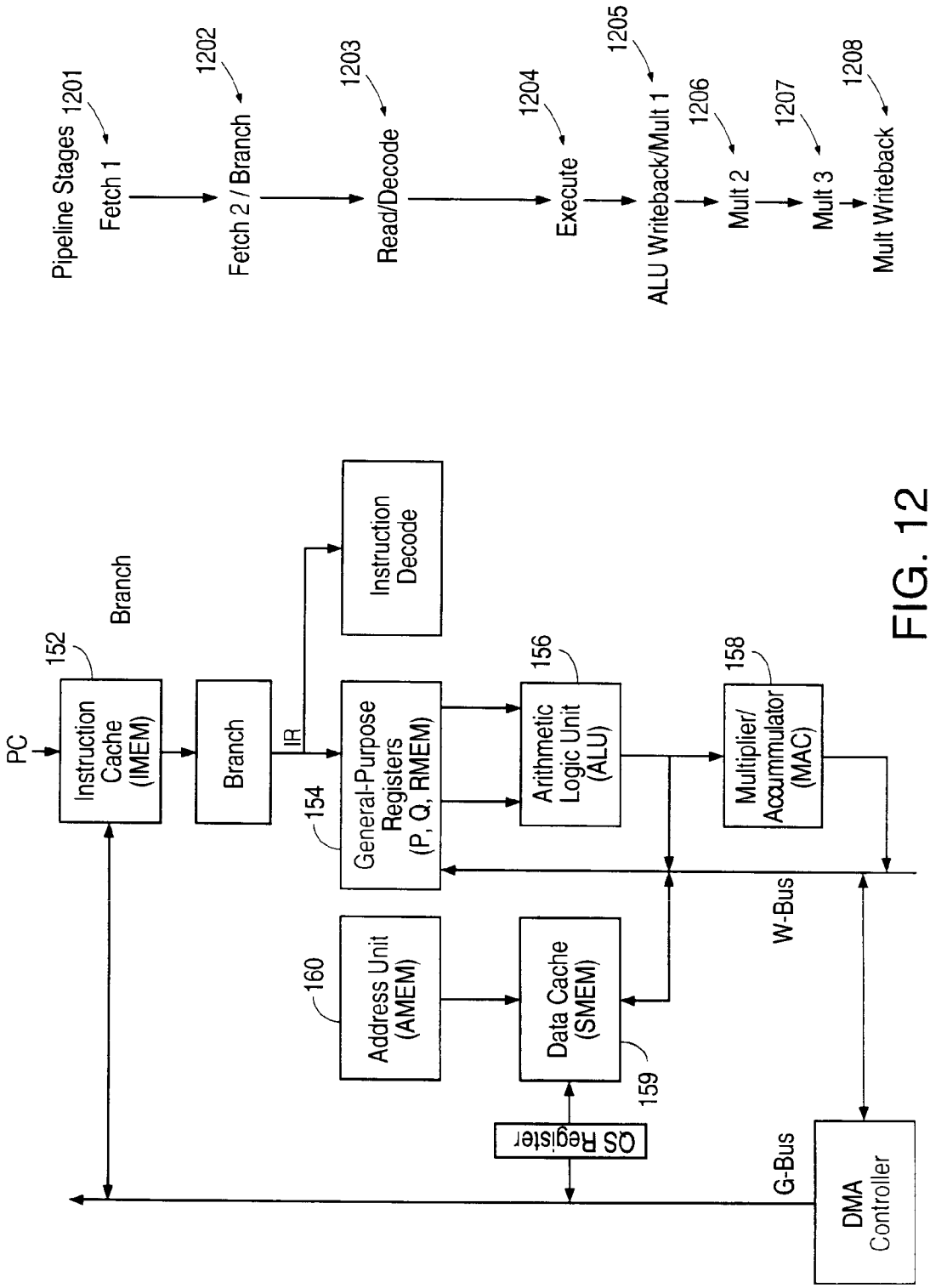

Pipeline Stages
1201
Fetch 1
1202
Fetch 2 / Branch
1203
Read/Decode
1204
Execute
1205
ALU Writeback/Mult 1
1206
Mult 2
1207
Mult 3
1208
Mult Writeback
PC
152
Instruction Cache (IMEM)
Branch
Branch
IR
Instruction Decode
154
General-Purpose Registers (P, Q, RMEM)
156
Arithmetic Logic Unit (ALU)
158
Multiplier/ Accummulator (MAC)
160
Address Unit (AMEM)
Data Cache (SMEM)
159
W-Bus
QS Register
G-Bus
DMA Controller

FIG. 12

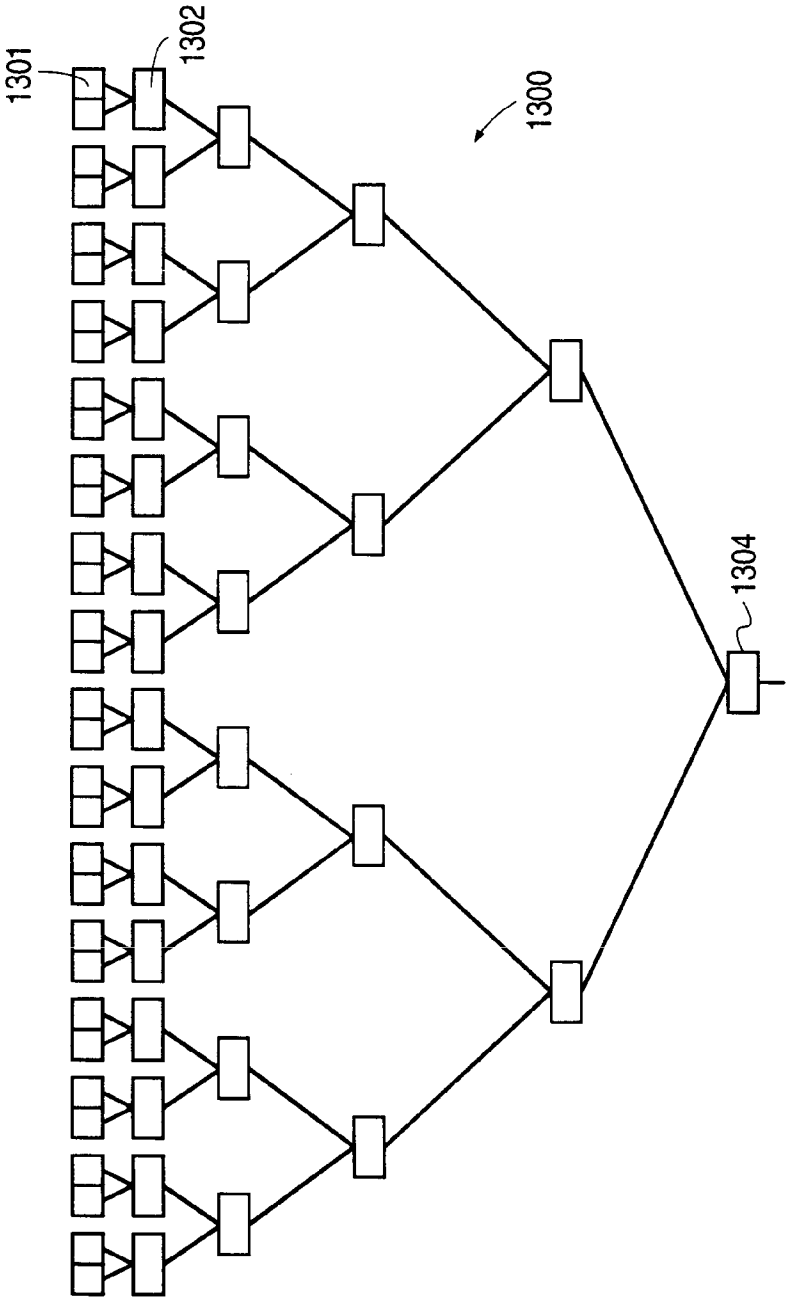


FIG. 13A

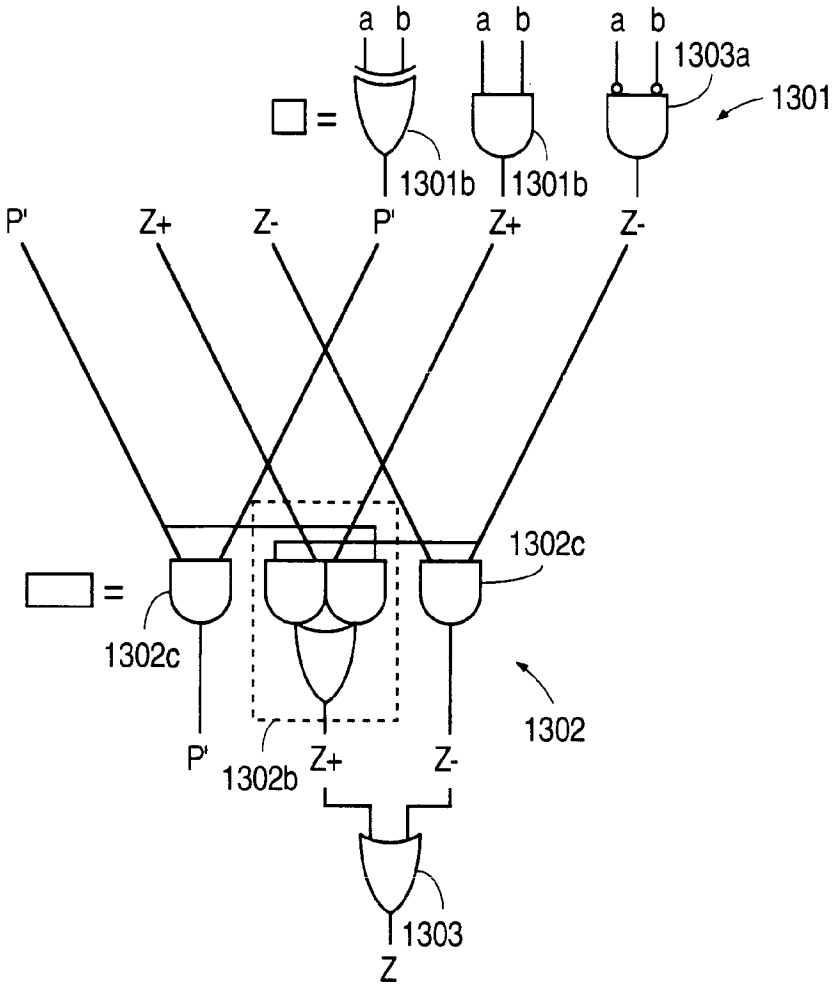

a b
a b
a b
1303a
1301
=
1301b
1301b
P'
Z+
Z-
P'
Z+
Z-
1302c
=
1302c
1302
P'
1302b
Z+
Z-
1303
Z

FIG. 13B

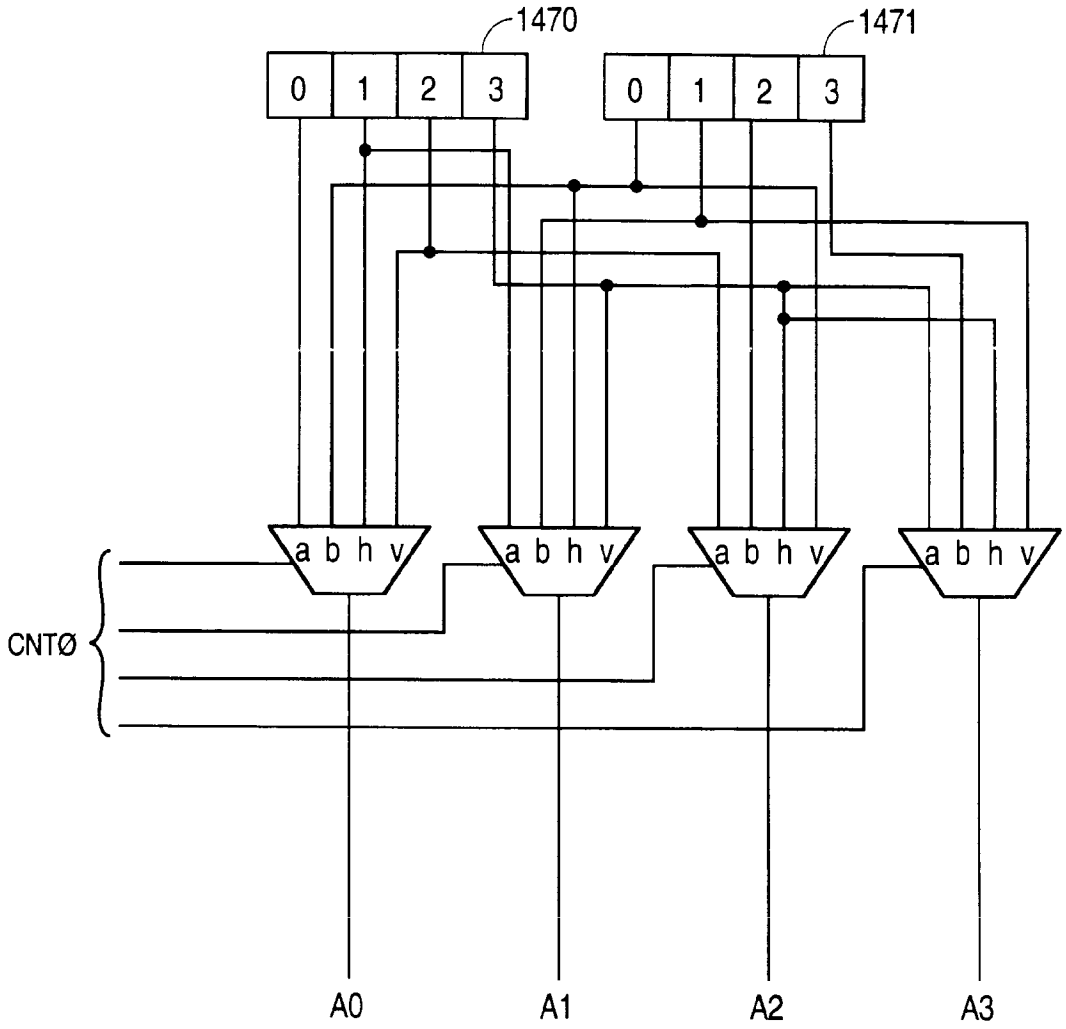


FIG. 14A

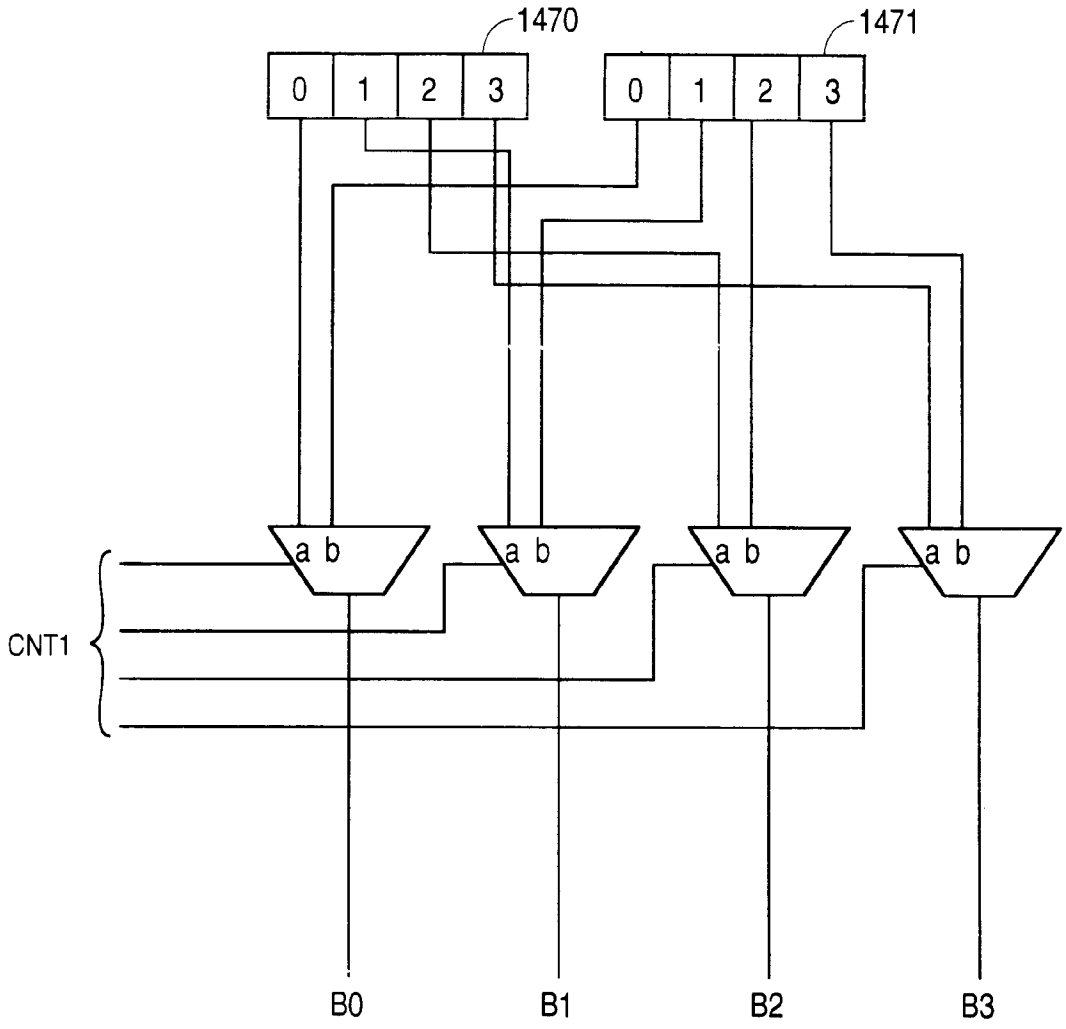


FIG. 14B

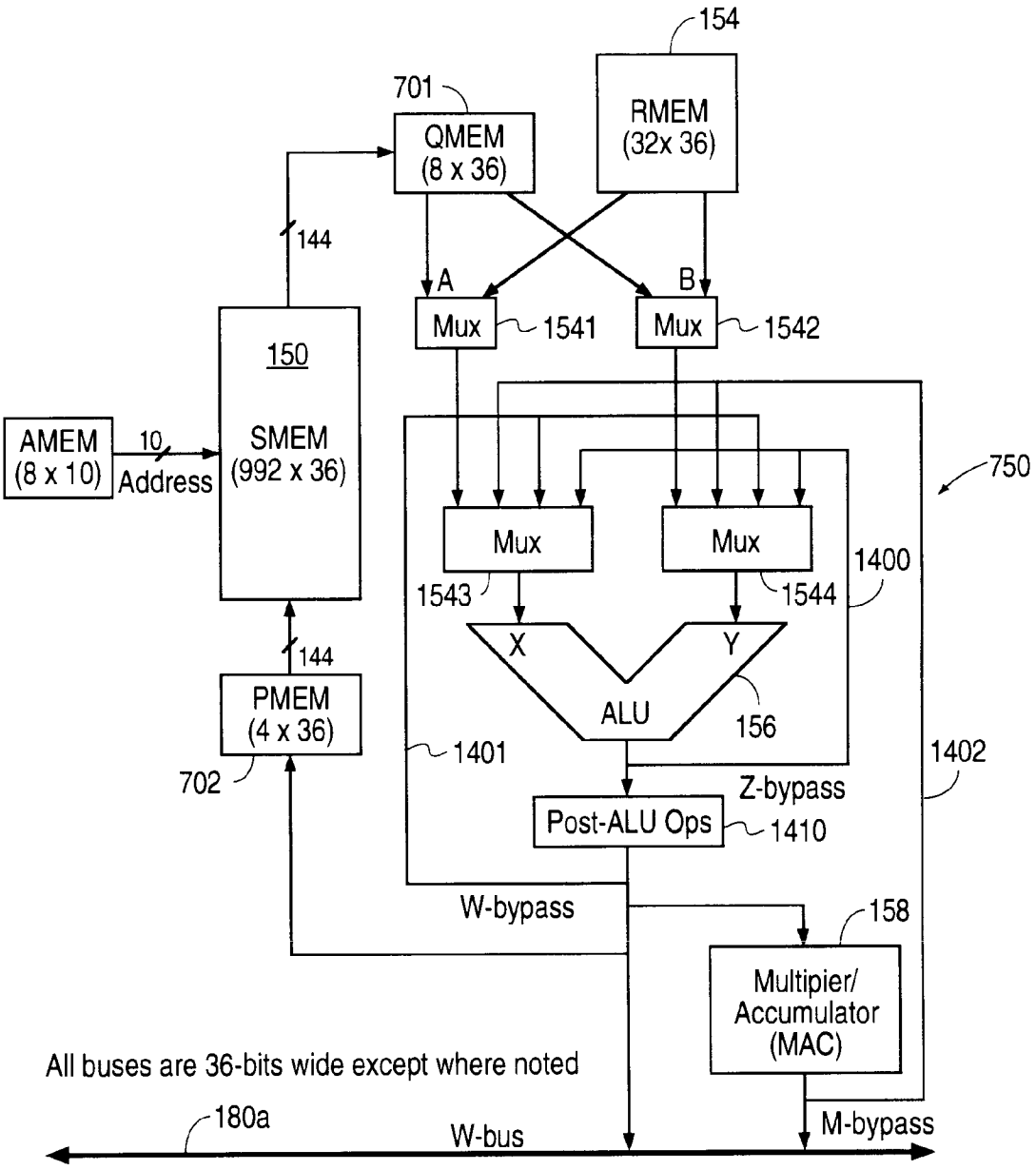

154
701
QMEM
(8 x 36)
RMEM
(32x 36)
144
A
B
Mux
1541
Mux
1542
150
AMEM
(8 x 10)
10
Address
SMEM
(992 x 36)
750
Mux
Mux
1400
1543
1544
X
Y
144
PMEM
(4 x 36)
ALU
156
1401
1402
702
Z-bypass
Post-ALU Ops
1410
W-bypass
158
Multipier/
Accumulator
(MAC)
All buses are 36-bits wide except where noted
180a
W-bus
M-bypass

FIG. 15A

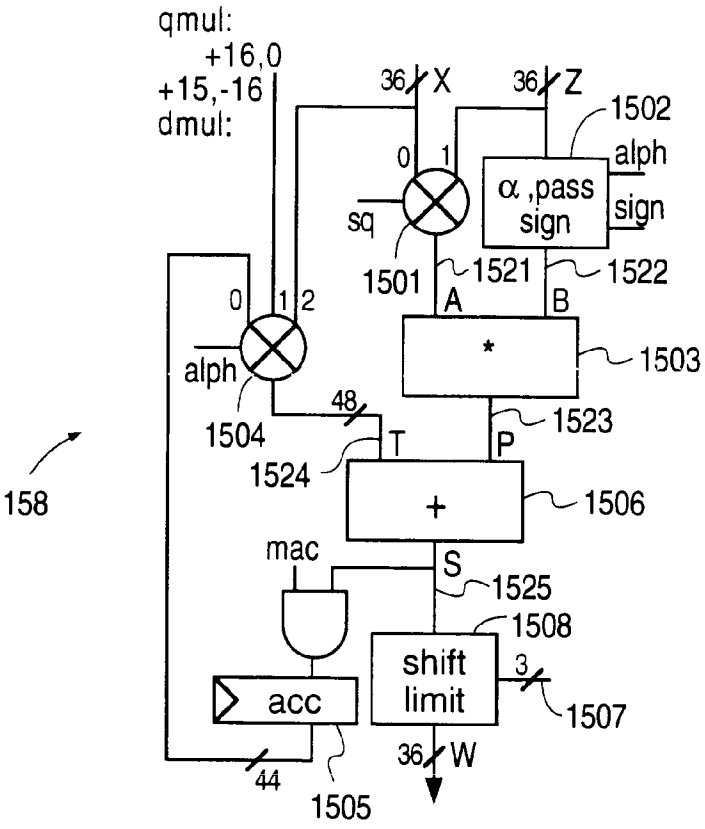

qmul:
+16,0
+15,-16
dmul:
36
X
36
Z
1502
alph
sign
0
1
sq
α ,pass
sign
1501
1521
1522
A
B
0
1
2
alph
*
1503
48
1504
T
P
1523
1524
+
1506
158
mac
S
1525
1508
shift
limit
3
1507
acc
36
W
44
1505

FIG. 15B

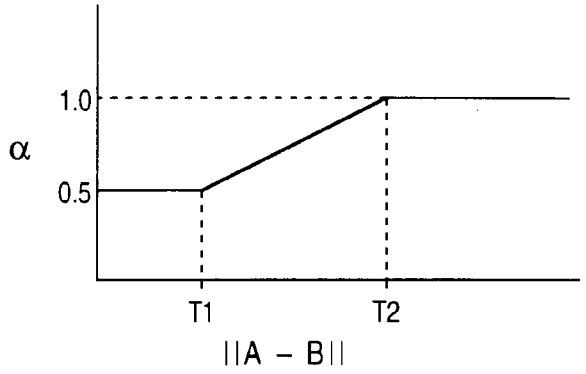


FIG. 15C(i)

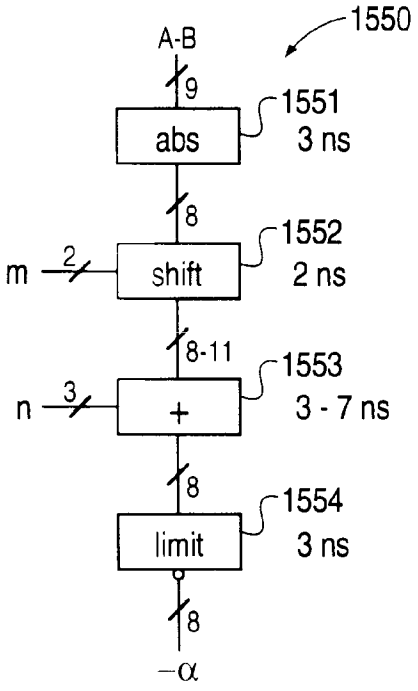
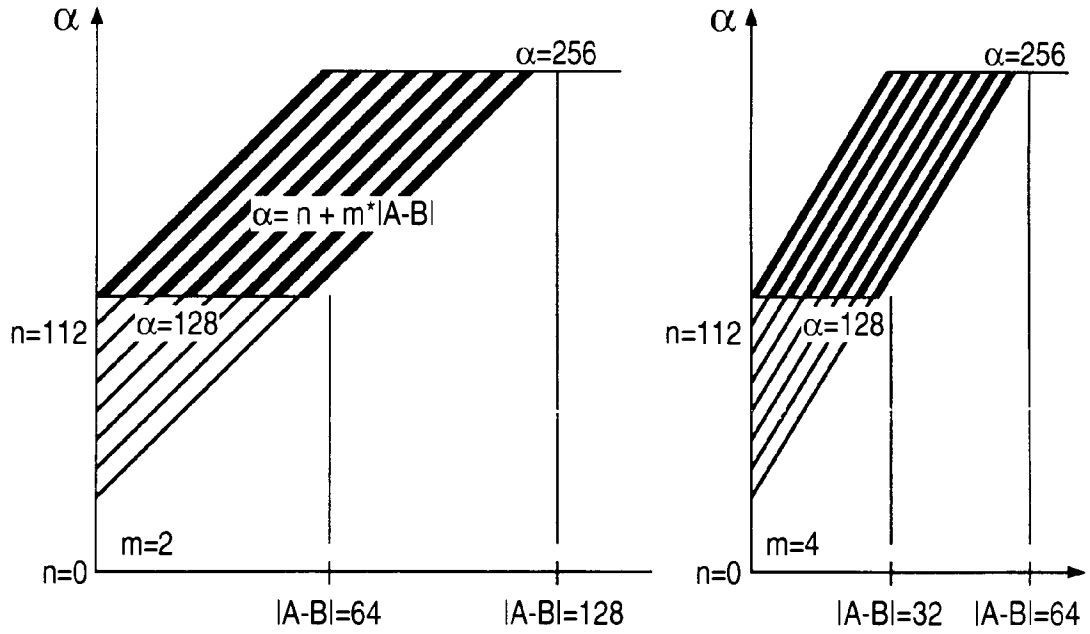


FIG. 15C(ii)



23

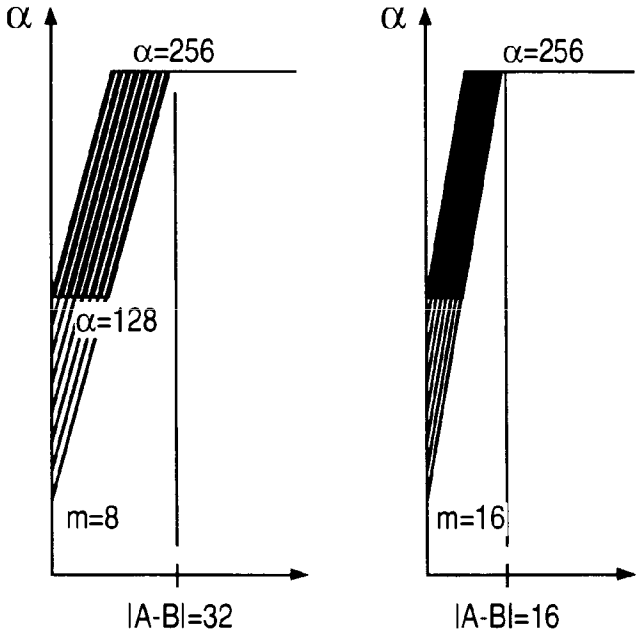
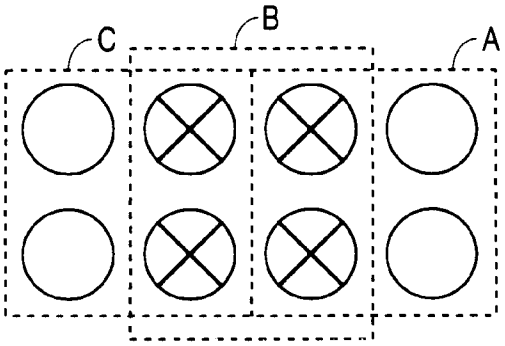
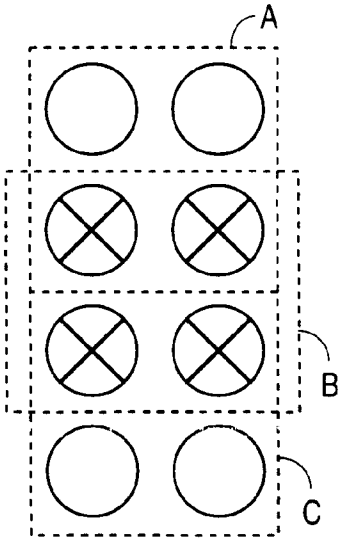


FIG. 15C(iii)



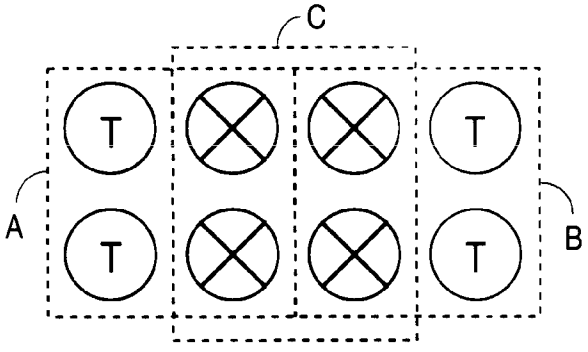
HOFF

FIG. 15D(i)



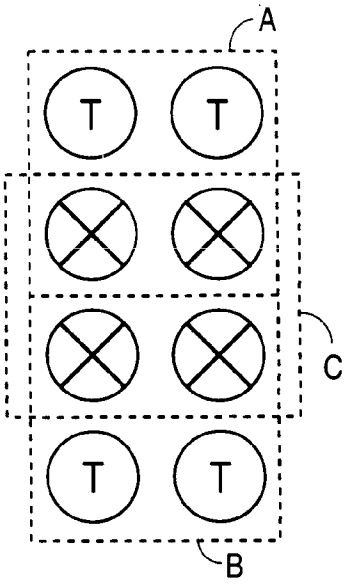
VOFF

FIG. 15D(ii)



HSHRINK

FIG. 15D(iii)



VSHRINK

FIG. 15D(iv)

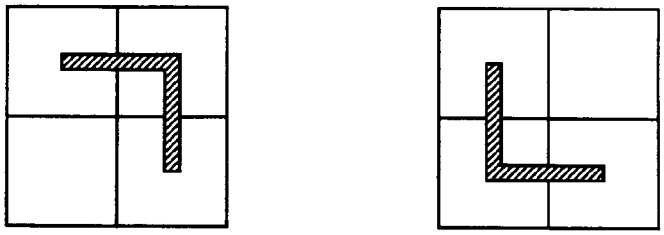


FIG. 15E

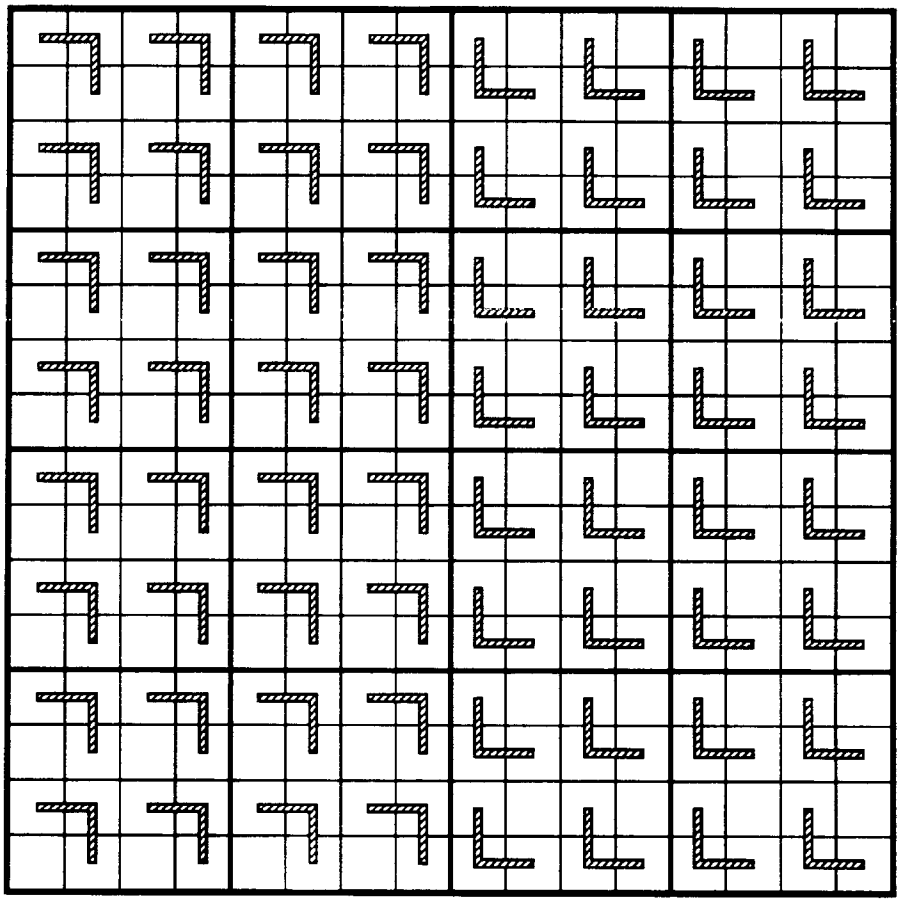


FIG. 15F

KEY TO
FIG. 16A

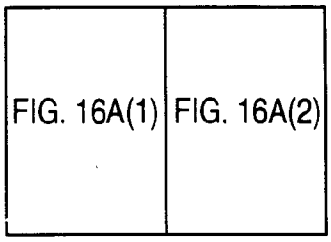
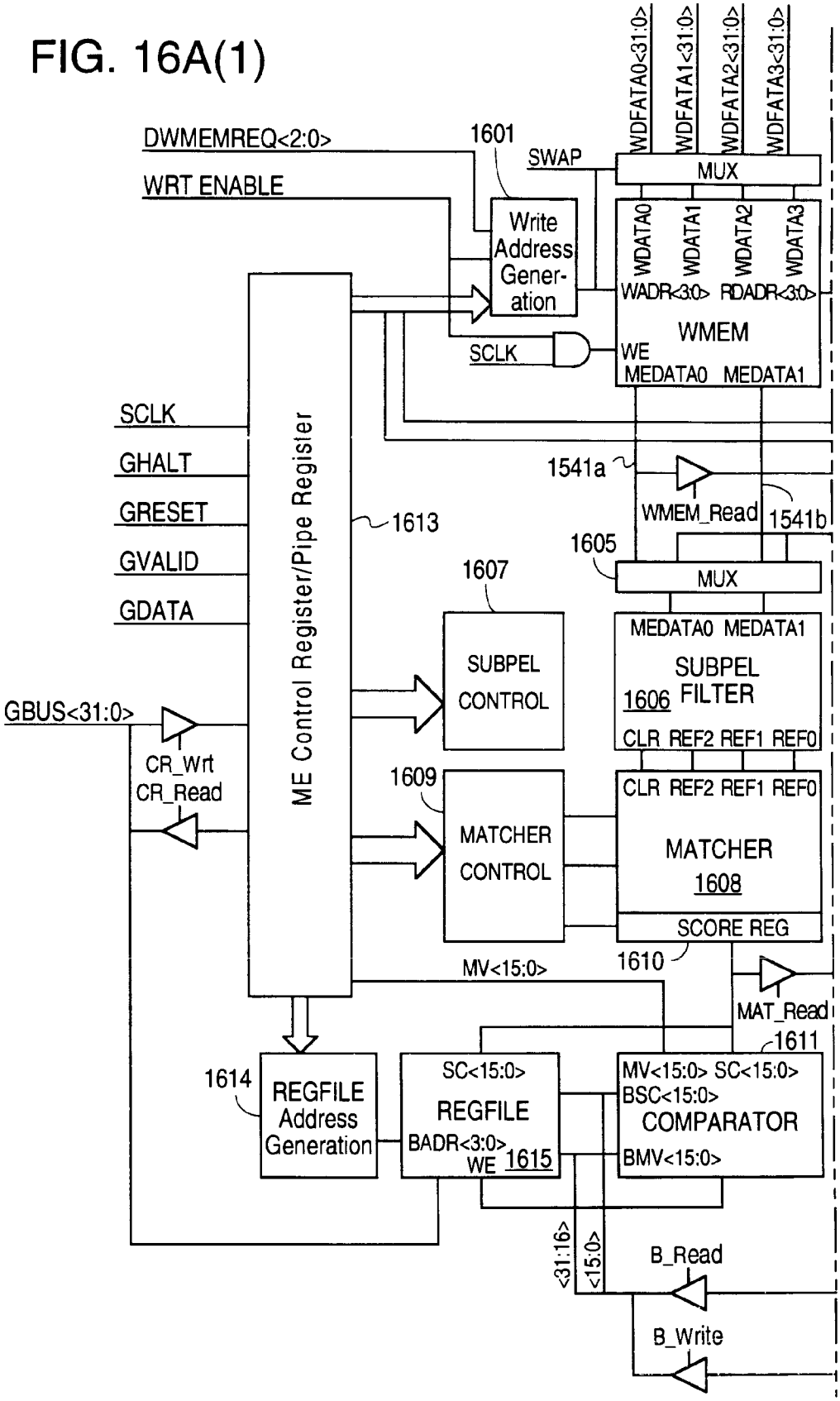


FIG. 16A

FIG. 16A(1)


WDFATA0<31:0>
WDFATA1<31:0>
WDFATA2<31:0>
WDFATA3<31:0>
DWMEMREQ<2:0>
1601
SWAP
MUX
WRT ENABLE
Write Address Gener-ation
WDATA0
WDATA1
WDATA2
WDATA3
WADR<3:0>
RDADR<3:0>
WMEM
SCLK
WE
MEDATA0 MEDATA1
SCLK
GHALT
GRESET
GVALID
GDATA
ME Control Register/Pipe Register
1613
1541a
WMEM_Read
1541b
1605
MUX
1607
SUBPEL CONTROL
MEDATA0 MEDATA1
SUBPEL FILTER
1606
CLR REF2 REF1 REF0
GBUS<31:0>
CR_Wrt
CR_Read
1609
MATCHER CONTROL
CLR REF2 REF1 REF0
MATCHER
1608
SCORE REG
1610
MV<15:0>
MAT_Read
1611
1614
REGFILE Address Generation
SC<15:0>
REGFILE
BADR<3:0>
WE 1615
MV<15:0> SC<15:0>
BSC<15:0>
COMPARATOR
BMV<15:0>
<31:16>
<15:0>
B_Read
B_Write

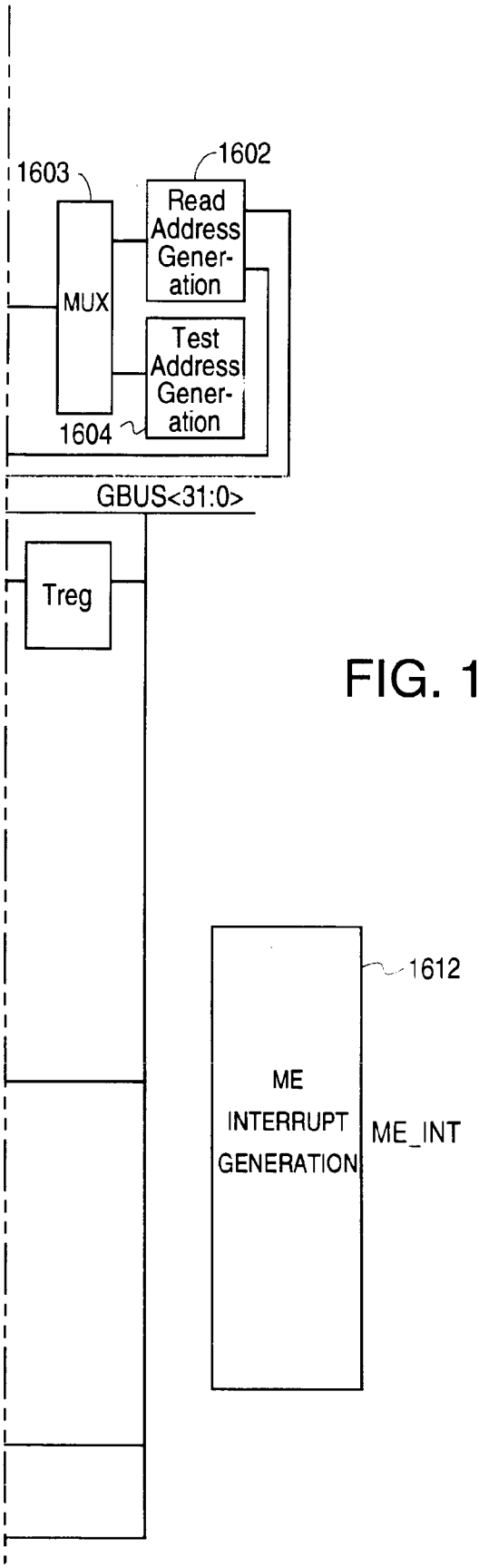

1603
1602
Read Address Gener-ation
MUX
Test Address Gener-ation
1604
GBUS<31:0>
Treg
1612
ME INTERRUPT GENERATION
ME_INT

FIG. 16A(2)

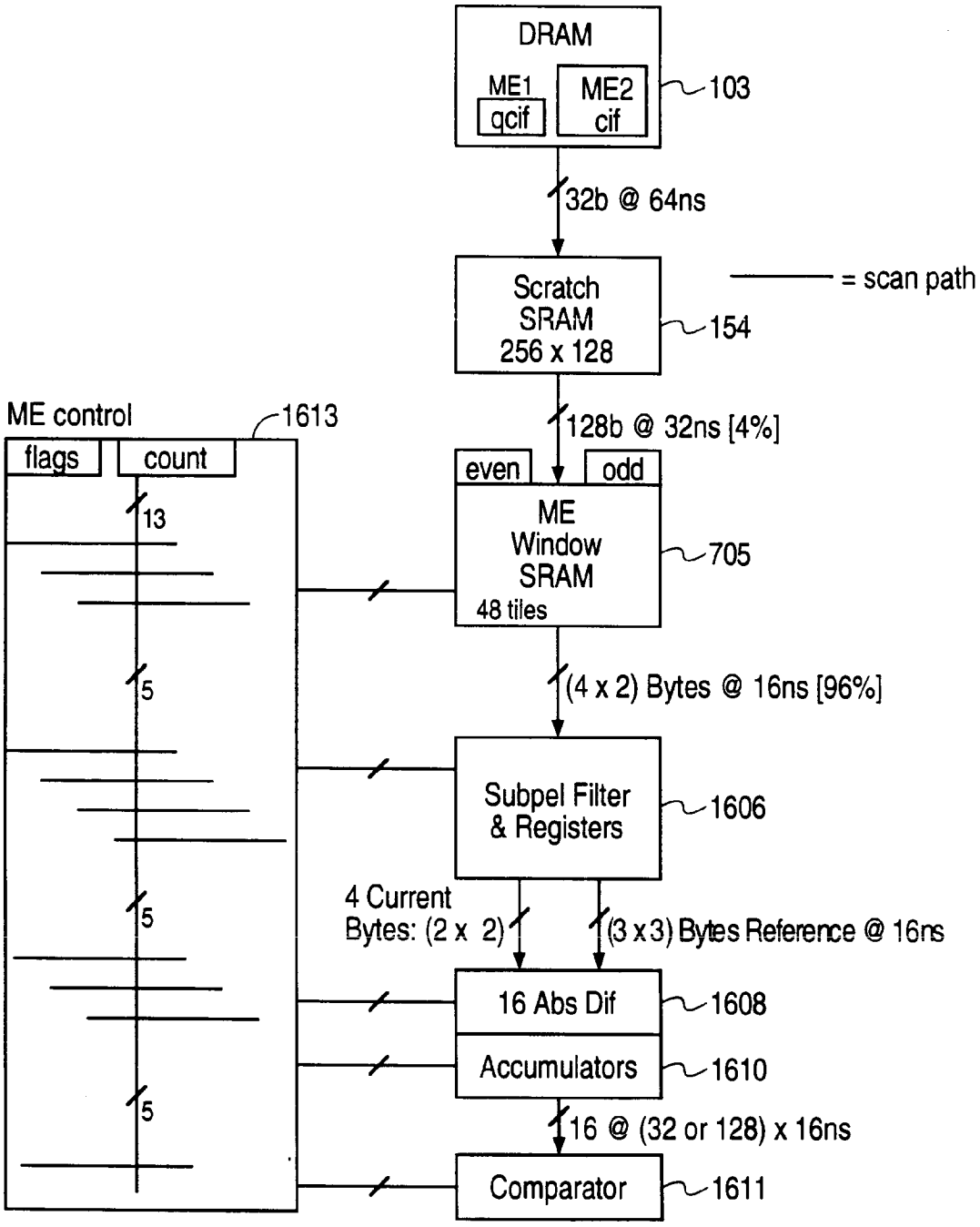

DRAM
ME1
qcif
ME2
cif
103
32b @ 64ns
= scan path
Scratch
SRAM
256 x 128
154
ME control
1613
flags
count
128b @ 32ns [4%]
even
odd
ME
Window
SRAM
48 tiles
705
13
5
5
5
(4 x 2) Bytes @ 16ns [96%]
Subpel Filter
& Registers
1606
4 Current
Bytes: (2 x 2)
(3 x 3) Bytes Reference @ 16ns
16 Abs Dif
1608
Accumulators
1610
16 @ (32 or 128) x 16ns
Comparator
1611

FIG. 16B

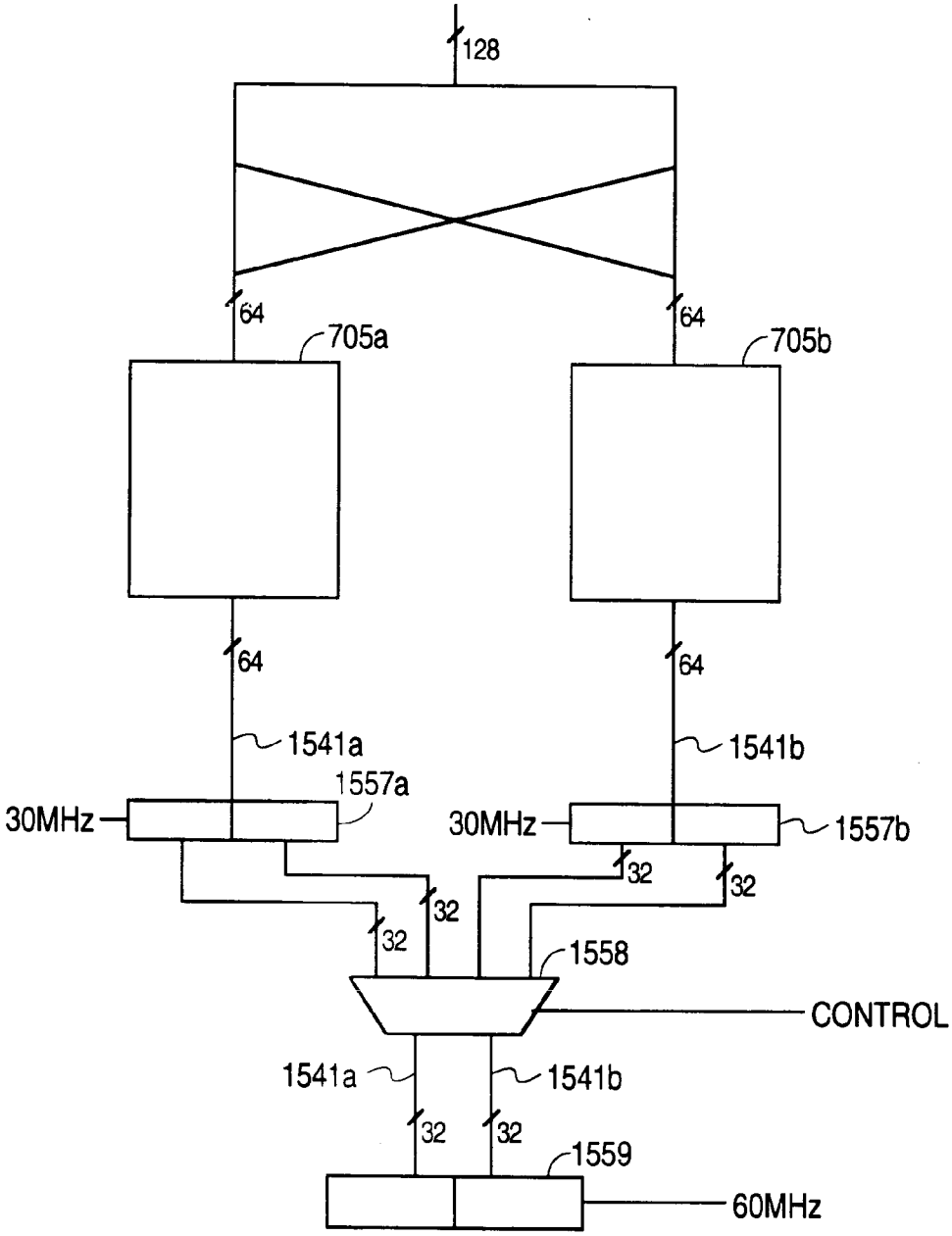

128
64
705a
64
705b
64
64
1541a
1541b
1557a
30MHz
30MHz
1557b
32
32
32
32
1558
CONTROL
1541a
1541b
32
32
1559
60MHz

FIG. 16C

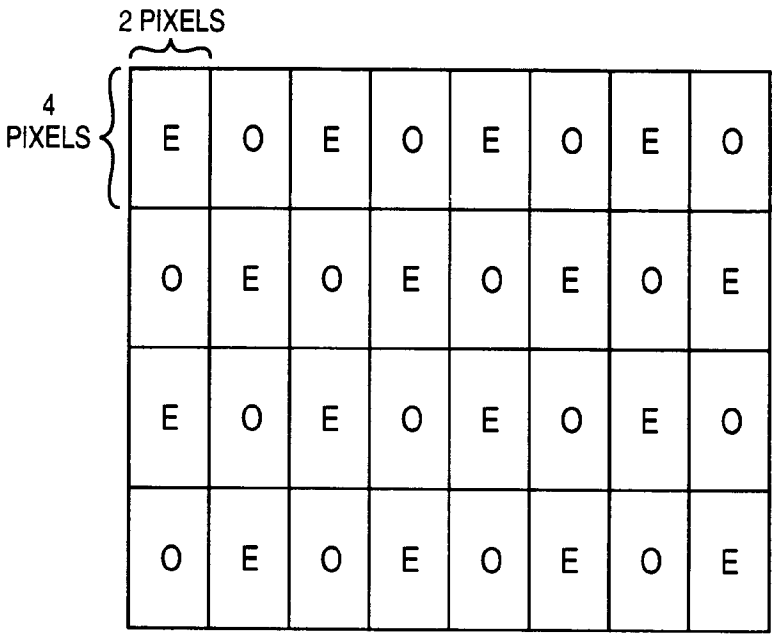


FIG. 16D

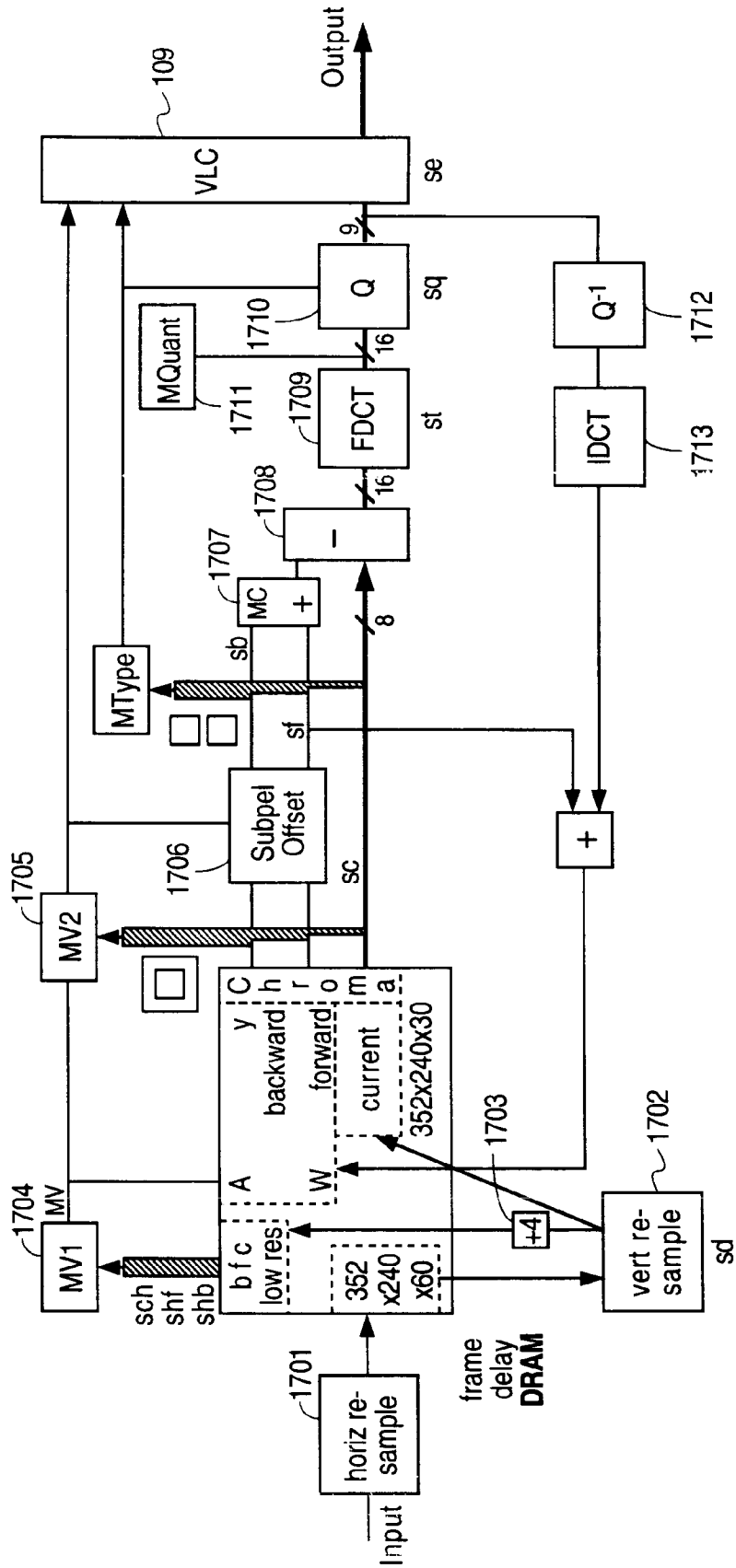

Output
109
VLC
se
9
Q
sq
16
MQuant
1710
1711
1709
FDCT
st
16
1708
−
1707
MC
+
8
sb
MType
sf
Subpel Offset
1706
sc
1705
MV2
1704
MV
MV1
sch
shf
shb
A
W
b f c
low res
352 x240 x60
Chroma
backward
forward
current
352x240x30
1703
+4
1702
vert re-sample
sd
frame delay DRAM
1701
horiz re-sample
Input
+
Q-1
1712
IDCT
1713

FIG. 17

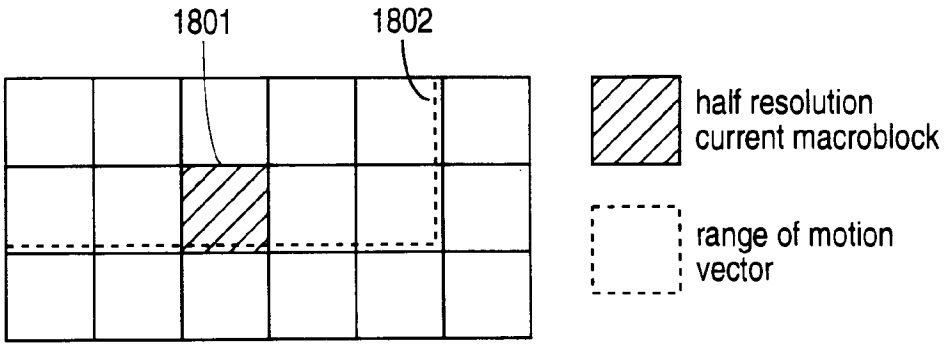


FIG. 18A

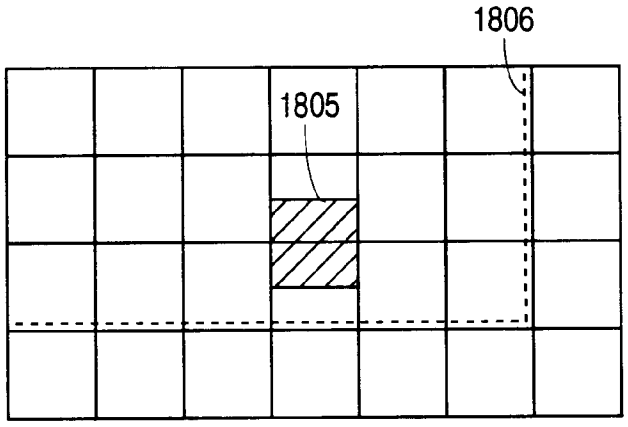


FIG. 18B

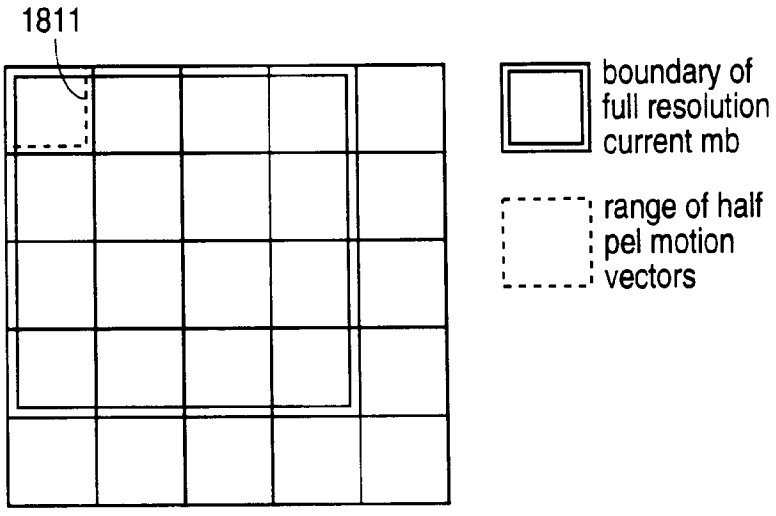


FIG. 18C

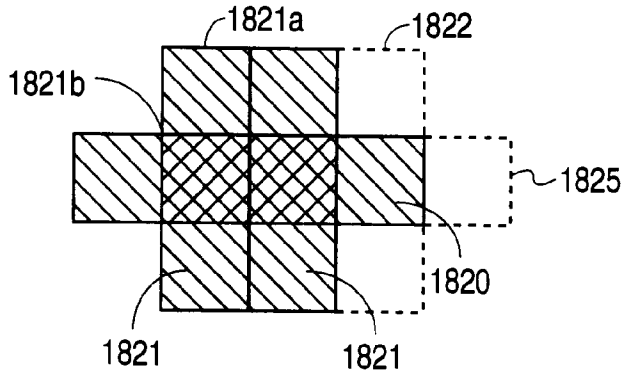


FIG. 18D

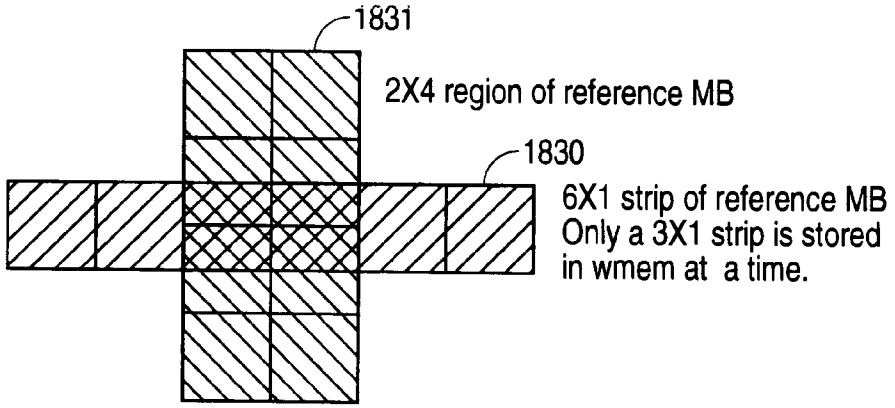


FIG. 18E

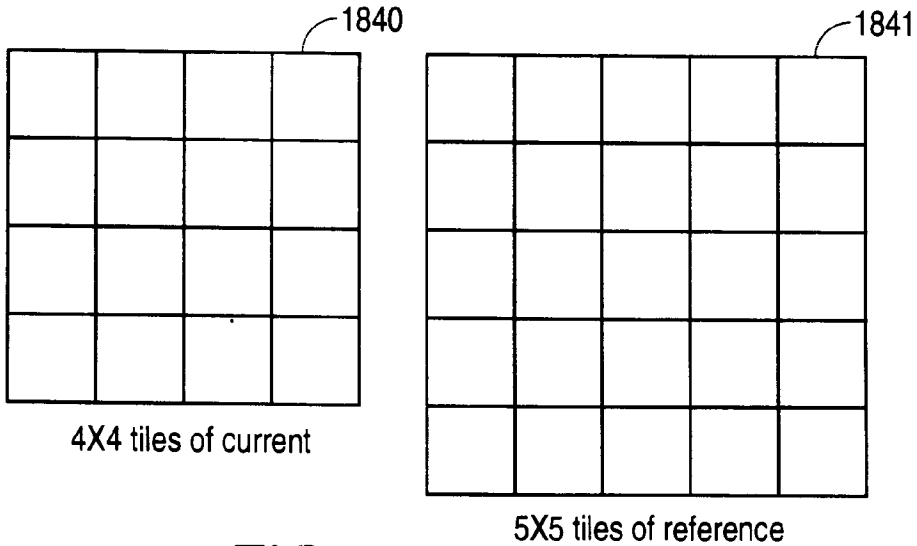


FIG. 18F

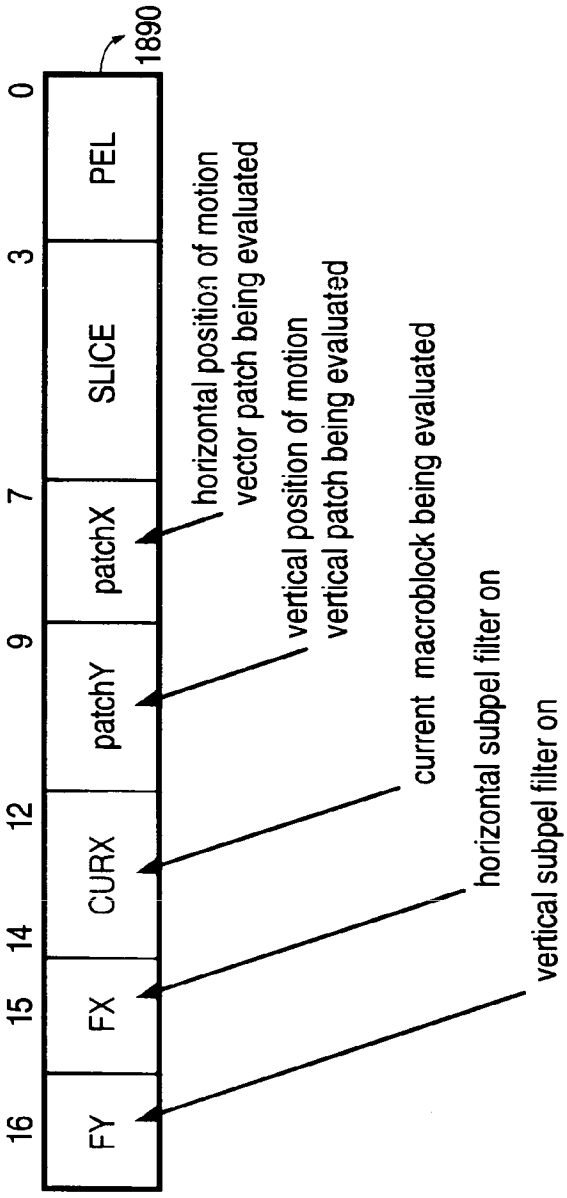

1890
0
3
7
9
12
14
15
16
PEL
SLICE
patchX
patchY
CURX
FX
FY
horizontal position of motion vector patch being evaluated
vertical position of motion vertical patch being evaluated
current macroblock being evaluated
horizontal subpel filter on
vertical subpel filter on

FIG. 18G

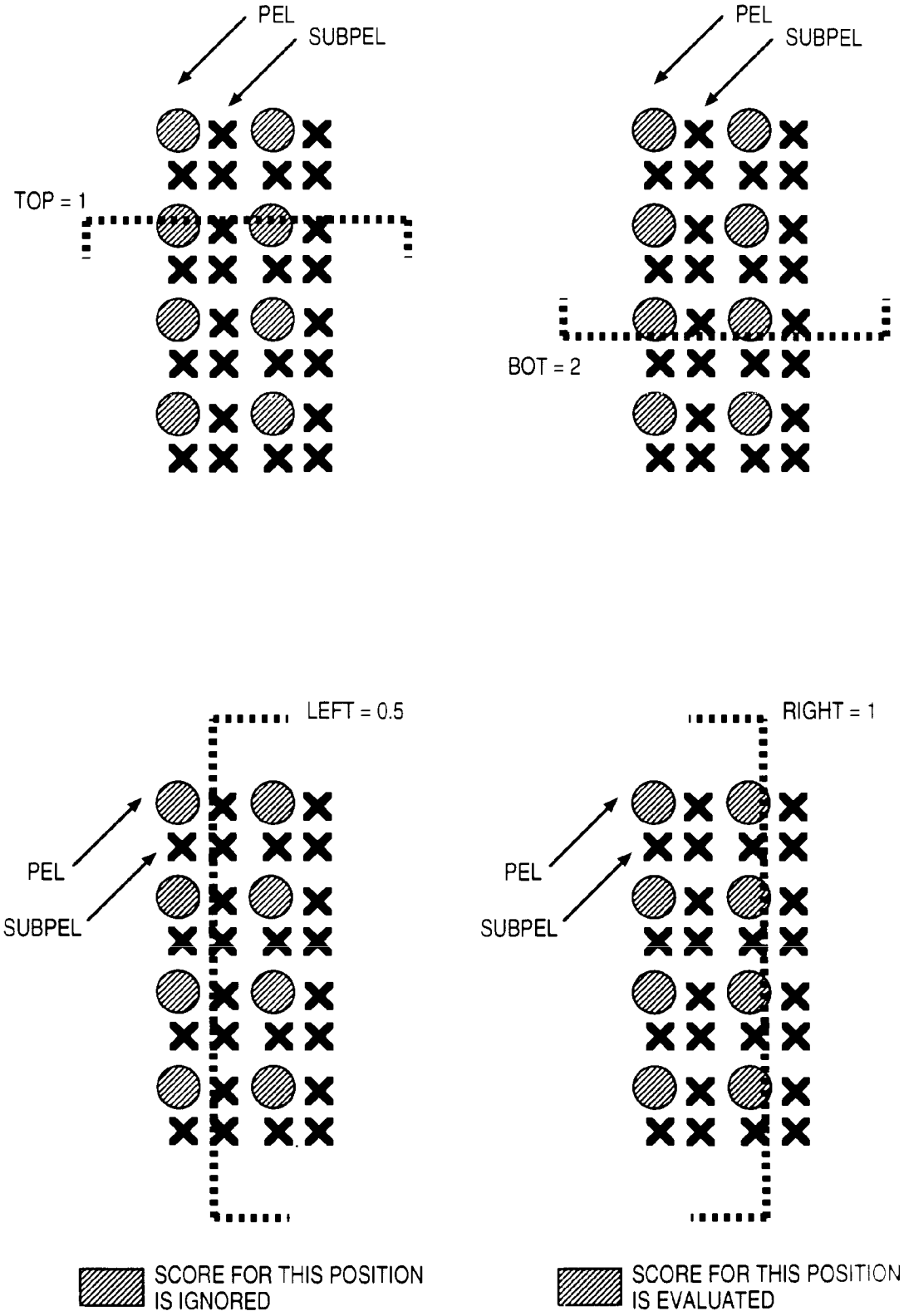

PEL
SUBPEL
TOP = 1
PEL
SUBPEL
BOT = 2
LEFT = 0.5
PEL
SUBPEL
RIGHT = 1
PEL
SUBPEL
SCORE FOR THIS POSITION IS IGNORED
SCORE FOR THIS POSITION IS EVALUATED

FIG. 18H

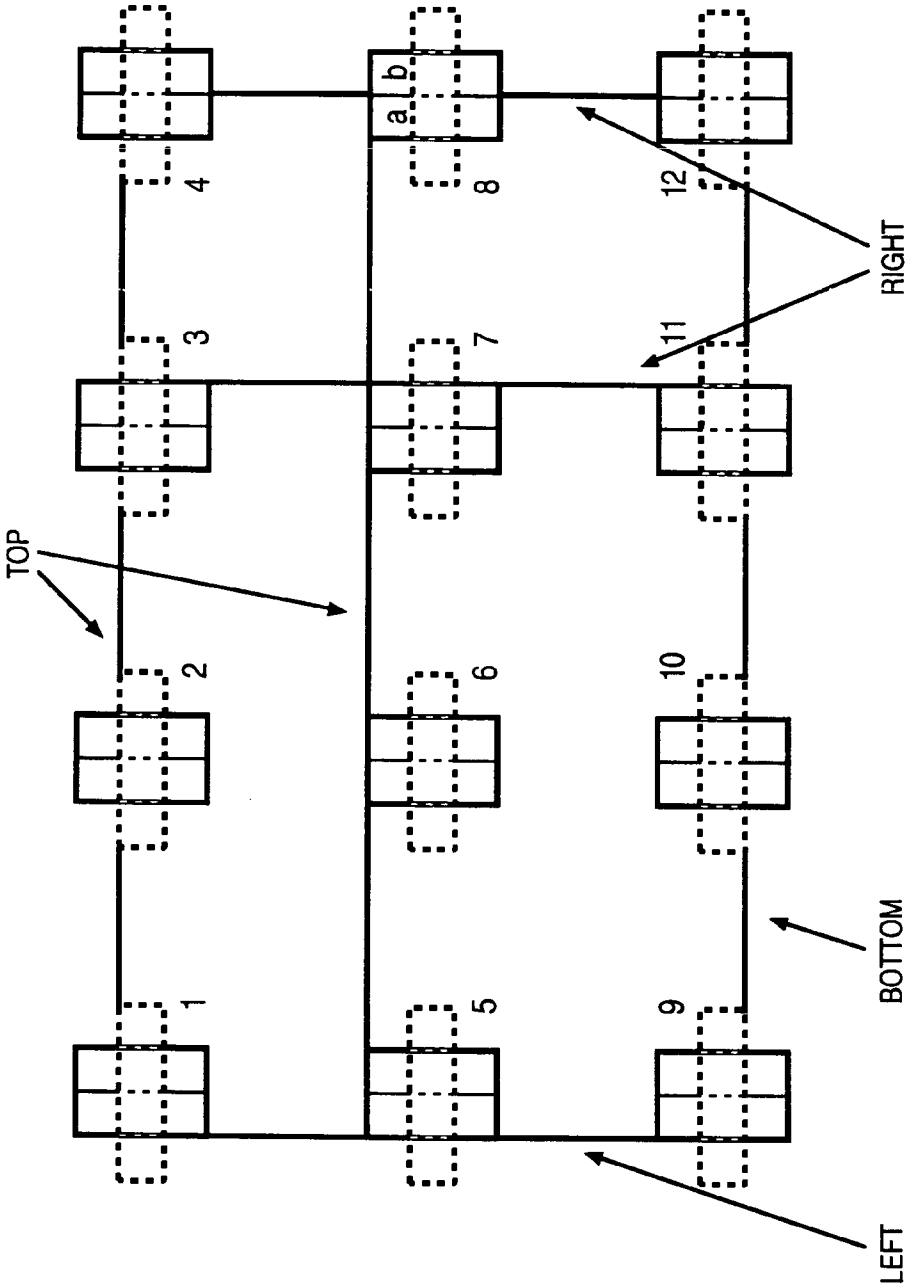


FIG. 18I

CASE	SUBY		SUBX		CUR		PATCHY				PATCHX				SLICE	PEL
	INIT	WRAP	INIT	WRAP	MIN	MAX	INIT	TOP	WRAP	BOT	INIT	LEFT	WRAP	RIGHT		
1	0	0	0	0	1	3	2	0	3	0	0	0	3	0	3	7
2	0	0	0	0	0	3	2	0	3	0	0	0	3	0	3	7
3	0	0	0	0	0	2	2	0	3	0	0	0	3	0	3	7
4	0	0	0	0	0	1	2	0	3	0	0	0	0	1	3	7
5	0	0	0	0	1	3	0	0	3	0	0	0	3	0	3	7
6	0	0	0	0	0	3	0	0	3	0	0	0	3	0	3	7
7	0	0	0	0	0	2	0	0	3	0	0	0	3	0	3	7
8	0	0	0	0	0	1	0	0	3	0	0	0	0	1	3	7
9	0	0	0	0	1	3	0	0	2	1	0	0	3	0	3	7
10	0	0	0	0	0	3	0	0	2	1	0	0	3	0	3	7
11	0	0	0	0	0	2	0	0	2	1	0	0	3	0	3	7
12	0	0	0	0	0	1	0	0	2	1	0	0	0	1	3	7

FIG. 18J

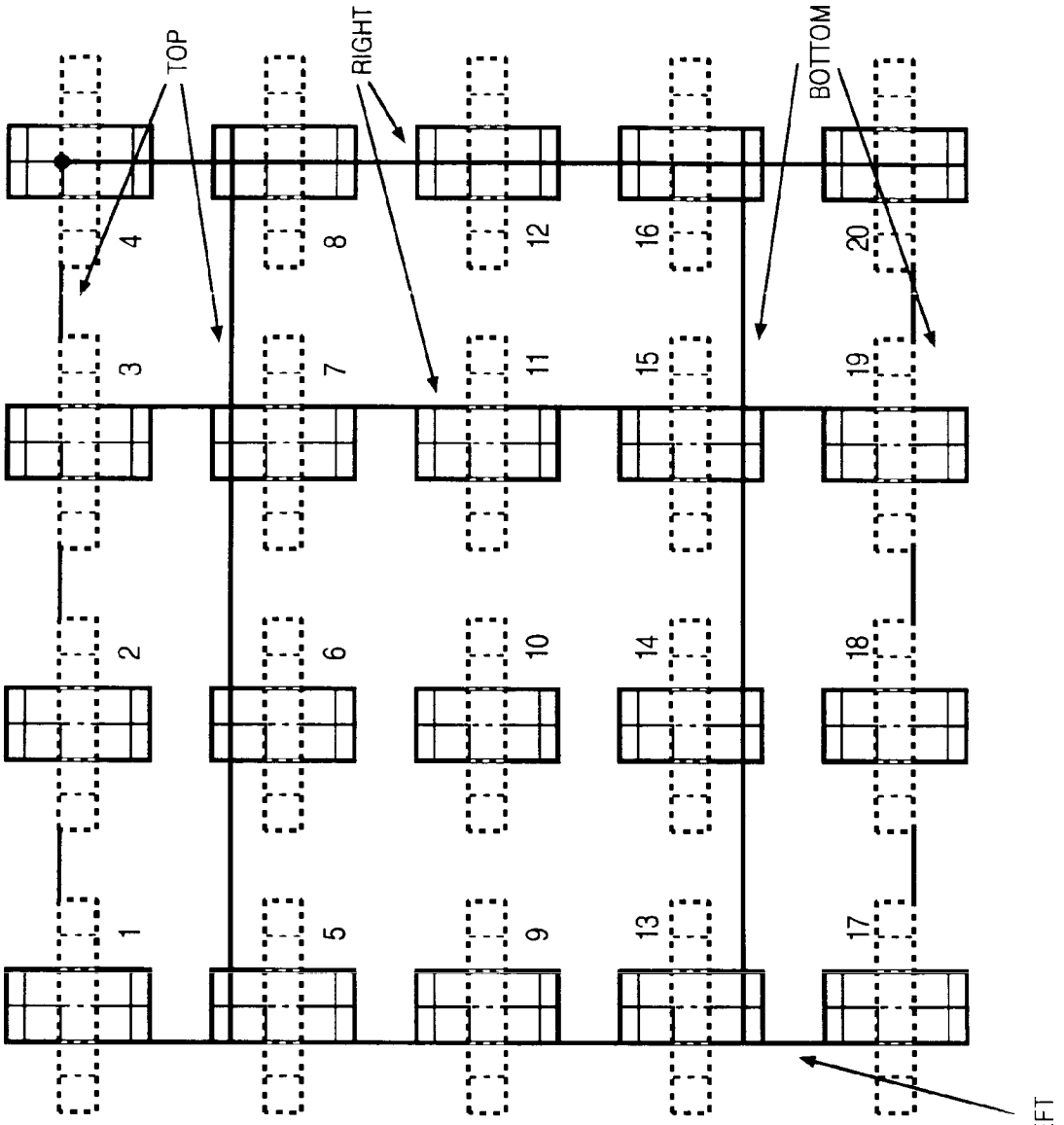
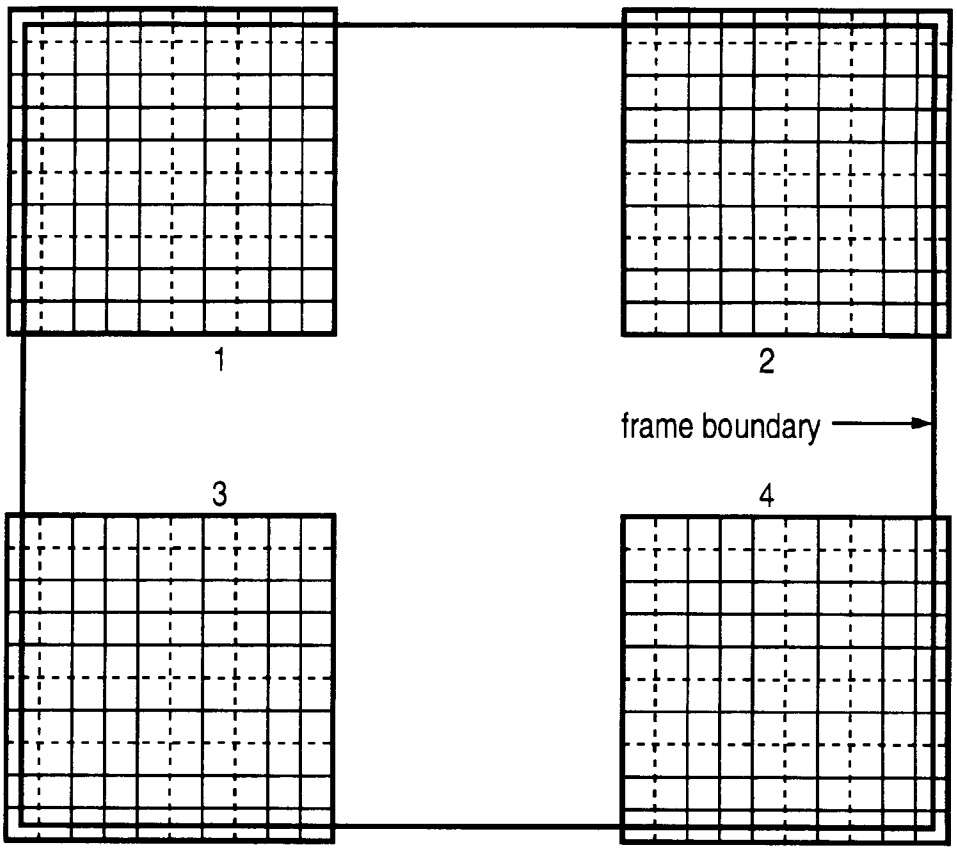


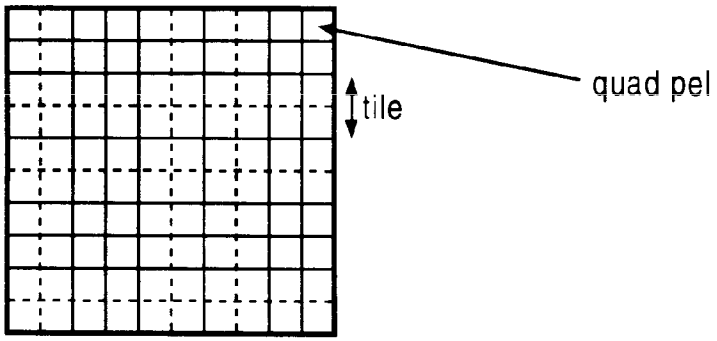
FIG. 18K

CASE	SUBY		SUBX		CUR		PATCHY				PATCHX				SLICE	PEL
	INIT	WRAP	INIT	WRAP	INIT	WRAP	INIT	TOP	WRAP	BOT	INIT	LEFT	WRAP	RIGHT		
1	0	0	0	0	2	5	3	0	5	0	0	0	3	0	3	7
2	0	0	0	0	0	5	3	0	5	0	0	0	3	0	3	7
3	0	0	0	0	0	3	3	0	5	0	0	0	3	0	3	7
4	0	0	0	0	0	2	3	0	5	0	0	0	0	1	3	7
5	0	0	0	0	2	5	1	0	5	0	0	0	3	0	3	7
6	0	0	0	0	0	5	1	0	5	0	0	0	3	0	3	7
7	0	0	0	0	0	3	1	0	5	0	0	0	3	0	3	7
8	0	0	0	0	0	2	1	0	5	0	0	0	0	1	3	7
9	0	0	0	0	2	5	0	0	5	0	0	0	3	0	3	7
10	0	0	0	0	0	5	0	0	5	0	0	0	3	0	3	7
11	0	0	0	0	0	3	0	0	5	0	0	0	3	0	3	7
12	0	0	0	0	0	2	0	0	5	0	0	0	0	1	3	7
13	0	0	0	0	2	5	0	0	4	1	0	0	3	0	3	7
14	0	0	0	0	0	5	0	0	4	1	0	0	3	0	3	7
15	0	0	0	0	0	3	0	0	4	1	0	0	3	0	3	7
16	0	0	0	0	0	2	0	0	4	1	0	0	0	1	3	7
17	0	0	0	0	2	5	0	0	2	1	0	0	3	0	3	7
18	0	0	0	0	0	5	0	0	2	1	0	0	3	0	3	7
19	0	0	0	0	0	3	0	0	2	1	0	0	3	0	3	7
20	0	0	0	0	0	2	0	0	2	1	0	0	0	1	3	7

FIG. 18L



Positions of reference macroblock region with respect to corners of the frame



reference macroblock region of 5X5 tiles

FIG. 18M-1

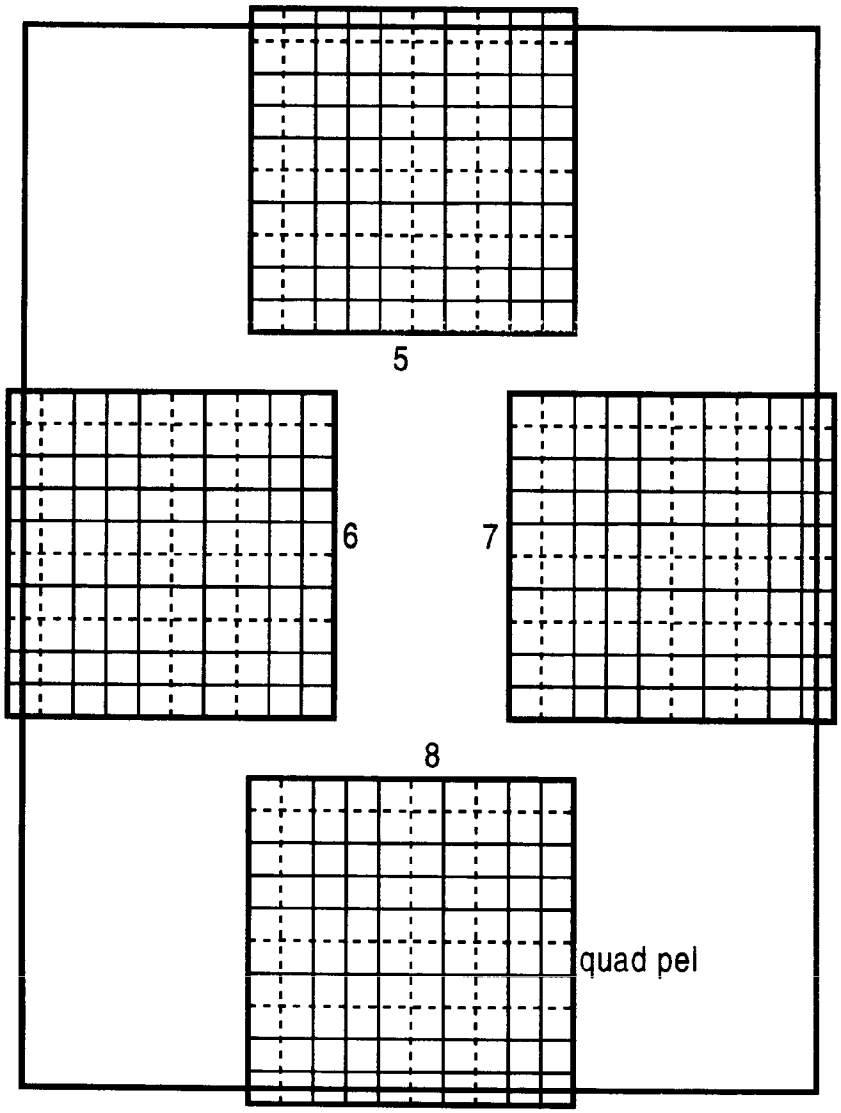


FIG. 18M-2

CASE	SUBY		SUBX		CUR		PATCHY				PATCHX				SLICE	PEL
	INIT	WRAP	INIT	WRAP	INIT	WRAP	INIT	TOP	WRAP	BOT	INIT	LEFT	WRAP	RIGHT		
1	0	1	0	1	0	3	0	2	0	0	1	0	1	0	15	7
2	0	1	0	1	0	3	0	2	0	0	0	0	0	1	15	7
3	0	1	0	1	0	3	0	0	0	2	1	0	1	0	15	7
4	0	1	0	1	0	3	0	0	0	2	0	0	0	1	15	7
5	0	1	0	1	0	3	0	2	0	0	0	0	1	0	15	7
6	0	1	0	1	0	3	0	0	0	0	1	0	1	0	15	7
7	0	1	0	1	0	3	0	0	0	0	0	0	0	1	15	7
8	0	1	0	1	0	3	0	0	0	2	0	0	1	0	15	7
inside	0	1	0	1	0	3	0	0	0	0	0	0	1	0	15	7

FIG. 18N

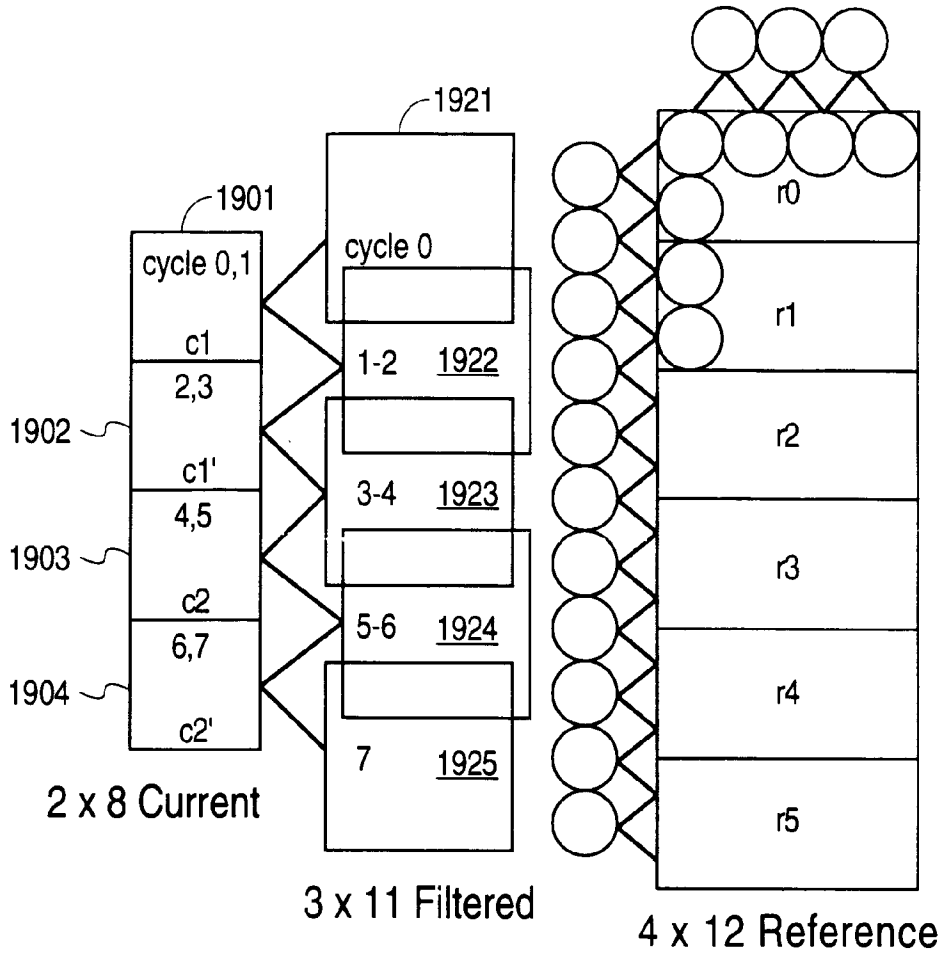


FIG. 19A

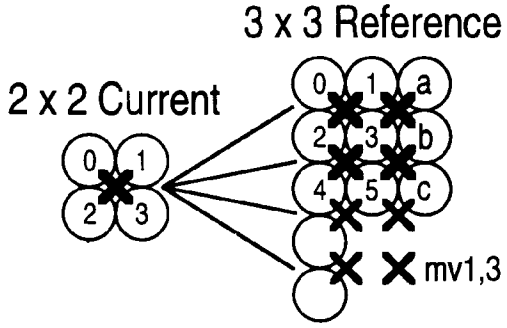
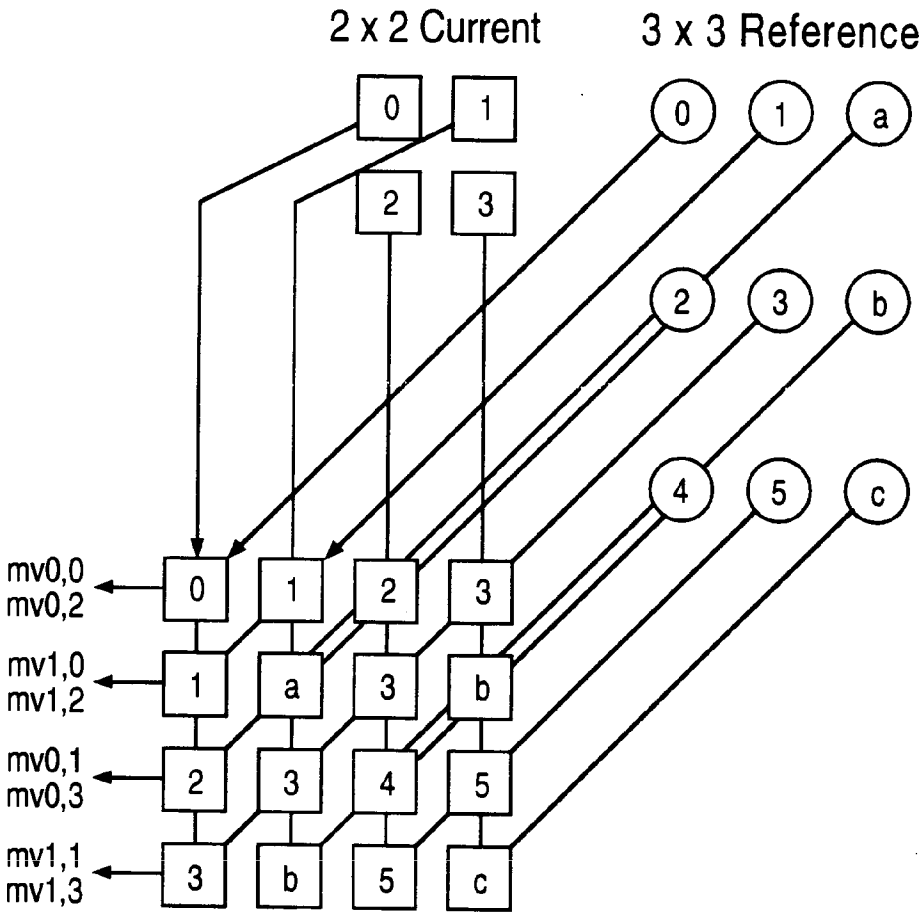


FIG. 19B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3 x 3 Reference
0
1
2
3
0
1
a
2
3
b
4
5
c
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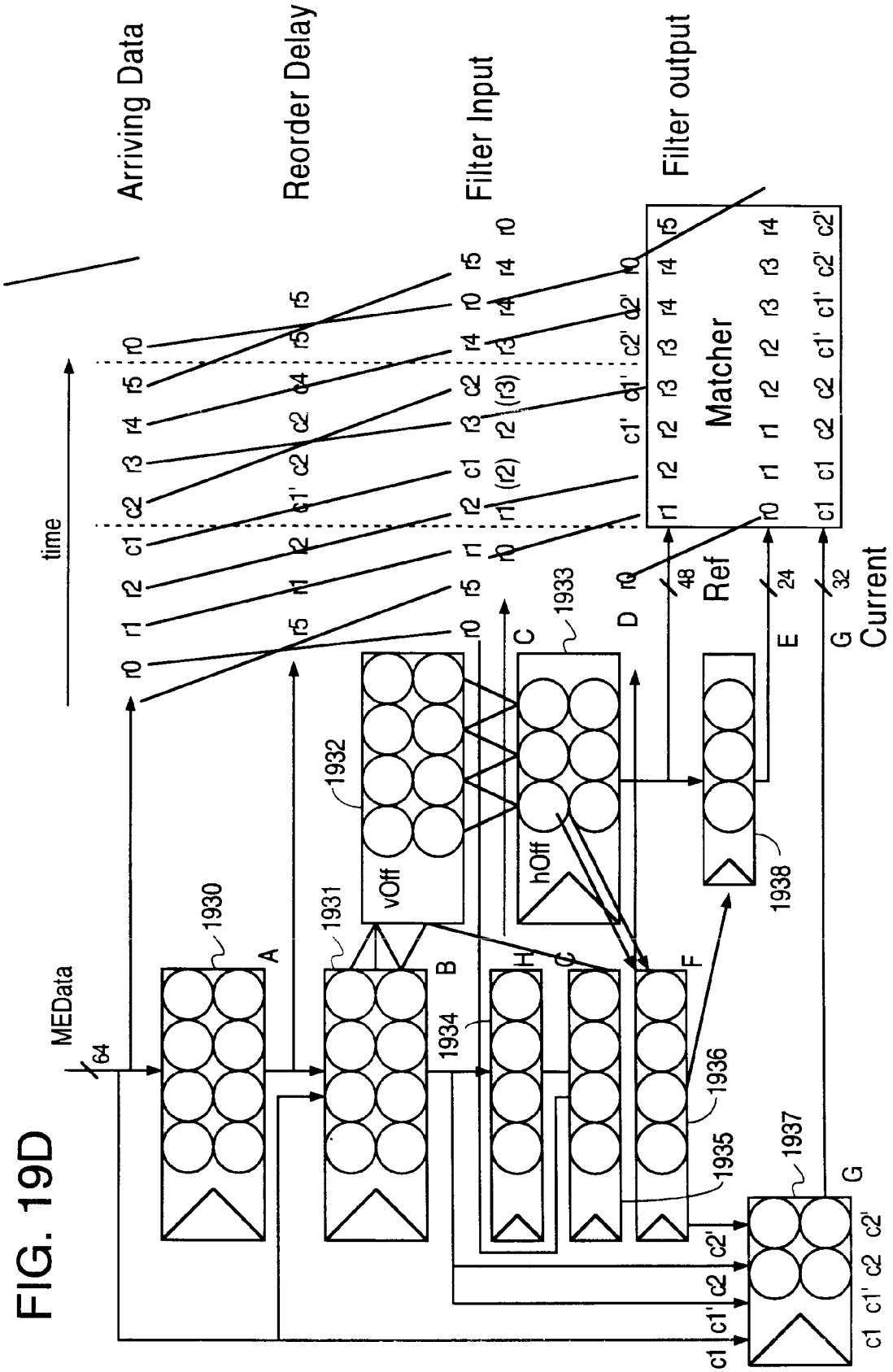
mv0,2
mv1,0
mv1,2
mv0,1
mv0,3
mv1,1
mv1,3

FIG. 19C


Arriving Data
Reorder Delay
Filter Input
Filter output
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MEData
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1930
1931
1932
1933
1934
1935
1936
1937
1938
vOff
hOff
Matcher
Ref
Current
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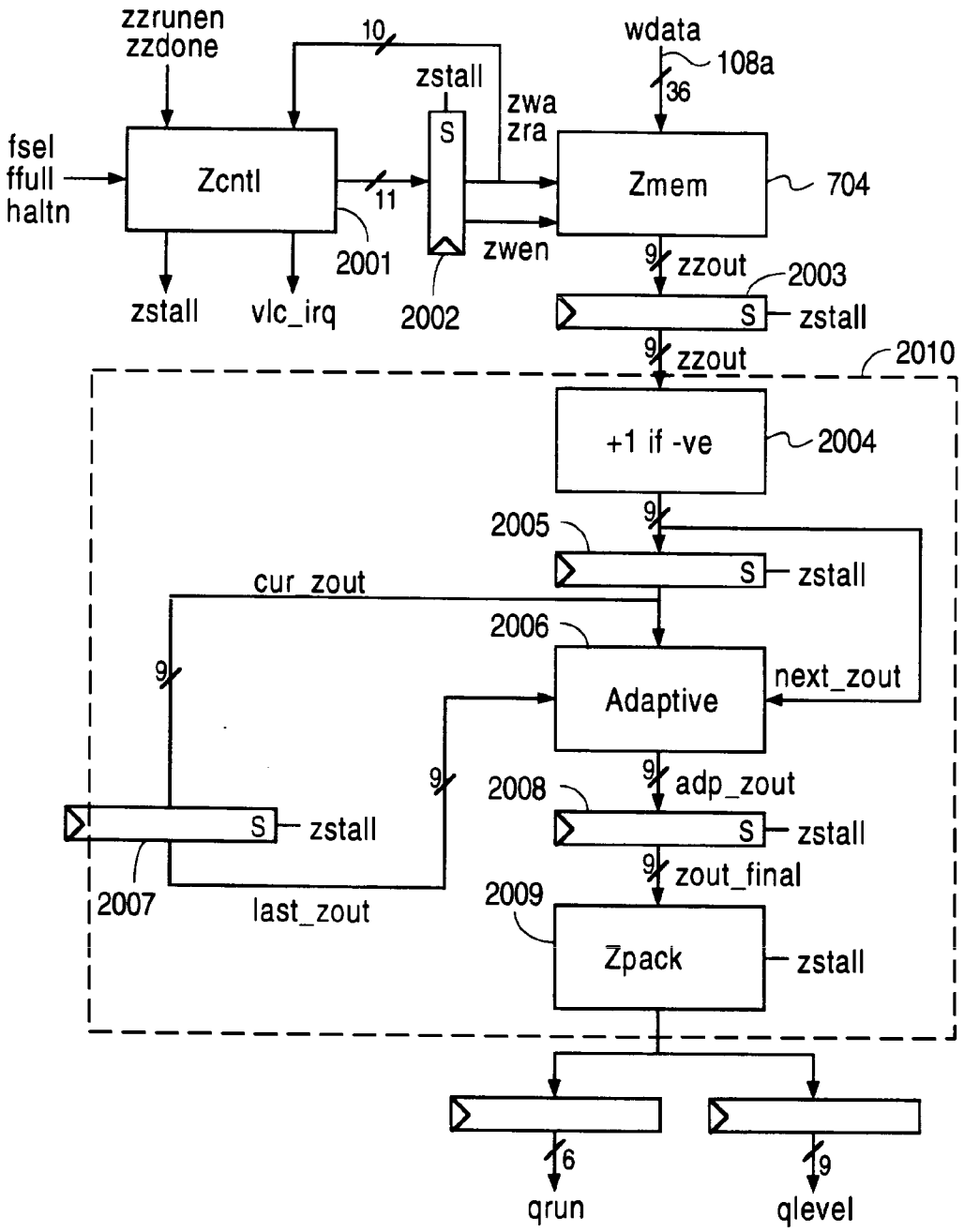
24
32
A
B
C
D
E
F
G
H

FIG. 19D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zzout
2003
zstall
vlc_irq
2002
2010
+1 if -ve
2004
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cur_zout
2006
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2008
adp_zout
2007
last_zout
zout_final
2009
Zpack
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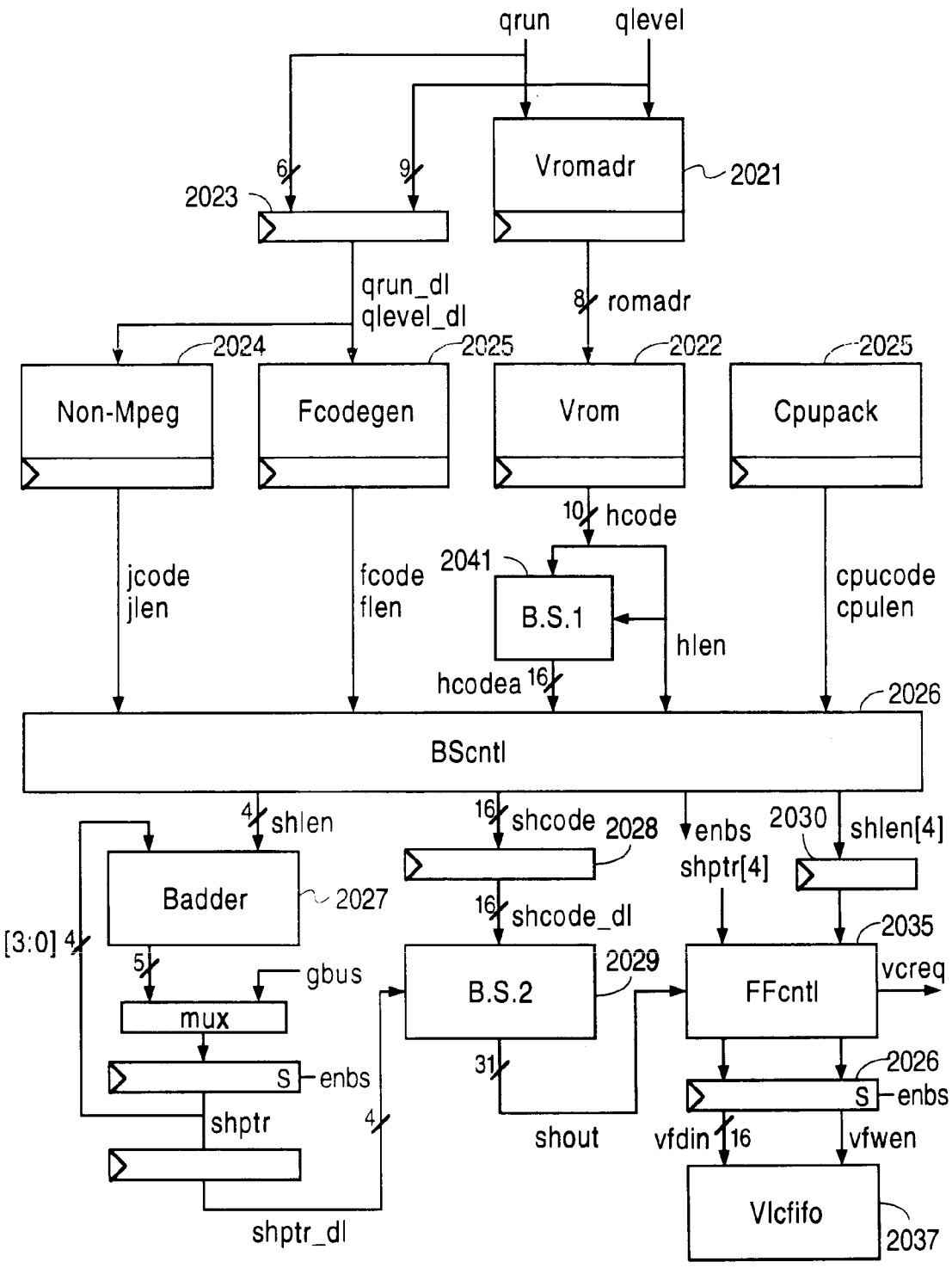
qrun
qlevel

FIG. 20A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qlevel
Vromadr
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2023
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qlevel_dl
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romadr
2024
2025
2022
2025
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Fcodegen
Vrom
Cpupack
10
hcode
jcode
jlen
fcode
flen
2041
B.S.1
hlen
cpucode
cpulen
hcodea
16
2026
BScntl
4
shlen
16
shcode
2028
enbs
2030
shlen[4]
shptr[4]
Badder
2027
16
shcode_dl
[3:0]
4
5
gbus
2035
vcreq
B.S.2
2029
FFcntl
mux
S
enbs
2026
S
enbs
shptr
4
31
shout
vfdin
16
vfwen
Vlcfifo
2037
shptr_dl

FIG. 20B

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012CON1

CONFIRMATION NO. 6996

30423
STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX75006

Title: ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

Publication No. US-2008-0088637-A1
Publication Date: 04/17/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/956,165	12/13/2007	Jefferson Eugene Owen	96-S-012CON1

CONFIRMATION NO. 6996

30423
STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX75006

Date Mailed. 01/10/2008

NOTICE OF NEW OR REVISED PROJECTED PUBLICATION DATE

The above-identified application has a new or revised projected publication date. The current projected publication date for this application is 04/17/2008. If this is a new projected publication date (there was no previous projected publication date), the application has been cleared by Licensing & Review or a secrecy order has been rescinded and the application is now in the publication queue.

If this is a revised projected publication date (one that is different from a previously communicated projected publication date), the publication date has been revised due to processing delays in the USPTO or the abandonment and subsequent revival of an application. The application is anticipated to be published on a date that is more than six weeks different from the originally-projected publication date.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/956,165	12/13/2007	2621	1450	96-S-012C3 (850063.553C3)	20	5

CONFIRMATION NO. 6996

30423
STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

FILING RECEIPT

OC00000027406946

Date Mailed: 12/27/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jefferson Eugene Owen, Freemont, CA;
Raul Zegers Diaz, Palo Alto, CA;
Osvaldo Colavin, Tucker, GA;

Assignment For Published Patent Application

STMICROELECTRONICS, INC., Carrollton, TX

Power of Attorney: The patent practitioners associated with Customer Number 30423

Domestic Priority data as claimed by applicant

This application is a CON of 10/174,918 06/19/2002
which is a CON of 09/539,729 03/30/2000 PAT 6,427,194
which is a CON of 08/702,910 08/26/1996 PAT 6,058,459

Foreign Applications

Projected Publication Date: To Be Determined - pending completion of Security Review

Non-Publication Request: No

Early Publication Request: No

Title

ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

Preliminary Class

375

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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This POA copy is intended for the attached continuation application being submitted on December 13, 2007; attorney docket no. 850063.553C3.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson E. Owen et al.
Application No.	:	08/702,910
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY
Examiner	:	Glenn Gossage
Art Unit	:	2751
Docket No.	:	96-S-12 (850063.553)
Date	:	April 12, 1999

Assistant Commissioner for Patents
Washington, DC 20231

APPOINTMENT OF ASSOCIATE POWER OF ATTORNEY

Sir:

I, Lisa K. Jorgenson, attorney of record in the above-identified application, appoint as associate attorneys David V. Carlson, Reg. No. 31,153; Michael J. Donohue, Registration No. 35,859, Kevin S. Ross, Reg. No. 42,116; Dale C. Barr, Reg. No. 40,498; Kevin S. Costanza, Reg. No. 37,801, Brian L. Johnson, Reg. No. 40,033, Paul F. Rusyn, Reg. No. 42,118, Dennis M. de Guzman, Reg. No. 41,702; E. Russell Tarleton, Reg. No. 31,800, John M. Wechkin, Reg. No. 42,216; Robert D. McCutcheon, Reg. No. 38,717; and Theodore E. Galanthay, Reg. No. 24,122.

It is requested that correspondence continue to be addressed to Lisa K. Jorgenson at:

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Respectfully submitted,
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PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C3 (850063.553C3)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
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Citizenship under 37 CFR 1.41(b) i: US

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Address 2	

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Postal Code	94303	Country i	US

Applicant 3 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
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Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C3 (850063.553C3)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY	

Citizenship under 37 CFR 1.41(b) [i]	FR		
Mailing Address of Applicant:			
Address 1	2820 Livsey Court		
Address 2			
City	Tucker	**State/Province**	GA
Postal Code	30084	**Country**[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	30423		
Email Address	davec.docketing@seedip.com	Add Email	Remove Email

Application Information:

Title of the Invention	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY		
Attorney Docket Number	96-S-012C3 (850063.553C3)	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C3 (850063.553C3)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY	
Customer Number	30423	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	10174918	2002-06-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
10174918	Continuation of	09539729	2000-03-30	6427194	2002-07-30

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
09539729	Continuation of	08702910	1996-08-26	6058459	2000-05-02

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

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Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	STMicroelectronics, Inc.

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C3 (850063.553C3)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY	

Mailing Address Information:			
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Address 2			
City	Carrollton	**State/Province**	TX
Country [i]	US	Postal Code	75006
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/David V. Carlson/			Date (YYYY-MM-DD)	2007-12-13
First Name	David	Last Name	Carlson	Registration Number	31153

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
For	:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
Docket No.	:	96-S-012C3 (850063.553C3)
Date	:	December 13, 2007

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FEE DEFICIENCY AUTHORIZATION FORM

Commissioner for Patents:

Applicants hereby authorize the Director to charge any deficiencies in fees due by way of the enclosed papers only under 37 CFR 1.16 and 1.17 to Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
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1077869_1.DOC

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	David V. Carlson/Tyler Livas
Attorney Docket Number:	96-S-012C3 (850063.553C3)

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Independent claims in excess of 3	1201	2	210	420
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1450**

Electronic Acknowledgement Receipt

EFS ID:	2589134
Application Number:	11956165
International Application Number:	
Confirmation Number:	6996
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Tyler Livas
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C3 (850063.553C3)
Receipt Date:	13-DEC-2007
Filing Date:	
Time Stamp:	18:26:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1450
RAM confirmation Number	3294
Deposit Account	191090
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		850063_553C3_APP.pdf	167001 d2993ace667d77086fad0c643099b54e881f9ea6	yes	30

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	24
Claims	25	29
Abstract	30	30

Warnings:					
Information:					
2	Drawings-only black and white line drawings	850063_553C3_Drawings.PDF	3985251 e0869325b2a8cb63930308b3dffe0f886506989f	no	6
Warnings:					
Information:					
3	Oath or Declaration filed	850063_553C3_Declaration.PDF	108011 1491bb35bef9de9fbb1e6f287940fa876f99851e	no	4
Warnings:					
Information:					
4	Power of Attorney	850063_553C3_POA.PDF	39268 d58ea03065144d455b8fc92da9962f976d8299cb	no	1
Warnings:					
Information:					
5	Application Data Sheet	850063_553C3_ADS.PDF	1093949 97534eeb0fbae03b4ef92390d6c69ca18bf7a722	no	5
Warnings:					
Information:					
6	Miscellaneous Incoming Letter	850063_553C3_FDA.pdf	55486 d887dca807063a3a06e0494ba49fe39b15f40c9f	no	1
Warnings:					
Information:					
7	Fee Worksheet (PTO-06)	fee-info.pdf	8576 6e17bcc13e0c43fc2caa0703f12ae3eb8312cf65	no	2
Warnings:					
Information:					

Total Files Size (in bytes): 5457542

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

ELECTRONIC SYSTEM AND METHOD FOR DISPLAY USING A DECODER AND ARBITER TO SELECTIVELY ALLOW ACCESS TO A SHARED MEMORY

Cross-reference to Related Applications

This application is a continuation of U.S. Patent Application No. 10/174,918, filed June 19, 2002, and allowed November 29, 2007; which is a continuation of U.S. Patent No. 6,427,194, issued July 30, 2002; which is a continuation of U.S. Patent No. 6,058,459, issued May 2, 2000. All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

Cross-reference to Other Related Applications

The present application contains some text and drawings in common with U.S. Patent Application No. 08/702,911, filed August 26, 1996, and issued September 22, 1998 as U.S. Patent No. 5,812,789, entitled: "VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE" by Raul Z. Diaz and Jefferson E. Owen, which had the same effective filing date and ownership as the present application, and to that extent is related to the present application, which is incorporated herein by reference.

Background

The present invention relates to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.

The size of a digital representation of uncompressed video images is dependent on the resolution and color depth of the image. A movie composed of a sequence of such images, and the audio signals that go along with them, quickly become

large enough so that, uncompressed, such a movie typically cannot fit entirely onto a conventional recording medium such as a Compact Disc (CD). It is now also typically prohibitively expensive to transmit such a movie uncompressed.

It is therefore advantageous to compress video and audio sequences before they are transmitted or stored. A great deal of effort is being expended to develop systems to compress these sequences. Several coding standards currently in use are based on the discrete cosine transfer algorithm including MPEG-1, MPEG-2, H.261, and H.263. (MPEG stands for "Motion Picture Expert Group", a committee of the International Organization for Standardization, also known as the International Standards Organization, or ISO.) The MPEG-1, MPEG-2, H.261, and H.263 standards are decompression protocols that describe how an encoded bitstream is to be decoded. The encoding can be done in any manner, as long as the resulting bitstream complies with the standard.

Video and/or audio compression devices (hereinafter "encoders") are used to encode the video and/or audio sequence before it is transmitted or stored. The resulting bitstream is decoded by a video and/or audio decompression device (hereinafter "decoder") before the video and/or audio sequence is displayed. However, a bitstream can only be decoded by a decoder if it complies with the standard used by the decoder. To be able to decode the bitstream on a large number of systems, it is advantageous to encode the video and/or audio sequences in compliance with a well accepted decompression standard. The MPEG standards are currently well accepted standards for one-way communication. H-261, and H.263 are currently well accepted standards for video telephony.

Once decoded, the images can be displayed on an electronic system dedicated to displaying video and audio, such as television or a Digital Video Disk (DVD) player, or on electronic systems where image display is just one feature of the system, such as a computer. A decoder needs to be added to these systems to allow them to display compressed sequences, such as received images and associated audio, or ones taken from a storage device. An encoder needs to be added to allow the system to compress video and/or audio sequences, to be transmitted or stored. Both need to be added for two-way communication such as video telephony.

A typical decoder, such as an MPEG decoder 10 shown in Figure la, contains video decoding circuit 12, audio decoding circuit 14, a microcontroller 16, and a memory interface 18. The decoder can also contain other circuitry depending on the electronic system in which the decoder is designed to operate. For example, when the decoder is designed to operate in a typical television, it will also contain an on-screen display (OSD) circuit.

Figure 1b shows a better decoder architecture, used in the STi3520 and STi3520A MPEG Audio/MPEG-2 Video Integrated Decoder manufactured by ST Microelectronics, Inc., Carrollton, Texas. The decoder has a register interface 20 instead of a microcontroller. The register interface 20 is coupled to an external microcontroller 24. The use of a register interface 20 makes it possible to tailor the decoder 10 to the specific hardware with which the decoder 10 interfaces, or to change its operation without having to replace the decoder by just reprogramming the register interface. It also allows the user to replace the microcontroller 24, to upgrade or tailor the microcontroller 24 to a specific use, by just replacing the microcontroller and reprogramming the register interface 20, without having to replace the decoder 10.

The memory interface 18 is coupled to a memory 22. A typical MPEG decoder 10 requires 16 Mbits of memory to operate in the Main Profile at Main Level mode (MP at ML). This typically means that the decoder requires a 2Mbyte memory. Memory 22 is dedicated to the MPEG decoder 10 and increases the price of adding a decoder 10 to the electronic system. In current technology, the cost of this additional dedicated memory 22 can be a significant percentage of the cost of the decoder.

An encoder also requires a memory interface 18 and dedicated memory. Adding the encoder to an electronic system again increases the price of the system by both the price of the encoder and its dedicated memory.

Figure 1c shows a conventional decoder inserted in a computer architecture. A conventional computer generally includes a peripheral bus 170 to connect several necessary or optional components, such as a hard disk, a screen, etc. These peripherals are

connected to bus 170 via interfaces (e.g., a display adapter 120 for the screen) which are provided directly on the computer's motherboard or on removable boards.

A Central Processing Unit (CPU) 152 communicates with bus 170 through an interface circuit 146 enabling a main memory 168 of the computer to be shared between CPU 152 and peripherals of bus 170 which might require it.

The decoder 10 is connected as a master peripheral to bus 170, that is, it generates data transfers on this bus without involving CPU 152. The decoder receives coded or compressed data CD from a source peripheral 122, such as a hard disk or a compact disk read only memory (CD-ROM), and supplies decoded images to display adapter 120. Recent display adapters make it possible to directly process the "YUV" (luminance and chrominance) image data normally supplied by a decoder, while a display adapter is normally designed to process "RGB" (red, green, blue) image information supplied by CPU 152.

Display adapter 120 uses memory 12-1 for storing the image under display, which comes from the CPU 152 or from the decoder 10. A conventional decoder 10 also uses dedicated memory 22. This memory is typically divided into three image areas or buffers M1 to M3 and a buffer CDB where the compressed data are stored before they are processed. The three image buffers respectively contain an image under decoding and two previously decoded images.

Figure 1d illustrates the use of buffers M1 to M3 in the decoding of a sequence of images I0, P1, B2, B3, P4, B5, B6, P7. I stands for a so-called "intra" image, whose compressed data directly corresponds to the image. P stands for a so-called "predicted" image, the reconstruction of which uses pixel blocks (or macroblocks) of a previously decoded image. Finally, B stands for a so-called "bidirectional" image, the reconstruction of which uses macroblocks of two previously decoded images. The intra and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while the bidirectional images are not used again.

Images I0 and P1 are respectively stored in buffers M1 and M2 during their decoding. The filling and the emptying of a buffer in Fig. 1d are indicated by oblique

lines. The decoding of image P1 uses macroblocks of image I0. Image I0, stored in buffer M1, is displayed during the decoding of image B2, this image B2 being stored in buffer M3. The decoding of image B2 uses macroblocks of images I0 and P1. Image B2 is displayed immediately after image I0. As the locations of buffer M3 become empty, they are filled by decoded information of image B3. The decoding of image B3 also uses macroblocks of images I0 and P1. Once image B3 is decoded, it is displayed immediately, while image P4 is decoded by using macroblocks of image P1. Image P4 is written over image I0 in buffer M1 since image I0 will no longer be used to decode subsequent images. After image B3, image P1 is displayed while buffer M3 receives image B5 under decoding. The decoding of image B5 uses macroblocks of images P1 and P4. Image P1 is kept in buffer M2 until the decoding of image B6, which also uses macroblocks of images P1 and P4, and so on.

Referring again to Figure 1c, when any component needs access to the main memory 168 either to read from or write to the main memory 168, it generates a request which is placed on the bus 170. When the request is a write, the data to be written is also placed on the bus 170. The request is processed and the data is then either written to or read from the main memory 168. When data is read from the main memory 168, the data is now placed on the bus and goes to the component that requested the read.

There are typically many components in the computer systems that may require access to the main memory 168, and they are typically all coupled to the same bus 170, or possibly to several buses if there are not enough connectors on one bus to accommodate all of the peripherals. However, the addition of each bus is very expensive. Each request is typically processed according to a priority system. The priority system is typically based on the priority given to the device and the order in which the requests are received. Typically, the priority system is set up so no device monopolizes the bus, starving all of the other devices. Good practice suggest that no device on the bus require more than approximately 50% of the bus's bandwidth.

The minimum bandwidth required for the decoder 10 can be calculated based on the characteristics and desired operation of the decoder. These characteristics

include the standard with which the bitstream is encoded to comply, whether the decoder is to operate in real time, to what extent frames are dropped, and how the images are stored. Additionally, the latency of the bus that couples the decoder to the memory should be considered.

If the decoder does not operate in real time, the decoded movie would stop periodically between images until the decoder can get access to the memory to process the next image. The movie may stop and wait quite often between images.

To reduce the minimum required bandwidth and still operate in real time, the decoder 10 may need to drop frames. If the decoder 10 regularly does not decode every frame, then it may not need to stop between images. However, this produces very poor continuity in the images. This is problematic with an image encoded to the MPEG-1 or MPEG-2 standards, or any standard that uses temporal compression. In temporal (interpicture) compression, some of the images are decoded based on previous images and some based on previous and future images. Dropping an image on which the decoding of other images is based is unacceptable, and will result in many poor or even completely unrecognizable images.

The computer can also contain both a decoder and encoder to allow for video telephony, as described above. In this case, not operating in real time would mean that the length of time between the occurrence of an event such as speaking at one end of the conversation until the event is displayed at the other end of the conversation--is increased by the time both the encoder and then the decoder must wait to get access to the bus and the main memory. Not being able to operate in real time means that there would be gaps in the conversation until the equipment can catch up. This increases the time needed to have a video conference, and makes the conference uncomfortable for the participants.

One widely used solution to allow a component in a computer system to operate in real time is to give the component its own dedicated memory. Thus, as shown in Figure 1c, the decoder 10 can be given its own dedicated memory 22, with a dedicated bus 26 to connect the decoder 10 to its memory 22. The dedicated memory 22 significantly

increases the cost of adding a decoder 10 to the computer. A disadvantage of a computer equipped with a conventional decoder is that it has a non-negligible amount of memory which is unused most of the time.

Indeed, memory 22 of the decoder is only used when decoded images are being viewed on the computer screen or need to be encoded, which amounts to only a fraction of the time spent on a computer. This memory--inaccessible to the other peripherals or to the CPU--has a size of 512 Kbytes in an MPEG-1 decoder and Mbytes in an MPEG-2 decoder. Further, this memory is oversized, since it is obtained by using currently available memory components.

Summary of the Invention

The present application discloses an electronic system that contains a first device and video and/or audio decompression and/or compression device capable of operating in real time. Both the first device and the video and/or audio decompression and/or compression device require access to a memory. The video and/or audio decompression and/or compression device shares the memory with the first device. The two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time.

In one preferred embodiment of the invention the two devices share an arbiter. The arbiter and Direct Memory Access (DMA) engines of the video and/or audio decompression and/or compression device and of the first device are configured to arbitrate between the two devices when one of them is requesting access to the memory. This allows both the video and/or audio decompression and/or compression device and the first device to share the memory.

When the video and/or audio decompression and/or compression device used in an electronic system, such as a computer, already containing a device that has a memory the video and/or audio decompression and/or compression device can share that memory, and the memory of the video and/or audio decompression and/or compression

device can be eliminated. Eliminating the memory greatly reduces the cost of adding the video and/or audio decompression and/or compression device to the electronic system.

The decoder memory is part of the main memory of the computer. The computer should have a fast bus (such as a memory bus, a PCI -"Peripheral Component Interconnect" - bus, a VLB -"VESA (Video Electronics Standards Association) Local Bus", or an AGP - "Advanced Graphics Port" - bus, or any bus having a bandwidth sufficient to allow the system to operate in real time) which will accept high image rates between the decoder, the main memory and the display adapter.

According to an embodiment of the present invention, the decoder directly supplies a display adapter of the screen with an image under decoding which is not used to decode a subsequent image.

According to an embodiment of the present invention, the main memory stores predicted images which are obtained from a single preceding image and also stores intra images which are not obtained from a preceding image. The images directly supplied to the display adapter are bidirectional images obtained from two preceding intra or predicted images.

According to an embodiment of the present invention, the decoder is disposed on the computer's motherboard.

An advantage of the present invention is the significant cost reduction due to the fact that the video and/or audio decompression and/or compression device does not need its own dedicated memory but can share a memory with another device and still operate in real time.

A further advantage of the present invention is that the video and/or audio decompression and/or compression device can share the memory with a device without being integrated into this device, allowing the first device to be a standard device with some adjustments made to its memory interface.

Other advantages and objects of the invention will be apparent to those of ordinary skill in the art having reference to the following specification together with the drawings.

Brief Description of the Drawings

Figure 1a and 1b are electrical diagrams, in block form, of prior art decoders.

Figure 1c is an electrical diagram, in block form, of a computer architecture including a conventional decoder.

Figure 1d, illustrates the use of image buffers in the processing of an image sequence by a conventional MPEG decoder.

Figure 2 is an electrical diagram, in block form, of an electronic system containing a device having a memory interface and an encoder and decoder.

Figure 3 is an electrical diagram, in block form, of a computer system containing a core logic chipset designed for the CPU to share a memory interface with an encoder and/or decoder according to one embodiment of the present invention.

Figure 4 is an electrical diagram, in block form, of a computer architecture including an encoder and/or decoder according to another embodiment of the present invention.

Figure 5 illustrates the use of image buffers in the processing of an image sequence by an MPEG decoder according to the present invention.

Figure 6 is an electrical diagram, in block form, of an embodiment of an MPEG decoder architecture according to the present invention.

Figure 7 is an electrical diagram, in block form, of a computer system containing a graphics accelerator designed to share a memory interface with an encoder and/or decoder.

Detailed Description of the Preferred Embodiment

Figure 2 shows an electronic system 40 containing a first device 42 having access to a memory 50, and a decoder 44 and encoder 46, having access to the same memory 50. First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50, and either contains or is coupled to a memory interface. In the preferred embodiment of the invention, electronic system 40

contains a first device 42, a decoder 44, an encoder 46, and a memory 50, although, either the decoder 44 or encoder 46 can be used in the video and/or audio decompression and/or compression device 80 without the other. For ease of reference, a video and/or audio decompression and/or compression device 80 will hereinafter be referred to as decoder/encoder 80. The decoder/encoder 80 may be a single device, or a cell in an integrated circuit; or it may be two separate devices, or cells in an integrated circuit. In the preferred embodiment of the invention, the first device 42, decoder/encoder 80, are on one integrated circuit, however, they can be on separate integrated circuits in any combination.

The decoder 44 includes a video decoding circuit 12 and an audio decoding circuit 14, both coupled to a register interface 20. The decoder 44 can be either a video and audio decoder, just a video encoder, or just an audio decoder. If the decoder 44 is just a video decoder, it does not contain the audio decoding circuitry 14. The audio decoding can be performed by a separate audio coder-decoder (codec) coupled to the first device 42, or through software. In the preferred embodiment of the invention, when the decoder/encoder 80 is in a system containing a processor and is coupled to the processor, the audio decoding is performed in software. This frees up space on the die without causing significant delay in the decoding. If the audio decoding is performed in software, the processor should preferably operate at a speed to allow the audio decoding to be performed in real time without starving other components of the system that may need to utilize the processor. For example, current software to perform AC-3 audio decoding takes up approximately 40% of the bandwidth of a 133 MHz Pentium. The encoder 46 includes a video encoding circuit 62 and an audio encoding circuit 64, both coupled to a register interface 20. The encoder 46 can be either a video and audio encoder, just a video encoder, or just an audio encoder. If the encoder 46 is just a video encoder, it does not contain the audio encoding circuitry 64. The audio encoding can be performed by a separate audio codec coupled to the first device 42, or through software. In the preferred embodiment of the invention, when the decoder/encoder 80 is in a system containing a processor and is coupled to the processor, the audio encoding is performed in software, presenting the same advantages of freeing up space on the die without causing significant delay in the encoding, as in the case

of decoding discussed above. The register interfaces 20 of the decoder 44 and encoder 46 are coupled to a processor.

The decoder 44 and encoder 46 are coupled to the Direct Memory Access (DMA) engine 52. The decoder and encoder can be coupled to the same DMA engine as shown in Figure 2, or each can have its own DMA engine, or share a DMA engine with another device. When the decoder/encoder 80 are two separate devices or cells, decoder 44 and encoder 46 can still be coupled to one DMA engine 52. When the decoder/encoder is one device or is one cell on an integrated circuit, the DMA engine 52 can be part of the decoder/encoder 80, as shown in Figure 2. The DMA engine 52 is coupled to the arbiter 82 of the memory interface 76. The arbiter 82 is preferably monolithically integrated into the memory interface 76 of the decoder or into the memory interface 72 of the first device. However, the arbiter 82 can be a separate cell or device coupled to the memory interfaces 76, 72 of the decoder/encoder 80 and the first device 42. The arbiter 82 is also coupled to the refresh logic 58 and the memory controller 56 of the device into which it is monolithically integrated. The refresh logic 58, like the arbiter 82, can be monolithically integrated into the memory interface 76 of the decoder, into the memory interface 72 of the first device, or can be a separate cell or device coupled to the arbiter 82.

The first device 42 also contains a memory interface 72 and a DMA engine 60. The DMA engine 60 of the first device 42 is coupled to the memory interface 72 of the first device 72.

Both memory interfaces 72 and 76 are coupled to a memory 50. The memory controllers 56 are the control logic that generates the address the memory interfaces 72, 76 access in the memory 50 and the timing of the burst cycles.

In current technology, memory 50 is typically a Dynamic Random Access Memory (DRAM). However, other types of memory can be used. The refresh logic 58 is needed to refresh the DRAM. However, as is known in the art, if a different memory is used, the refresh logic 58 may not be needed and can be eliminated.

The decoder/encoder 80 is coupled to the memory 50 through devices, typically a bus 70, that have a bandwidth greater than the bandwidth required for the

decoder/encoder 80 to operate in real time. The minimum bandwidth required for the decoder/encoder 80 can be calculated based on the characteristics and desired operation of the decoder, including the standard with which the bitstream is encoded to comply, whether the decoder/encoder 80 is to operate in real time, to what extent frames are dropped, and which images are stored. Additionally, the latency of the bus 70 that couples the decoder/encoder 80 to the memory 50 should be considered.

A goal is to have the decoder/encoder 80 operate in real time without dropping so many frames that it becomes noticeable to the movie viewer. To operate in real time the decoder/encoder 80 should decode and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 80 has a required bandwidth that allows the decoder/encoder 80 to operate fast enough to decode the entire image in the time between screen refreshes, typically 1/30 of a second, with the human viewer unable to detect any delay in the decoding and/ or encoding. To operate in real time, the required bandwidth should be lower than the bandwidth of the bus. In order not to starve the other components on the bus, i.e., deny these components access to the memory for an amount of time that would interfere with their operation, this required bandwidth should be less than the entire bandwidth of the bus. Therefore, a fast bus 70 should be used. A fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth. In current technology, there are busses, including the Industry Standard Architecture (ISA) bus, whose bandwidth is significantly below the bandwidth required for this.

In the preferred embodiment of the invention, the decoder/encoder 80 is coupled to the memory 50 through a fast bus 70 that has a bandwidth of at least the bandwidth required for the decoder/encoder 80 to operate in real time, a threshold bandwidth. Preferably the fast bus 70 has a bandwidth of at least approximately twice the bandwidth required for the decoder/encoder 80 to operate in real time. In the preferred embodiment, the fast bus 70 is a memory bus, however, any bus having the required bandwidth can be used.

The decoder/encoder 80 only requires access to the memory during operation. Therefore, when there is no need to decode or encode, the first device 42 and any other devices sharing the memory 50 have exclusive access to the memory and can use the entire bandwidth of the fast bus 70.

In the preferred embodiment, even during decoding and encoding, the decoder/encoder 80 does not always use the entire required bandwidth. Since the fast bus 70 has a bandwidth a little less than twice the size of the required bandwidth, the decoder/encoder 80 uses at most 60% of the bandwidth of the fast bus 70.

The required bandwidth is determined based on the size and resolution of the image and the type of frame (I, P, or B). In the preferred embodiment the decoder/encoder typically will be using less than 40% of the bandwidth of the fast bus 70. This frees up the remaining bandwidth to be used by the other devices with which the decoder/encoder 80 is sharing the memory 50.

The decoder/encoder 80 can decode a bitstream formatted according to any one or a combination of standards. In the preferred embodiment of the invention, the decoder/encoder 80 is a multi-standard decoder/encoder capable of decoding and encoding sequences formatted to comply with several well accepted standards. This allows the decoder/encoder 80 to be able to decode a large number of video and/or audio sequences. The choices of which standards the decoder/encoder 80 is capable of decoding bitstreams formatted to, and of encoding sequences to comply with, are based on the desired cost, efficiency, and application of the decoder/encoder 80.

In the preferred embodiment, these standards are capable of both intrapicture compression and interpicture compression. In intrapicture compression the redundancy within the image is eliminated. In interpicture compression the redundancy between two images is eliminated, and only the difference information is transferred. This requires the decoder/encoder 80 to have access to the previous or future image that contains information needed to decode or encode the current image. These previous and/or future images need to be stored and then used to decode the current image. This is one of the reasons the decoder/encoder 80 requires access to the memory, and requires a large

bandwidth. The MPEG-1 and MPEG-2 standards allow for decoding based on both previous images and/or future images. Therefore, for a decoder/encoder 80 capable of operating in real time to be able to comply with the MPEG-1 and MPEG-2 standards, it should be able to access two images--a previous and a future image--fast enough to decode the current image in the 1/30 of a second between screen refreshes.

An MPEG environment is asymmetrical; there are much fewer encoders than decoders. The encoders are very difficult and expensive to manufacture, and the decoders are comparatively easy and cheap. This encourages many more decoders than encoders, with the encoders in centralized locations, and decoders available such that every end user can have a decoder. Therefore, there are many receivers but few transmitters.

For video telephony and teleconferencing, each end user must be able to both receive and transmit. H.261, and H.263 are currently well accepted standards for video telephony. An encoder that can encode sequences to comply with the H.261 and H.263 standards is less complicated, having a lower resolution and lower frame rate than an encoder that complies with the MPEG-1 or MPEG-2 standards, possibly making the quality of the decoded images somewhat lower than those from an encoder that complies with the MPEG-1 or MPEG-2 standards. Since it should be inexpensive and operate in real time, such an encoder is also less efficient than an encoder to encode sequences to comply with the MPEG-1 or MPEG-2 standards, meaning that the compression factor--which is the ratio between the source data rate and the encoded bitstream data rate--of such an encoder is lower for a given image quality than the compression factor of an MPEG encoder. However, because such an encoder is less complicated, it is much cheaper and faster than an encoder capable of complying with the MPEG-1 and/or MPEG-2 standards. This makes video telephony possible, since both a long delay in encoding the signal and a cost that is prohibitively expensive for many users is unacceptable in video telephony.

In the preferred embodiment, the decoder/encoder 80 is capable of decoding a bitstream formatted to comply with the MPEG-1, MPEG-2, H.261, and H.263 standards, and encoding a sequence to produce a bitstream to comply with the H.261, and H.263 standards. This allows the decoder/encoder 80 to be able to be used for video telephony.

The encoding to comply with the H.261 and H.263 standards but not the MPEG-1 and MPEG-2 standards balances the desire to reduce the cost of transmission and storage by encoding to produce the highest compression factor and the desire to keep cost low enough to be able to mass market the device.

Figure 3 shows one embodiment of a computer where the decoder/encoder 80 is sharing a main memory 168 with a core logic chipset 190. The core logic chipset 190 can be any core logic chipset known in the art. In the embodiment shown in Figure 3, the core logic chipset 190 is a Peripheral Component Interconnect (PCI) core logic chipset 190, which contains a PCI core logic device 158, the processor interface 154, a memory interface 72, and bus interface 156 for any system busses 170 to which it is coupled. The core logic chipset 190 can also contain an Accelerated Graphics Port (AGP) 160 if a graphics accelerator 200 is present in the computer, and an Enhanced Integrated Device Electronics (EIDE) interface 186. The core logic chipset 190 is coupled to a processor (Central Processing Unit or CPU) 152, peripherals such as a hard disk drive 164 and a Digital Versatile Disk (DVD) CD-ROM 166, a bus such as a PCI bus 170, the arbiter 82, and the main memory 168.

In this embodiment, the main memory 168 is the memory 50 to which the memory interfaces 72 and 76 are coupled. The main memory 168 is coupled to the memory interfaces 72 and 76 through a memory bus 167. In current technology the memory bus 167, which corresponds to the fast bus 70 for coupling the core logic chipset to the memory, is capable of having a bandwidth of approximately 400 Mbytes/s. This bandwidth is at least twice the bandwidth required for an optimized decoder/encoder 80, allowing the decoder/encoder 80 to operate in real time.

The core logic chipset 190 can also be coupled to cache memory 162 and a graphics accelerator 200 if one is present in the computer. The PCI bus 170 is also coupled to the graphics accelerator 200 and to other components, such as a Local-Area Network (LAN) controller 172. The graphics accelerator 200 is coupled to a display 182 and a frame buffer 184. The graphics accelerator can also be coupled to an audio codec 180 for decoding and/or encoding audio signals.

Figure 4 shows another embodiment of a computer where the decoder/encoder 80 is sharing the main memory 168. In this embodiment, the main memory 168 corresponds to the shared memory 50 of Figure 2. In Figure 4, the decoder/encoder 80 according to the present invention is connected as a peripheral to a conventional computer equipped with a fast peripheral bus 170, for example, a PCI bus, although the bus can be VESA Local Bus (VLB), an Accelerated Graphics Port (AGP) bus, or any bus having the required bandwidth. In this embodiment, the fast peripheral bus 170 corresponds to the fast bus 70. As shown, the decoder/encoder 80 does not have a dedicated memory, but utilizes a region 22' of the main memory 168 of the computer.

Region 22' includes a Compressed Data Buffer (CDB), into which image source 122 writes the compressed image data, and two image buffers M1 and M2 associated with intra or predicted images. As will be seen hereafter, a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded.

Thus, in the system of Figure 4, compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168. These same compressed data are then transferred to the decoder/encoder 80 which, if they correspond to intra or predicted images, retransmits them in decoded form to buffers Ml and M2 of memory 168. In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data. The display adapter then supplies these data to a display device such as a screen. The intra or predicted images stored in buffers M1 and M2 are transferred to display adapter 120 at the appropriate time and are used in the decoding of subsequent predicted or bidirectional images.

With a decoder/encoder 80 according to the invention, the rates on peripheral bus 170 are particularly high, which is why a fast bus is needed. However, the rate required is substantially decreased due to the bidirectional images not being stored in main memory 168, but being directly sent to display adapter 120. According to the invention, the bandwidth used on a PCI bus is approximately 20% with an MPEG-1

decoder/encoder and approximately 80% with an MPEG-2 decoder/encoder. These bandwidths correspond to worst case situations. The bandwidth in typical operation can be lower.

Of course, the storage capacity of the main memory 168 available for other uses is reduced during the operation of the decoder/encoder 80 because the decoder/encoder 80 is using the memory region 22'. However, in this embodiment the size of region 22' is decreased from the size of the dedicated memory 22 used in the prior art (Figures 1a and 1c) by one image buffer. The memory region 22' is also only occupied while viewing video sequences. When the decoder/encoder is no longer used, memory region 22' can be freed at once for the other tasks.

The modifications to be made on the computer to use a decoder/encoder according to the invention primarily involve software changes and are within the capabilities of those skilled in the art, who will find the necessary information in the various standards relating to the computer. For the computer to be able to use its peripherals, it conventionally executes background programs called peripheral drivers, which translate specific addresses issued by the CPU or a master peripheral (such as the decoder/encoder 80) into addresses adapted to the variable configuration of the computer.

For example, a peripheral driver associated with the decoder/encoder according to the invention translates the fixed addresses issued by the decoder/encoder 80 to have access to its image memory into addresses corresponding to the physical location of region 22', this region being likely to be variably assigned by the operating system according to the occupancy of memory 168. Similarly, this peripheral driver answers requests issued by image source 122 to supply compressed data by transferring these data into buffer CDB of region 22'.

In an alternative embodiment the third image buffer M3 (Figure 1c) remains in the memory region 22' used for the decoder/encoder 80. A conventional decoder/encoder should be able to be used in several applications, especially to supply television images. In the case of television, the images are supplied in interlaced form, that is, all the odd lines of an image are supplied prior to the even lines. An MPEG decoder

generally reconstructs the images in progressive form, that is, it supplies the image lines consecutively. The third image buffer M3 is then necessary to store the bidirectional images in the order of arrival of the lines (in progressive form) and then reread this image in interlaced form. The third image buffer M3 may also be needed if there is a delay between when the images are decoded and when they can be viewed, requiring the images to be stored.

Figure 5 illustrates the use of memory region 22' in the decoding according to the invention of sequence 10, P1, B2, B3, P4, B5, B6, P7. Image I0 is stored in buffer M1 during its decoding. As the decoding and the storage in buffer M2 of image P1 begins, image I0 is displayed. The macroblocks used to decode image P1 are fetched from buffer M1. Images B2 and B3 are displayed as they are being decoded, the macroblocks used for their decoding being fetched from buffers M1 and M2. Image P1 is displayed while image P4 is being decoded and stored in buffer M1 in the place of image I0. Image P1 is kept in buffer M2 until image B6 is decoded and displayed, and so on.

Figure 6 shows an architecture of an MPEG decoder according to the invention. Like any conventional MPEG decoder, this decoder includes a Variable Length Decoder (VLD) receiving compressed data from a First-In, First-Out (FIFO) memory 30. The VLD is followed by a Run-Level Decoder (RLD), an inverse quantization circuit Q-1 and an inverse discrete cosine transform circuit DCT-1. The output of circuit DCT-1 is supplied to a first input of an adder 32, a second input of which receives macroblocks of a previously decoded image via a filter 34 and a FIFO 35. The decoded image data are supplied by the output of adder 32 and via a FIFO 37. FIFO 30 is supplied with compressed data from bus 10 via an interface circuit PCI I/F 39.

A decoder according to the invention differs from a conventional decoder in that the interface circuit 39 also connects FIFOs 35 and 37 to bus 170. A memory controller 41 calculates and supplies through bus 170 the addresses corresponding to the various exchanges required.

The management of the addresses of buffers M1 and M2 is similar to that performed by the memory controller of a conventional decoder, since these addresses are,

according to the invention, translated according to the physical location of these buffers in memory 168 by a peripheral driver. Moreover, the memory controller of a decoder/encoder 80 according to the preferred embodiment of the invention is substantially simplified due to the absence of the third image buffer M3. The memory controller of a conventional decoder has to manage this buffer in a specific way to avoid a bidirectional image under decoding being written over a bidirectional image under display.

Figure 7 shows a computer where the decoder/encoder 80 is sharing a frame buffer 184 with a graphics accelerator 200. The graphics accelerator 200 can be any graphics accelerator known in the art. In the embodiment shown in Figure 7, the graphics accelerator 200 contains a Two-Dimensional (2D) accelerator 204, a Three-Dimensional (3D) accelerator 206, a Digital to Analog Converter (DAC) 202, a memory interface 72, and bus interface 210 for any system busses 170 to which it is coupled. The graphics accelerator 200 can also contain an audio compressor/decompressor 208, here an AC-3 decoder. The graphics accelerator 200 is coupled to a display 182, and a frame buffer 184.

In this embodiment, the frame buffer 184 is the memory 50 to which the memory interfaces 72 and 76 are coupled. The frame buffer 184 is coupled to the memory interfaces 72 and 76 through a memory bus 185. In this embodiment, memory bus 185 corresponds to the fast bus 70. In current technology the memory bus 185 for coupling a graphics accelerator to a memory is capable of having a bandwidth of up to 400 Mbytes/s. This bandwidth is more that twice the bandwidth required for an optimized decoder/encoder 80. This allows the decoder/encoder 80 to operate in real time.

The graphics accelerator 200 can also be coupled to an audio codec 180 for decoding and/or encoding audio signals. The PCI bus 170 is also coupled to a chipset 190, and to other components, such as a LAN controller 172. In the present embodiment the chipset is a PCI chipset, although it can be any conventional chipset. The chipset 190 is coupled to a processor (CPU) 152, main memory 168, and a PCI bridge 192. The PCI bridge bridges between the PCI bus 170 and the ISA bus 198. The ISA bus 198 is coupled to peripherals, such as a modem 199 and to an EIDE interface 186, which is coupled to other peripherals, such as a hard disk drive 164 and a DVD CD-ROM 166, although, if the

peripherals are compatible to the PCI bus the EIDE interface 186 can be integrated into the PCI chipset 190 and the peripherals 164 and 166 can be coupled directly to the PCI chipset, eliminating the PCI bridge 192 and the ISA bus 198.

Referring to Figure 2, the operation of the arbiter 82 during a memory request will now be described. During operation the decoder/encoder 80, the first device 42, and the refresh logic 58, if it is present, request access to the memory through the arbiter 82. There may also be other devices that request access to the memory 50 through this arbiter. The arbiter 82 determines which of the devices gets access to the memory 50. The decoder/encoder gets access to the memory in the first time interval, and the first device gets access to the memory in the second time interval. The Direct Memory Access (DMA) engine 52 of the decoder/encoder 80 determines the priority of the decoder/encoder 80 for access to the memory 50 and of the burst length when the decoder/encoder 80 has access to the memory. The DMA engine 60 of the first device determines its priority for access to the memory 50 and the burst length when the first device 42 has access to the memory.

The decoder/encoder 80 or one of the other devices generates a request to access the memory 50. The request will be transferred to the arbiter 82. The state of the arbiter 82 is determined. The arbiter typically has three states. The first state is idle when there is no device accessing the memory and there are no requests to access the memory. The second state is busy when there is a device accessing the memory and there is no other request to access the memory. The third state is queue when there is a device accessing the memory and there is another request to access the memory.

It is also determined if two requests are issued simultaneously. This can be performed either before or after determining the state of the arbiter. Access to the memory is determined according to the following chart.

Arbiter state	Simultaneous requests	Action
Idle	Yes	One of the requests gets access to the memory based on the priority scheme, and the other request is queued.
Busy	Yes	Both requests are queued in an order based on the priority scheme.
Queue	Yes	Both requests are queued in an order based on the priority scheme.
Idle	No	The device gets access to the memory.
Busy	No	The request is queued.
Queue	No	The requests are queued in an order based on the priority scheme.

The priority scheme can be any priority scheme that ensures that the decoder/encoder 80 gets access to the memory 50 often enough and for enough of a burst length to operate properly, yet not starve the other devices sharing the memory. The priority of the first device, device priority, and the priority of the decoder/encoder 80, decoder priority, are determined by the priority scheme. This can be accomplished in several ways.

To operate in real time, the decoder/encoder 80 has to decode an entire image in time to be able to display it the next time the screen is refreshed, which is typically every 1/30 of a second. The decoder/encoder 80 should get access to the memory to store and retrieve parts of this and/or of past and/or future images, depending on the decoding standard being used, often enough and for long enough burst lengths to be able to decode the entire image in the 1/30 of a second between screen refreshes.

There are many ways to do this. One way is to make the burst length of the first device and any other device like the screen refresh that shares the memory and memory interface (hereinafter sharing device) have short burst lengths, and to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. Another way is to preempt the sharing device if its

burst length exceeds a burst length threshold and again to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. Preferably, when the preemption is used the sharing device would be preempted when its burst length exceeds 16 words. A third way is to limit the bandwidth available to the sharing devices. This way the decoder/encoder 80 always has enough bandwidth to operate in real time. Preferably the bandwidth of the sharing devices is limited only when the decoder/encoder 80 is operating. In the preferred embodiment a memory queue such as a FIFO in the decoder/encoder 80 generates an error signal when it falls below a data threshold. The error is sent to the CPU 152 and the CPU 152 can either shut down the system, drop an image frame or resume the decoding/encoding process.

There are also many ways to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. This both ensures that the decoder/encoder 80 gets access to the memory 50 often enough, yet does not starve the other devices sharing the memory. One way to do this is to disallow back-to-back requests. Another is to have shifting priority, where a particular request starts with a lower priority when first made, and the priority increases with the length of time the request is in the queue, eventually reaching a priority above all of the other requests. In the preferred embodiment, the decoder/encoder 80 has a one-clock cycle delay between requests to allow a sharing device to generate a request between the decoder/encoder requests.

In the preferred embodiment of the invention, the burst length of the decoder/encoder is relatively short, approximately four to seventeen words. This allows the graphics accelerator more frequent access to the memory to ensure that the display is not disturbed by the sharing of the memory interface 48 and memory 50 when the decoder/encoder shares a memory with the graphics accelerator 200.

An electronic system 40, shown in Figure 2, containing the first device 42 coupled to the memory 50, the decoder/encoder 80 coupled to the same memory 50, where the decoder/encoder 80 shares the memory 50 with the first device 42 provides several advantages. Referring to Figure 2 and Figure 1b simultaneously, the decoder 44 and

encoder 46 according to the preferred embodiment of the invention do not each need their own dedicated memory 22 that was necessary in the prior art for the decoder/encoder to operate in real time, resulting in significant reduction in the cost of the device. Allowing the decoder/encoder 80 to share the memory 50 with a first device 42 and to allow the decoder/encoder 80 to access the memory 50 through a fast bus 70 having a bandwidth of a least the bandwidth threshold permits the decoder/encoder to operate in real time. This reduces stops between images and the dropping of a significant number of frames to a point where both are practically eliminated. This produces better images and eliminates any discontinuities and delays present in the prior art.

Additionally, in the embodiment of the invention where the fast bus 70 is a system bus to which the decoder/encoder 80 is already coupled, the number of pins of the decoder/encoder 80 is considerably smaller than that of a conventional decoder. The decoder/encoder according to the invention only requires the signals of the peripheral bus 170 (49 signals for the PCI bus), while a conventional decoder further includes an interface with its dedicated memory 22, which is typically an external memory.

Thus, decoding in a computer can be performed according to the invention by means of a low-cost (due to the small number of pins) single integrated circuit, without the additional, costly, dedicated memory 22. This single integrated circuit can be directly placed on the computer motherboard for a low additional cost. 0f course, the decoder/encoder according to the invention can be mounted, as is conventional, on an extension board to be connected to a bus.

A further advantage of the present invention is that the video and/or audio decompression and/or compression device can share memory with the first device without being integrated into the first device. This allows the first device to be a standard device with some adjustments made to its memory interface.

Further background on compression can be found in: International Organization for Standards, *Information Technology - Coding of Moving Pictures and Associated Audio for Digital Storage Media at up to About 1.5 Mbits/S*, Parts 1-6, International Organization for Standards; International Standards Organization,

Information Technology - Generic Coding of Moving Pictures and Associated Audio Information, Parts 1-4, International Organization for Standards; Datasheet "STi3500A" Datasheet of SGS-THOMSON Microelectronics; STi3500A - Advanced Information for an MPEG Audio/ MPEG-2 Video Integrated Decoder" (June 1995); Watkinson, John, *Compression in Video and Audio*, Focal Press, 1995; Minoli, Daniel, *Video Dialtone Technology*, McGraw-Hill, Inc., 1995. Further background on computer architecture can be found in Anderson, Don and Tom Shanley, *ISA System Architecture*, 3rd ed., John Swindle ed., MindShare Inc., Addison-Wesley Publishing Co., 1995. All of the above references are incorporated herein by reference.

While the invention has been specifically, described with reference to several preferred embodiments, it will be understood by those of ordinary skill in the prior art having reference to the current specification and drawings that various modifications may be made and various alternatives are possible therein without departing from the spirit and scope of the invention. For example: Although the memory is described as DRAM, other types of memories including read-only memories, Static Random Access Memories (SRAMs), or FIFOs may be used without departing from the scope of the invention.

Any conventional decoder including a decoder complying to the MPEG-1, MPEG-2, H.261, or H.261 standards, or any combination of them, or any other conventional standard can be used as the decoder/encoder.

CLAIMS

1. An electronic system comprising:

a bus couplable to a main memory having stored therein data corresponding to images to be decoded and also decoded data corresponding to images that have previously been decoded;

a decoder coupled to the bus for receiving compressed images and for outputting data for displaying the decoded images on a display device, the decoder receiving data from the main memory corresponding to at least one previously decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being stored in the main memory;

a microprocessor system coupled to the main memory, the microprocessor system storing non-image data in and retrieving data from the main memory; and

an arbiter circuit coupled to both the microprocessor system and the decoder for controlling the access to said main memory by the decoder and the microprocessor.

2. An electronic system according to claim 1, wherein the decoder directly supplies a display adapter with an image under decoding which is not used to decode a subsequent image.

3. An electronic system according to claim 1, wherein the memory stores intra images which are not obtained from a preceding image and predicted images which are obtained from a single preceding image, the images directly supplied to the display adapter being bidirectional images obtained from two preceding intra or predicted images.

4. An electronic system according to claim 1, wherein the decoder is integrated into a computer motherboard.

5. A method of outputting data corresponding to an image to be displayed, comprising:

storing within a main memory data corresponding to images to be decoded and also data corresponding to images that have previously been decoded;

transferring from the memory to a decoder on a first bus, data corresponding to an image to be decoded;

transferring from the main memory to a decoder data corresponding to images that have been previously decoded;

decoding, within the decoder, the current image using data corresponding to the current image and also using data corresponding to one or more previously decoded images;

outputting to the main memory data corresponding to the current image most recently decoded;

storing in the main memory decoded data corresponding to the most recently decoded image;

processing data that does not contain image information within a microprocessor;

storing the non-image data in said main memory by transferring the data from the microprocessor on the first bus;

transferring the non-image data from the main memory to the microprocessor on the first bus;

receiving signals in an arbitration circuit from the decoder and from the microprocessor; and

arbitrating access to said main memory via the arbitration circuit between the decoder and microprocessor.

6. An electronic system comprising:

a fast bus couplable a main memory having stored therein data corresponding to images to be decoded, decoded data corresponding to images that have previously been decoded, and non-image data that contains information other than image information and does not contain any image information;

a plurality of bus interfaces coupled to the fast bus;

a decoder coupled to the main memory via a first bus interface and adapted to receive compressed images and output a data stream of decoded images adapted to be displayed on a display device, the decoder receiving data from the main memory corresponding to at least one previously decoded and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being stored in the main memory;

a central processing circuit coupled to the main memory via a second bus interface, the central processing circuit storing non-image data in and retrieving non-image data from the main memory; and

an arbiter circuit coupled to the decoder and to the second bus interface of the central processing circuit for controlling access to the bus via the respective bus interfaces of data to and from the first bus interface of the central processing circuit and the decoder.

7. An electronic circuit for use with a bus coupled to a system memory and a device, comprising:

a video decoder coupled to the bus for receiving compressed video images and for outputting video data for displaying the video decoded images on a display device, the video decoder configured to receive data from the system memory corresponding to at least one previously decoded image and to a current image to be decoded and configured to output decoded data corresponding to a current image to be displayed, the current image being stored in system memory; and

a memory arbiter coupled to both the device and the video decoder configure to control access to the system memory by the video decoder and the device.

8. An electronic circuit according to claim 7, wherein the decoder directly supplies a display device with an image under decoding which is not used to decode a subsequent image.

9. An electronic circuit according to claim 7, wherein the device is a microprocessor system.

10. An electronic circuit according to claim 7, wherein the decoder and arbiter circuit are integrated into a computer motherboard.

11. An electronic circuit according to claim 7, wherein the decoder and arbiter are integrated into a single chip.

12. An electronic circuit according to claim 7, wherein the compressed images are encoded in the MPEG standard.

13. An electronic circuit for use with a memory, comprising:

a bus couplable to the memory;

a decoder coupled to the bus for receiving compressed images and for outputting data for displaying the decoded images on a display device, the decoder receiving data from the memory corresponding to at least one previously decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being stored in the memory;

a central processing unit coupled to the bus for accessing memory; and

an arbiter coupled to the decoder and to the central processing unit for controlling access to the bus.

14. An electronic circuit according to claim 13, wherein the decoder directly supplies a display device with an image under decoding which is not used to decode a subsequent image.

15. An electronic circuit according to claim 13, wherein the bus, decoder, central processing unit, and arbiter are integrated into a computer motherboard.

16. An electronic circuit according to claim 13 wherein the bus, decoder, central processing unit, and arbiter are integrated into a single chip.

17. An electronic circuit according to claim 13, wherein the compressed images are encoded in the MPEG standard.

18. An electronic circuit according to claim 13, wherein the central processing unit stores non-image data in and retrieves data from the memory.

19. The method according to claim 5 wherein receiving signals in the arbitration circuit is carried out by receiving signals on a separate signal path than the first bus.

20. The circuit according to claim 7 further including an independent signal path, separate from the bus, by which the arbiter is coupled to the device and the video decoder.

ABSTRACT OF THE DISCLOSURE

An electronic system, an integrated circuit and a method for display are disclosed. The electronic system contains a first device, a memory and a video/audio compression/decompression device such as a decoder/encoder. The electronic system is configured to allow the first device and the video/audio compression/decompression device to share the memory. The electronic system may be included in a computer in which case the memory is a main memory. Memory access is accomplished by one or more memory interfaces, direct coupling of the memory to a bus, or direct coupling of the first device and decoder/encoder to a bus. An arbiter selectively provides access for the first device and/or the decoder/encoder to the memory. The arbiter may be monolithically integrated into a memory interface. The decoder may be a video decoder configured to comply with the MPEG-2 standard. The memory may store predicted images obtained from a preceding image.

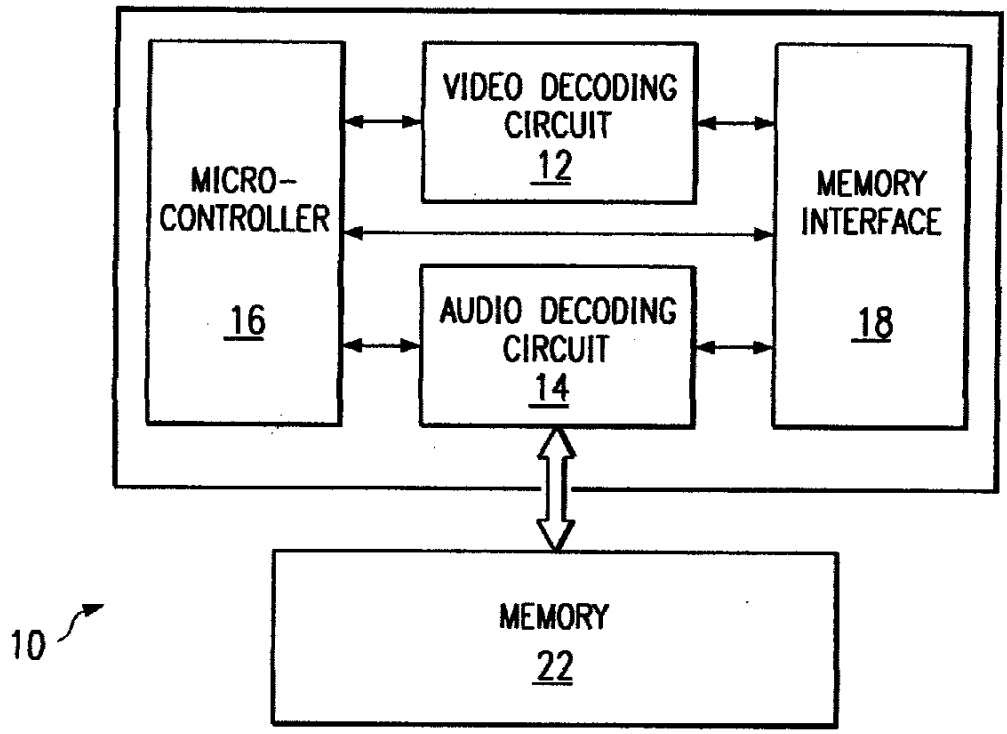


Fig. 1a
(Prior Art)

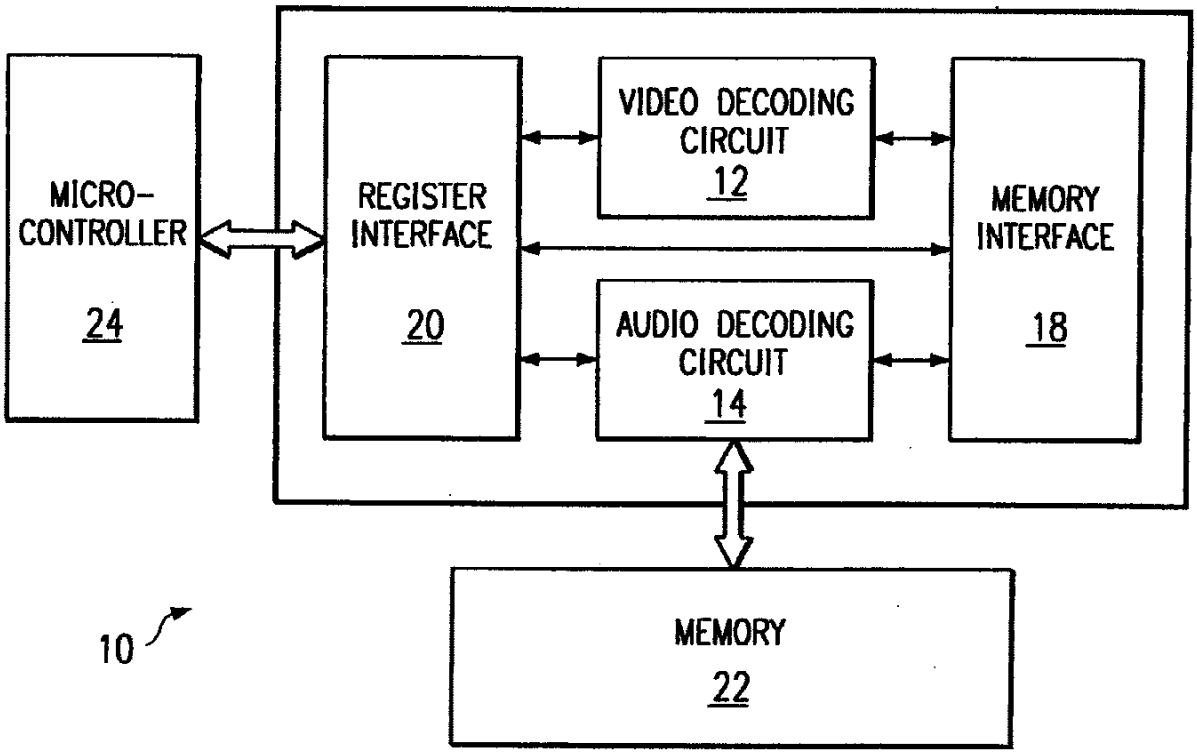


Fig. 1b
(Prior Art)

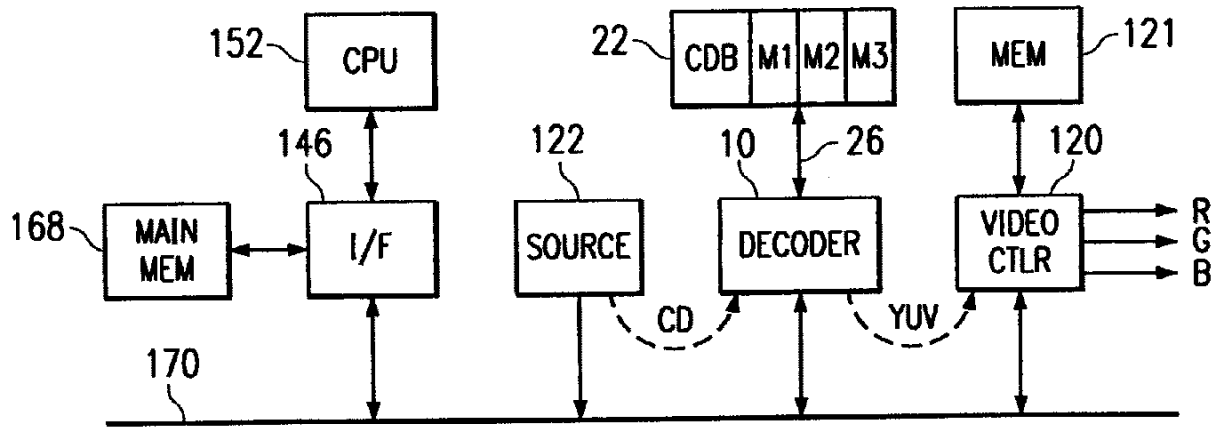


Fig. 1c
(Prior Art)

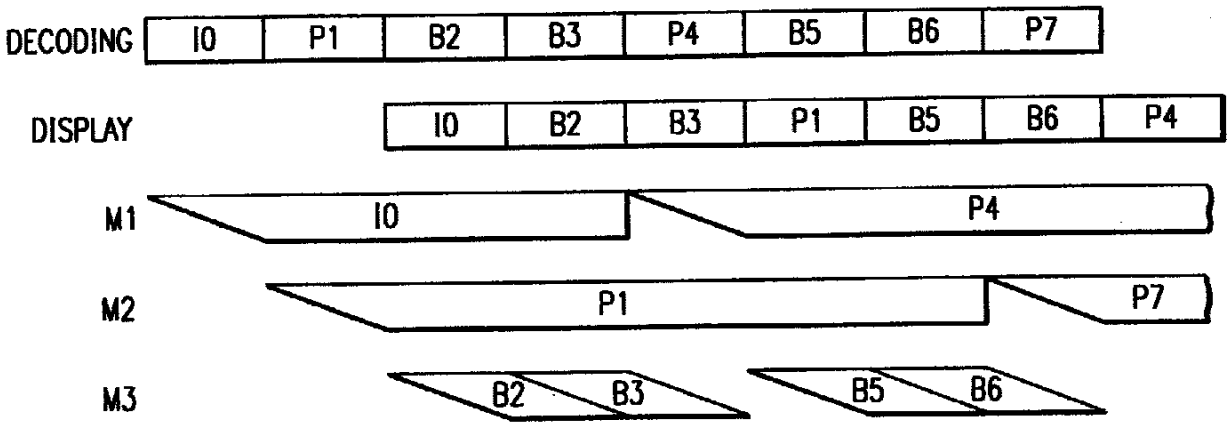


Fig. 1d
(Prior Art)

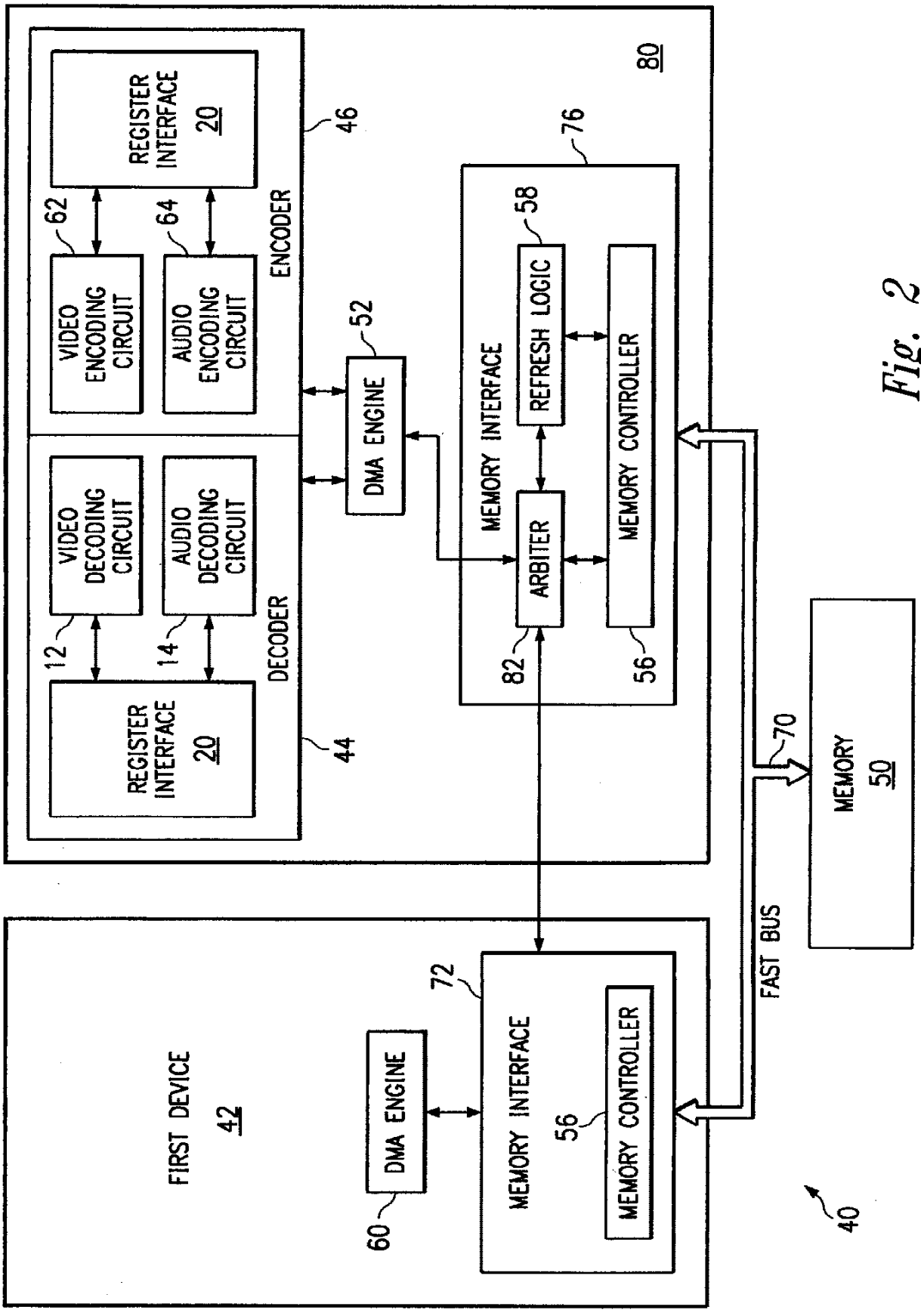
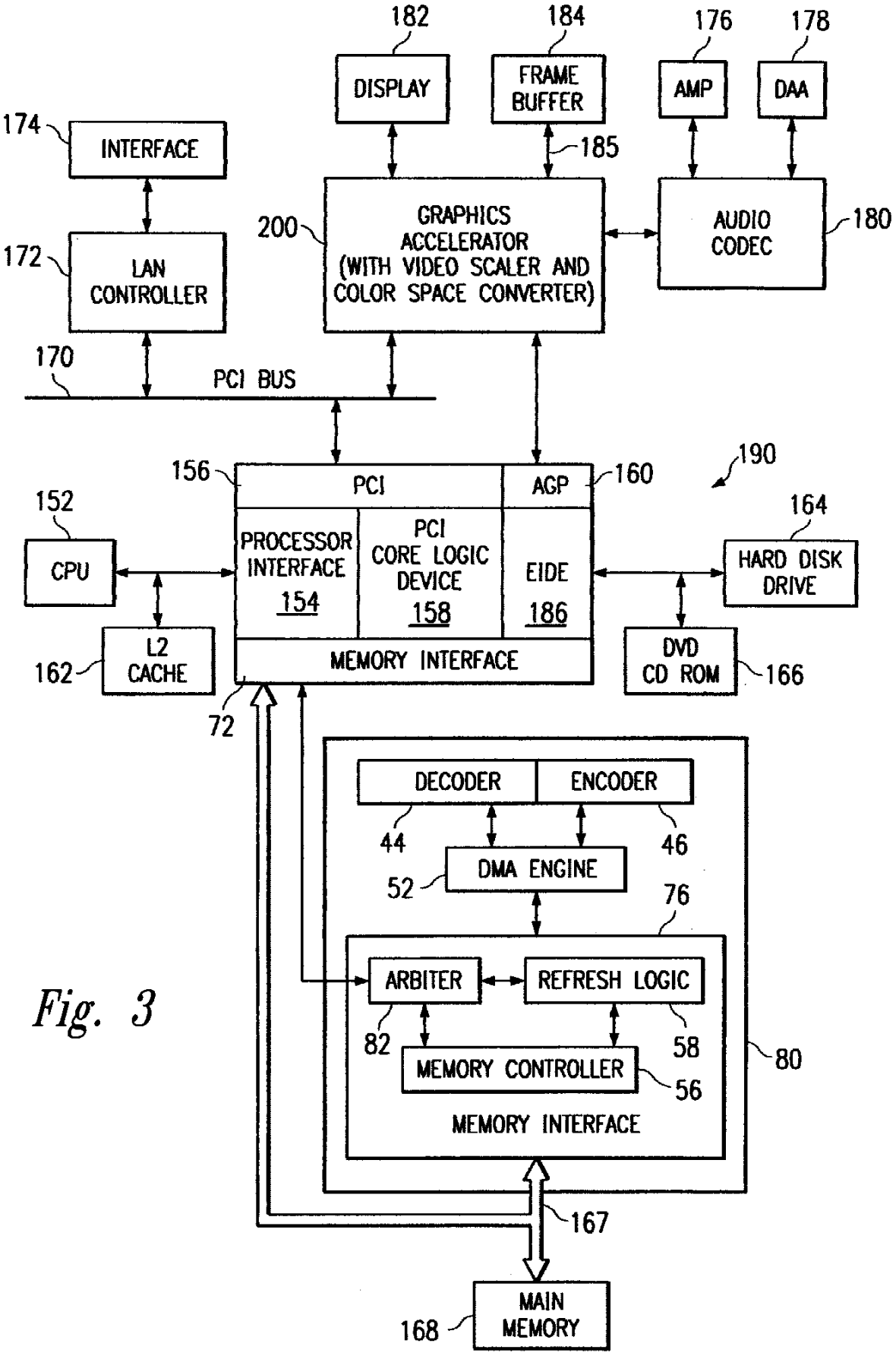

80
ENCODER
46
REGISTER INTERFACE 20
62
64
VIDEO ENCODING CIRCUIT
AUDIO ENCODING CIRCUIT
DECODER
44
VIDEO DECODING CIRCUIT
AUDIO DECODING CIRCUIT
12
14
REGISTER INTERFACE 20
DMA ENGINE
52
MEMORY INTERFACE
76
REFRESH LOGIC
58
ARBITER
82
MEMORY CONTROLLER
56
70
MEMORY 50
FAST BUS
FIRST DEVICE 42
DMA ENGINE
60
72
MEMORY INTERFACE
56
MEMORY CONTROLLER
40

Fig. 2


182
184
176
178
DISPLAY
FRAME BUFFER
AMP
DAA
174
INTERFACE
185
200
GRAPHICS ACCELERATOR (WITH VIDEO SCALER AND COLOR SPACE CONVERTER)
AUDIO CODEC
180
172
LAN CONTROLLER
170
PCI BUS
190
156
PCI
AGP
160
152
164
CPU
PROCESSOR INTERFACE 154
PCI CORE LOGIC DEVICE 158
EIDE 186
HARD DISK DRIVE
L2 CACHE
162
MEMORY INTERFACE
DVD CD ROM
166
72
DECODER
ENCODER
44
46
DMA ENGINE
52
76
ARBITER
REFRESH LOGIC
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MEMORY INTERFACE
167
MAIN MEMORY
168

Fig. 3

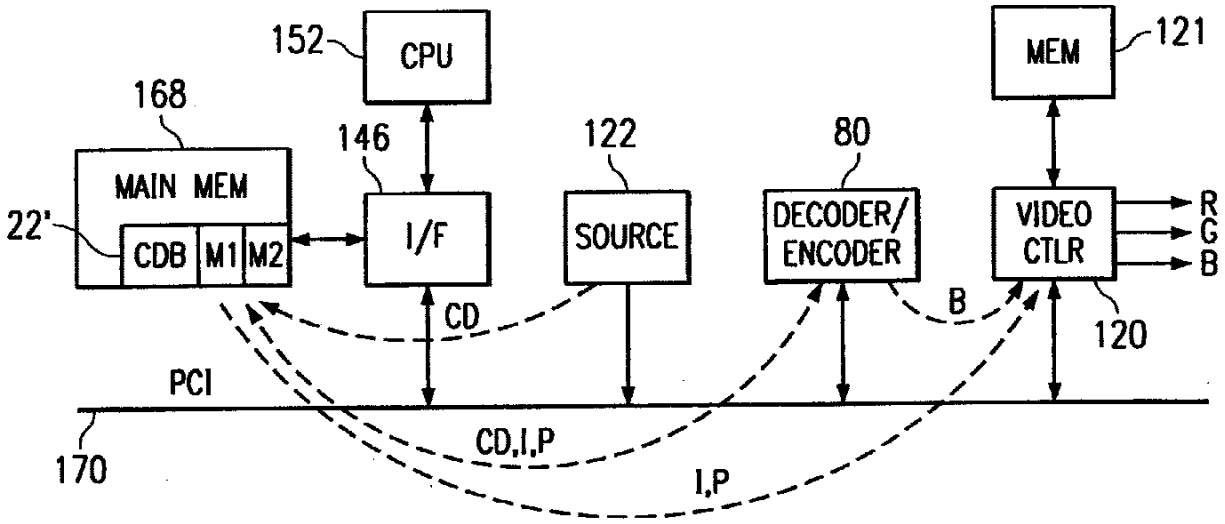


Fig. 4

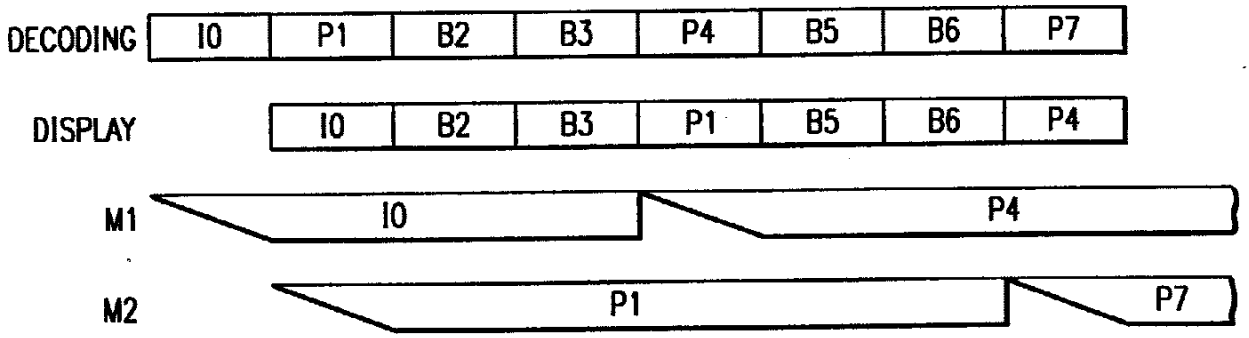


Fig. 5

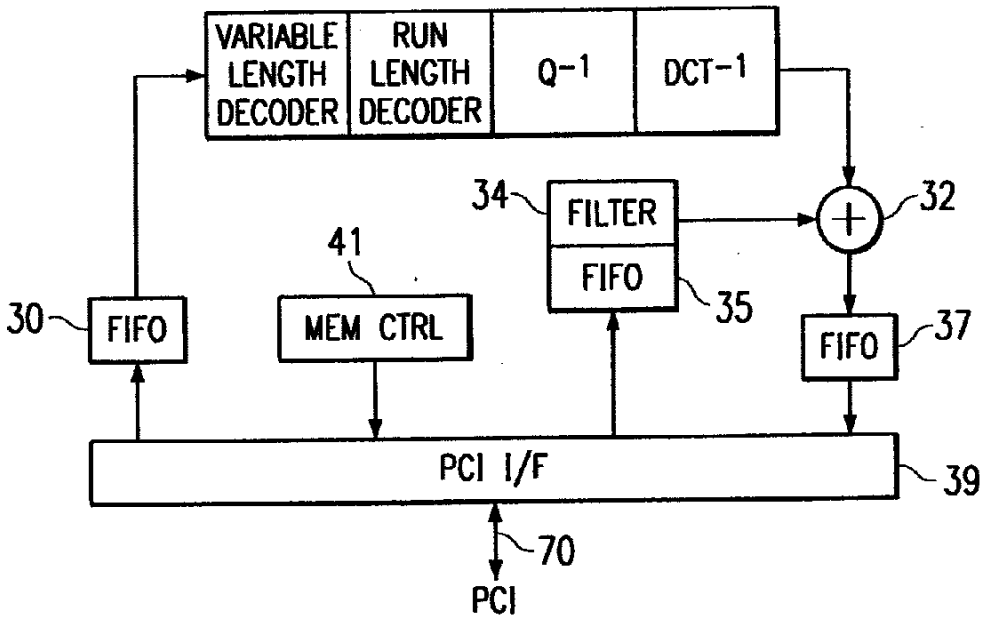
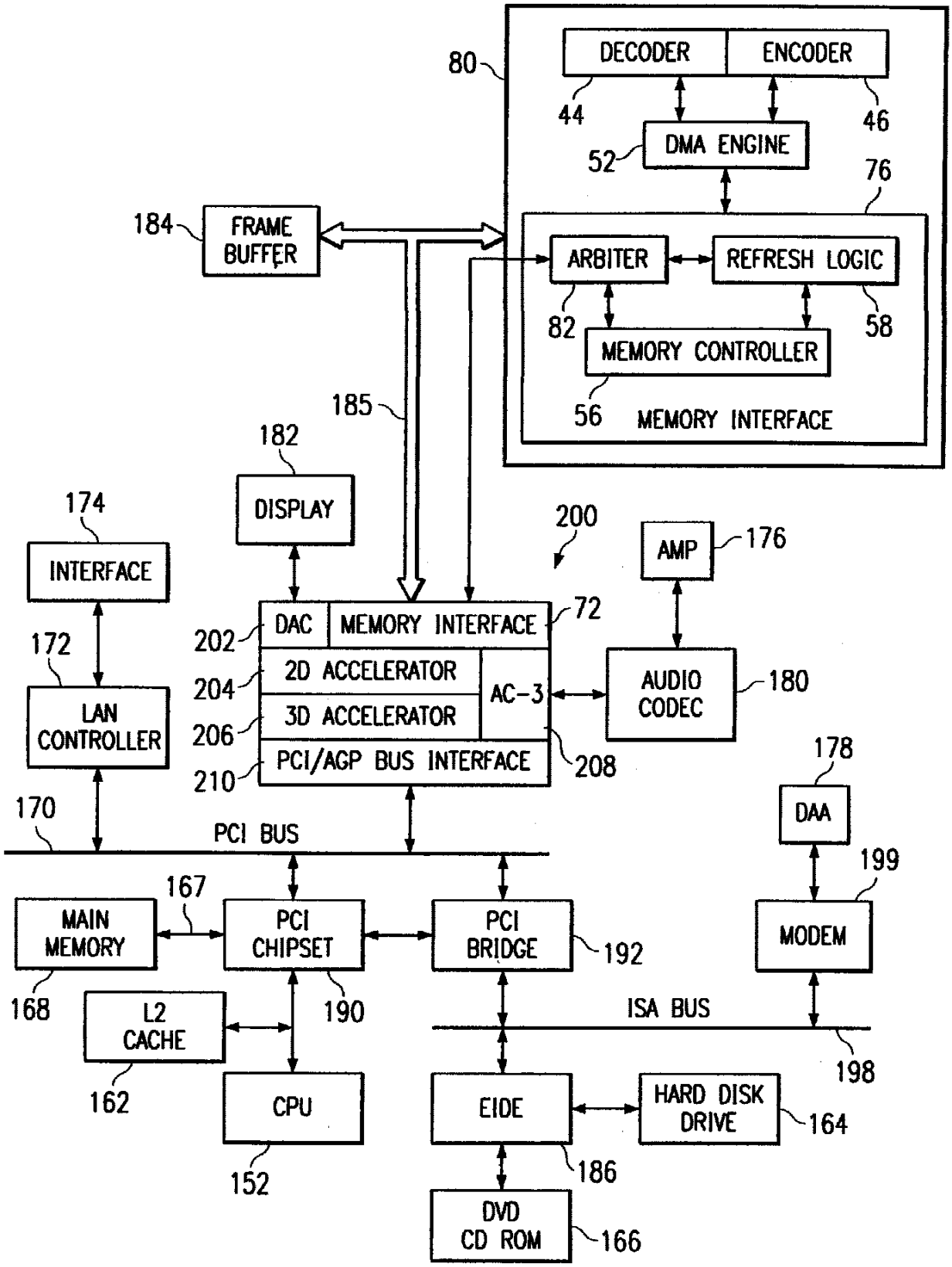


Fig. 6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DECODER
ENCODER
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DMA ENGINE
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FRAME BUFFER
ARBITER
REFRESH LOGIC
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MEMORY CONTROLLER
56
MEMORY INTERFACE
185
182
DISPLAY
174
INTERFACE
200
AMP
176
172
202
DAC
MEMORY INTERFACE
72
204
2D ACCELERATOR
AC-3
AUDIO CODEC
180
206
3D ACCELERATOR
LAN CONTROLLER
208
210
PCI/AGP BUS INTERFACE
178
DAA
170
PCI BUS
199
167
MAIN MEMORY
PCI CHIPSET
PCI BRIDGE
192
MODEM
168
L2 CACHE
190
ISA BUS
198
162
CPU
EIDE
HARD DISK DRIVE
164
152
186
DVD CD ROM
166

Fig. 7

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Video and/or Audio Decompression and/or Compression Device that Shares a Memory

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Lisa K. Jorgenson, Reg. No. 34,845 and Irena Lager, Reg. No. 39,260 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

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PTO/SB/06 (12-04)

Filing Date: **12/13/07**

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 11/956,165

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	310
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	510
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	210
TOTAL CLAIMS (37 CFR 1.16(i))	20		X$ 25		OR	X$50	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	* 2	X$105			X$210	420
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					260	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			185			370	
			TOTAL	0		TOTAL	1450

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.