Developer Note

Macintosh Quadra 840AV and Macintosh Centris 660AV Computers

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About This Developer Note

This developer note introduces the Macintosh Quadra 840AV and the Macintosh Centris 660AV, Apple's newest extensions to the Macintosh family of personal computers. It is written primarily for experienced Macintosh hardware and software engineers who want to create products that are compatible with these computers.

This note assumes that you are already familiar with both the functionality and programming requirements of Macintosh computers. If you are unfamiliar with Macintosh computers or would like more technical information, you may want to obtain copies of the related technical manuals listed in "Supplementary Documents," later in this preface.

Contents of This Note

This developer note is divided into four main parts, containing a total of 13 chapters.

Part 1, "Hardware," describes the Macintosh Quadra 840AV and Macintosh Centris 660AV computers from a hardware viewpoint. It contains two chapters:

- Chapter 1, "The Macintosh Quadra 840AV and Macintosh Centris 660AV Computers," gives you an overview of the configurations and features of these products.
- Chapter 2, "Hardware Details," describes the circuit boards for the computers, including their physical layout, functional units, signal timing and other electronic characteristics, input and output connectors, and interfaces with other equipment.

Part 2, "Real-Time Data Processing," describes the software technology of the digital signal processing (DSP) facilities in the Macintosh Quadra 840AV and Macintosh Centris 660AV. It contains three chapters:

- Chapter 3, "Introduction to Real-Time Data Processing," summarizes the software architecture of their real-time data processing facility. This facility consists of an AT&T DSP3210 chip that performs data-processing operations for applications that contain DSP code.
- Chapter 4, "Real Time Manager," describes a new part of the Macintosh system software that supplies all the services an application requires to use the digital signal processor, including loading and running DSP code and performing DSP memory management.
- Chapter 5, "DSP Operating System," covers the DSP operating system, contained in the DSP chip. It provides the services every DSP program needs to work with the Macintosh Operating System.

Part 3, “Speech Synthesis and Recognition,” explains the capabilities of the Macintosh Quadra 840AV and Macintosh Centris 660AV system software for generating and understanding human speech. It contains three chapters:

- Chapter 6, “Speech Manager,” describes a new Macintosh system software manager that provides a standardized way for applications to generate synthesized speech. The Speech Manager also lets an application control one or more speech synthesizers, which generate spoken sound in specific languages, intonations, and speaking styles.
- Chapter 7, “Introduction to Speech Recognition,” contains a basic tutorial for the Speech Setup control panel. This control panel provides commands for controlling the speech recognition function.
- Chapter 8, “Speech Rules,” explains the speech rules that are built into the Macintosh Quadra 840AV and Macintosh Centris 660AV system software.

Part 4, “System Software Modifications,” describe miscellaneous changes to the Macintosh Quadra 840AV and Macintosh Centris 660AV system software, including a new manager for the internal and external SCSI (Small Computer System Interface) ports. It contains five chapters:

- Chapter 9, “SCSI Manager 4.3,” describes the new SCSI Manager.
- Chapter 10, “DMA Serial Driver,” details the new hardware-independent serial driver that uses direct memory access (DMA).
- Chapter 11, “Video Driver,” describes changes to the video driver.
- Chapter 12, “New Age Floppy Disk Driver,” lists changes to the floppy disk driver and tells you how they affect floppy disk compatibility with other Macintosh computers.
- Chapter 13, “Virtual Memory Manager,” details how the Virtual Memory Manager no longer disables interrupts when performing certain tasks.

Four appendixes follow the main parts of this note. They contain information that can help you with specific development tasks:

- Appendix A, “DSP d Commands for MacsBug,” describes three new `d` commands added to Macsbug that help in debugging DSP code.
- Appendix B, “BugLite User’s Guide,” describes a DSP module installer with a graphical user interface. It helps programmers create and install tasks to be executed by the DSP.
- Appendix C, “Snoopy User’s Guide,” tells you how to use a browser and debugger for the DSP. It helps programmers debug real-time tasks that run on the DSP.
- Appendix D, “Mechanical Details” contains foldout drawings of the physical mounting facilities that are provided for internal SCSI devices and accessory cards in the Macintosh Quadra 840AV and Macintosh Centris 660AV.

At the end of this developer note are a glossary and an index. Terms listed in the glossary are printed in **boldface** where they are first defined in the text.

Hardware Overview

The Macintosh Quadra 840AV and Macintosh Centris 660AV have the most features of any models in the Macintosh family of desktop computers. The Macintosh Quadra 840AV is also the fastest Macintosh computer. The two models have nearly identical electronic circuitry. Their differences are that the Macintosh Quadra 840AV is housed in a minitower enclosure with more room for internal disk drives and accessory cards, while the Macintosh Centris 660AV is housed in a low-profile enclosure designed to be placed under the user's monitor. The Macintosh Centris 660AV also offers somewhat lower speed and performance than the Macintosh Quadra 840AV and sells for a lower price.

Principal new hardware features of these computers include

- digital signal processing, using an AT&T DSP3210 chip
- video input and output facilities in NTSC, PAL, and SECAM formats
- high-quality sound processing
- direct memory access for peripheral devices
- integrated telephone I/O for ISDN, fax, and other signal forms

Chapter 1, "The Macintosh Quadra 840AV and Macintosh Centris 660AV Computers," describes these and other hardware features; Chapter 2, "Hardware Details," provides deeper technical information.

Software Overview

The Macintosh Quadra 840AV and Macintosh Centris 660AV are supplied with essentially identical versions of the Macintosh System 7.1 software, in ROM and on the internal hard disk. For technical information about standard System 7.1 software, see *Inside Macintosh,* listed in "Supplementary Documents," later in this preface. However, the system software in the Macintosh Quadra 840AV and Macintosh Centris 660AV also contains significant changes and additions to System 7.1. This section summarizes those changes and additions, which are described in greater detail in Chapters 3 through 13.

Digital Signal Processing

The Macintosh Quadra 840AV and Macintosh Centris 660AV use a digital signal processor (DSP) chip separate from the main microprocessor to perform real-time data processing, such as playing sound files. In addition, the DSP chip can perform processing-intensive operations that do not require real-time execution, such as file compression and three-dimensional drawing. Chapter 3, "Introduction to Real-Time Data Processing," explains this capability in more detail.

To take advantage of the DSP capability, you must write and compile DSP code and include it with your application. A new addition to the Macintosh system software, the Real Time Manager, supplies the services your application needs to handle DSP code. It contains the calls needed to access the DSP, load and run DSP code, and transfer data to and from the DSP. The Real Time Manager also handles system memory management for the DSP and automatically locks and unlocks memory that is accessed by both DSP and Macintosh software. Chapter 4, "Real Time Manager," describes these functions in detail.

The Real Time Manager coordinates usage of the DSP chip through a new concept called guaranteed processing bandwidth (GPB). This type of control guarantees that any application that is granted access to the DSP will always process the needed data at the time required.

The DSP operating system, contained in the DSP chip, provides the services that DSP code needs to drive the chip and work with the Macintosh Operating System. The DSP operating system's application programming interface (API) defines how you can create a resource that can be loaded and run on the DSP chip. It automatically handles on-chip memory management to minimize recaching of code and data used by more than one DSP code module. For real-time applications, actual GPB requirements are determined and saved automatically in the DSP Preferences file. For timeshare applications, the program context is automatically saved when execution switches to real-time code.

The DSP operating system provides a run-time environment for the DSP code modules that minimizes programmer difficulties while providing robust support for a variety of tasks. Caching and saving of data and variables can be handled by the DSP operating system or can be explicitly controlled by the programmer. You can exercise complete control over running DSP code or, by setting a counter, can cause code execution to be determined dynamically at run time. For further information, see Chapter 5, "DSP Operating System."

Text-to-Speech Conversion

A new Macintosh manager, the Speech Manager, provides a standardized API for applications to generate synthesized speech. A single call provides simple text-to-speech operation. Other API calls provide more detailed speech

features. Word pronunciation can also be defined by means of embedded commands within the text string being spoken. Chapter 6, “Speech Manager,” provides full details of these new capabilities.

Speech Recognition

A new Macintosh system feature, the Speech Recognition Control Panel, provides start, stop, and parameter setup commands for controlling speech recognition behavior. In the Macintosh Quadra 840AV and Macintosh Centris 660AV, built-in speech recognition is provided for many Macintosh system operations. The standard File and Edit menu commands are fully supported, as are the Finder operations. For example, opening the Control Panels folder is as easy as saying *open control panels.*

User-defined speech macros let you customize the speech recognition software to recognize application-specific speech input for performing common tasks. A 60,000-word dictionary allows selection from a wide variety of words to define spoken phrases that trigger user-defined operations by means of speech macros.

Chapter 7, “Introduction to Speech Recognition,” describes the current user controls for speech command in the Macintosh Quadra 840AV and Macintosh Centris 660AV. Chapter 8, “Speech Rules,” provides information about further programmable controls for speech recognition.

New SCSI Manager

SCSI Manager 4.3 incorporates a new multilevel architecture that affects all modes of Small Computer System Interface (SCSI) operation. It uses a parameter-block-based programming interface for executing SCSI input-output (I/O) requests, which contains all the information required to complete each I/O operation. The new architecture provides a hardware-independent interface to the SCSI Manager. The SCSI driver layer passes the hardware support it provides to the SCSI Manager for complete hardware support. The SCSI Manager follows the phases driven by the target and eliminates the need to track the SCSI bus phases.

SCSI Manager 4.3 supports SCSI connect/disconnect, parity transmission and parity error detection, all SCSI-2 mandatory messages, SCSI Fast or Wide, and autosense. The SCSI DMA supports asynchronous protocols using both multiple bus and multiple logic units on each target.

Besides supporting these new features, SCSI Manager 4.3 also supports the existing SCSI device drivers with little or no modification. However, you should evaluate your existing drivers for compatibility and incorporate the new features where possible. See Chapter 9, “SCSI Manager 4.3,” for further details.

Other System Software Changes

The DMA serial driver was completely rewritten internally. However, there are no API changes. The major operational changes affect interrupt handling and DMA versus non-DMA transmissions, elimination of the `PollProc` mechanism, and use of the new DMA chip. For technical details, see Chapter 10, "DMA Serial Driver."

The video driver has been modified as a result of new video capabilities. Changes and additions to the video driver are described in Chapter 11, "Video Driver."

The floppy disk driver has been modified to work with the New Age floppy disk drive controller. This has resulted in minor changes to the floppy disk drive control API, as described in Chapter 12, "New Age Floppy Disk Driver."

The Virtual Memory Manager has been changed so that it no longer disables interrupts when performing certain tasks. These tasks are listed in Chapter 13, "Virtual Memory Manager."

Supplementary Documents

The following documents provide information that complements or extends the information in this developer note:

Apple Computer:

Inside Macintosh is a collection of books, organized by topic, that describe the system software of Macintosh computers. Together, these books provide the essential reference for programmers, software designers, and engineers. Current volumes include the following titles:
Inside Macintosh: Overview
Inside Macintosh: Toolbox Essentials
Inside Macintosh: More Macintosh Toolbox
Inside Macintosh: Files
Inside Macintosh: Processes
Inside Macintosh: Memory
Inside Macintosh: Operating System Utilities
Inside Macintosh: Imaging
Inside Macintosh: Text
Inside Macintosh: Interapplication Communication
Inside Macintosh: Devices
Inside Macintosh: QuickTime
Inside Macintosh: QuickTime Components
Inside Macintosh: Networking

Technical Introduction to the Macintosh Family, second edition, surveys the complete Macintosh family of computers from the developer's point of view.

Macintosh Human Interface Guidelines provides authoritative information on the theory behind the Macintosh "look and feel" and Apple's standard ways of using individual interface components.

Designing Cards and Drivers for the Macintosh Family, third edition, explains the hardware and software requirements for drivers and NuBus '90 accessory cards compatible with Macintosh computers, including the Macintosh Quadra 840AV and Macintosh Centris 660AV.

Technical Note 144 (*Macintosh Color Monitor Connections*) and Technical Note 326 (*M.HW.SenseLines*) provide technical details of the interfaces to various Apple and third-party monitors.

The *NuBus Block Transfers* technical note provides information about block data transfers to and from accessory cards.

Macintosh Classic II, Macintosh PowerBook Family, Macintosh Quadra Family, Macintosh Centris 610, Macintosh Centris 650, and Macintosh Quadra 800 Developer Notes include hardware details for these computers.

The Apple publications listed above are available from APDA, Apple's source for development tools and publications. APDA offers convenient worldwide access to over three hundred Apple and third-party development tools, resources, and information for anyone interested in developing applications on Apple platforms. For a free copy of the *APDA Tools Catalog*, call 1-800-282-2732 (United States), 1-800-637-0029 (Canada), or 716-871-6555 (International).

The following documents are available from the organizations listed:

AT&T:

WEDSP3210 Digital Signal Processor Information Manual

Comité Consultatif International Radio (CCIR):

Recommended Standard 601-2.

IT&T Semiconductors:

ASCO 2300 Audio-Stereo Codec Specification

Motorola:

MC68040 32-Bit Microprocessor User's Manual
MC68040 32-Bit Microprocessor Programmer's Reference Manual
MC68040 32-Bit Microprocessor Designer's Handbook

Phillips:

7169 Video Data Path Chip data sheet
7191B Digital Multistandard Decoder data sheet

Standard Abbreviations

Acronyms and abbreviations that are specific to Macintosh technology are spelled out in the text where they first occur and are listed in the glossary. Other contractions commonly used in the electronics industry are not spelled out. They include the following:

A	amperes	mm	millimeters
cm	centimeters	ms	milliseconds
dB	decibels	mV	millivolts
GB	gigabytes	NC	no connection
KB	kilobytes	ns	nanoseconds
Kbit	kilobits	pF	picofarads
kHz	kilohertz	rms	root mean square
kΩ	kilohms	V	volts
mA	milliamperes	µF	microfarads
MB	megabytes	µs	microseconds
Mbit	megabits	Ω	ohms
MHz	megahertz		

Hardware

This part of the *Macintosh Quadra 840AV and Macintosh Centris 660AV Developer Note* describes these computers from a hardware viewpoint. It contains two chapters:

- Chapter 1, "The Macintosh Quadra 840AV and Macintosh Centris 660AV Computers," gives you an overview of the configurations and features of these products.
- Chapter 2, "Hardware Details," describes the Macintosh Quadra 840AV and Macintosh Centris 660AV circuit boards, including their physical layout, functional units, signal timing and other electronic characteristics, input and output connectors, and interfaces with other equipment.

Other parts of this developer note cover the following topics:

- Part 2, "Real-Time Data Processing," covers the software technology of the Macintosh Quadra 840AV and Macintosh Centris 660AV DSP facilities.
- Part 3, "Speech Synthesis and Recognition," explains the capabilities of the Macintosh Quadra 840AV and Macintosh Centris 660AV system software for generating and understanding human speech.
- Part 4, "System Software Modifications," covers miscellaneous changes to the Macintosh Quadra 840AV and Macintosh Centris 660AV system software, including a new manager for the internal and external SCSI ports.

CHAPTER 1

The Macintosh Quadra 840AV and Macintosh Centris 660AV Computers

The Macintosh Quadra 840AV and Macintosh Centris 660AV represent new advances in the Macintosh family of high-performance desktop computers. Both models contain an input/output (I/O) subsystem that runs independently of the main processor and an independent digital signal processor (DSP) subsystem that supports real-time processing of data. These facilities, combined with a 32-bit MC68040 main processor running at either 40 MHz (the Macintosh Quadra 840AV) or 25 MHz (the Macintosh Centris 660AV), let these computers perform sophisticated manipulation of sound, graphics, video, and analog modem signals.

Both models bring advanced application performance into the mainstream of desktop computing. Potential application features include real-time speech recognition and synthesis, compression and decompression of sound, complex graphics and video processing, widely compatible telephone networking, and three-dimensional graphics rendering. With Apple's mini-videocam (sold separately), both models can also support videophone and desktop photography software. Many of these application features are unattainable on other personal computing platforms.

This chapter describes the computers in general terms and lists some of their features, differences, and compatibility issues.

Models and Accessories

The Macintosh Quadra 840AV and the Macintosh Centris 660AV have many common features. They differ mainly in physical form, speed, and expansion facilities:

- The Macintosh Quadra 840AV is housed in the same minitower configuration as the Macintosh Quadra 800. It runs at 40 MHz and has three NuBus™ slots for expansion cards. The base configuration for this model includes 8 MB of random-access memory (RAM) and a 230 MB internal hard disk.
- The Macintosh Centris 660AV is a less expensive desktop version of the Macintosh Quadra 840AV in the same low-profile enclosure as the Macintosh Centris 610. It runs at 25 MHz and has only one NuBus expansion slot. The base configuration for this model includes 4 MB of RAM and an 80 MB internal hard disk.

The user can expand the RAM capacity of either model by installing expansion cards. The Macintosh Quadra 840AV has an ultimate RAM capacity of 128 MB; the Macintosh Centris 660AV, 68 MB.

Both models include an Apple SuperDrive floppy disk drive, capable of accepting 1.4 MB floppy disks. The Macintosh Quadra 840AV accepts up to three removable SCSI devices inside its case; the Macintosh Centris 660AV can accept two. Besides the base configuration disk drives, internal data storage options include

- a 500 MB internal hard disk
- a 1000 MB internal hard disk (in the Macintosh Quadra 840AV only)
- an internal compact disc read-only memory (CD-ROM) drive

The user can add a variety of external disk drives to either model, using the external SCSI port. For details of the possible SCSI configurations, see "SCSI Connection," in Chapter 2. For information about new SCSI software, see Chapter 9, "SCSI Manager 4.3."

Apple offers the following separate accessories for both models:

- an inexpensive mini-videocam that captures monochrome video action in an image 360 pixels wide by 288 pixels high
- a high-quality microphone specifically designed for speech recording and recognition
- an analog telecom adapter
- an Ethernet cable adapter

Apple will sell the Macintosh Quadra 840AV and Macintosh Centris 660AV in all domestic and international markets for Apple computers.

Summary of Features

Besides standard features common to the Macintosh family of computers, the Macintosh Quadra 840AV and the Macintosh Centris 660AV have these new or improved capabilities:

- *Direct memory access.* A **Peripheral Subsystem Controller (PSC)** provides **direct memory access (DMA)** between the main processor buses and peripheral devices. DMA permits very fast transfers of large amounts of data without burdening the main processor.
- *Widely compatible video input.* Both models can process a YUV 4:2:2 video input from internal accessory cards. These computers can also process composite or S-video inputs in NTSC, PAL, and SECAM formats from external sources, using standard television-type connectors. Both models store video information in RGB form in a video frame buffer separate from main memory.
- *Flexible video output.* Both models supply video signals to the full range of Apple monitors as well as many third-party monitors. These computers also provide NTSC and PAL composite and S-video outputs for other kinds of video equipment. The Macintosh Quadra 840AV supports color depths up to 24 bits for graphics and 16 bits for video; the Macintosh Centris 660AV supports up to 16 bits for both.
- *Digital signal processing.* A built-in digital signal processor provides fast processing of data in real time. The principles of digital signal processing are discussed in Chapter 3, "Introduction to Real-Time Data Processing."
- *Improved NuBus interface.* Both models use the **Macintosh Universal NuBus Interface (MUNI)** for accessory cards. This interface supports block transfers and data bursts to and from the main processor bus. MUNI capability is optional in the Macintosh Centris 660AV.
- *New floppy disk support.* A new controller for the built-in Apple SuperDrive disk drive is based upon Industry Standard 765, supporting both Apple's **Group Code Recording (GCR)** format and DOS-compatible **Modified Frequency Modulation (MFM)** format.

- *Built-in Ethernet support.* Both models contain built-in circuitry for Ethernet I/O.
- *Enhanced serial ports.* Two serial ports both support RS-232, RS-422, and AppleTalk I/O and offer improved system performance with LocalTalk networks.
- *Integrated telephone I/O.* Both models provide Apple's high-performance serial I/O capability (called **GeoPort**) on one serial port, permitting connection to analog, ISDN, facsimile (fax), and data telephone lines. These computers support full-duplex telephone I/O at transmission rates up to 9600 bits per second.
- *Enhanced sound I/O.* Using the DSP, both models provide 16-bit digital stereo sound I/O at sample rates up to 48 kHz, including the standard rate of 44.1 kHz.
- *Large-capacity ROM.* Identical ROM chips totaling 2 MB are provided with both models. These chips contain some of the system software that is on the hard disk in other Apple computers.
- *Expansion slots.* The Macintosh Quadra 840AV contains three NuBus slots for long or short Macintosh expansion cards; the Macintosh Centris 660AV accepts one short card using an optional angle adapter. All slots carry a 32-bit data and address bus; in addition, a **digital audio/video (DAV) expansion connector** in line with one slot gives an accessory card direct access to YUV video data and digital sound.
- *Mass media support.* Both models support up to a total of seven SCSI devices. Within this limit, the user can connect up to six external devices to either model's SCSI port in addition to internal hard disk drives and CD-ROM drives.
- *Advanced processor features.* The MC68040 main processor in both models performs 32-bit paged memory management and has internal 4 KB data and instruction caches. The MC68040 processor also performs high-speed, high-accuracy coprocessing of floating-point numeric data.
- *Software on/off power control.* The Macintosh Quadra 840AV provides power control service to its expansion slots, so plug-in cards can turn the computer on and off.
- *Replaceable real-time clock battery.* The real-time clock and parameter RAM in both models are powered by a long-life plug-in battery.
- *Automatic SCSI termination.* Built-in circuitry provides automatic termination of the internal and external SCSI cables if no SCSI devices are connected.

Differences Between Models

Besides the distinctions of speed, physical form, and base memory configuration cited in "Models and Accessories," earlier in this chapter, the Macintosh Quadra 840AV and the Macintosh Centris 660AV contain the following detailed hardware differences:

- The maximum video window size at a color depth of 16 bits is 640 by 480 pixels for the Macintosh Quadra 840AV and 512 by 384 pixels for the Macintosh Centris 660AV.
- The Macintosh Quadra 840AV computer's VRAM is expandable from 1 MB to 2 MB; the Macintosh Centris 660AV computer's is not.

- The Macintosh Quadra 840AV supports 21-inch RGB monitors; the Macintosh Centris 660AV does not.
- The Macintosh Quadra 840AV can accept up to three long (4 by 13 inches) or short (4 by 7 inches) NuBus accessory cards; the Macintosh Centris 660AV accepts only one short card, using an optional angle adapter card.
- The Macintosh Quadra 840AV lets a plug-in card turn the computer on and off. The Macintosh Centris 660AV does not.
- The Macintosh Centris 660AV can accept an accessory card that connects directly to the main processor bus; the Macintosh Quadra 840AV cannot.
- The Macintosh Quadra 840AV requires 60 ns DRAM chips; the Macintosh Centris 660AV can use 70 ns DRAM chips.

System Software

The Macintosh Quadra 840AV and the Macintosh Centris 660AV contain the same ROM and support the same set of system calls, instructions, and data structures (the same **application programming interface**, or **API**). Hence, an application that runs on one model will run on the other. However, the system software API includes access to several new managers in addition to the familiar Macintosh Toolbox. Applications that are written to use these managers can offer valuable new features and capabilities.

For complete information about the system software features that are new with the Macintosh Quadra 840AV and the Macintosh Centris 660AV, see Chapters 3 through 13.

Compatibility Issues

Products that are designed for other computers in the Macintosh family and are compatible with Macintosh system software release 7.0 or 7.1 should work with the Macintosh Quadra 840AV and the Macintosh Centris 660AV, provided they follow Apple's current design guidelines (such as being 32-bit clean). Of course, such products normally will not take advantage of the unique capabilities of these new computers.

Developers who want to design new products that make use of the features of the Macintosh Quadra 840AV and the Macintosh Centris 660AV, while remaining compatible with other Apple computers, should keep these compatibility pointers in mind:

- Use only system API calls to access hardware; never try to modify or program the serial, SCSI, ADB, sound, or video subsystems directly.
- Never change the processor status register directly.
- Do not disable interrupts for longer than 0.5 ms.
- Do not assume any fixed addresses for global variables or ROM routines. You can use the `GetTrapAddress` and `SetTrapAddress` functions to get and set these addresses.

Machine Identification

By using the Gestalt Manager and the `SysEnvirons` function, an application can determine which features exist on the user's system. Table 1-1 lists the relevant machine identification values.

Table 1-1 Gestalt values for the Macintosh Quadra 840AV and Macintosh Centris 660AV

Identifier	Value	Description
`SysEnvirons`	78	Macintosh Quadra 840AV processor (40 MHz)
`SysEnvirons`	60	Macintosh Centris 660AV processor (25 MHz)
`gestaltNuBusSlotCount`	`'nubs'`	Count of logical NuBus slots
`gestaltSlotAttr`	`'slot'`	Slot attributes
`gestaltSlotMgrExists`	0	True if Slot Manager exists
`gestaltNuBusPresent`	1	NuBus slots are present
`gestaltSESlotPresent`	2	SE PDS slot present
`gestaltSE30SlotPresent`	3	SE/30 slot present
`gestaltPortableSlotPresent`	4	Portable's slot present
`gestaltFirstSlotNumber`	`'slt1'`	Returns first physical slot
`gestaltIconUtilities`	`'icon'`	Icon utilities attributes
`gestaltIconUtilitiesPresent`	0	Icon utilities present
`gestaltRealtimeMgrAttr`	`'rtmr'`	Real Time Manager attributes
`gestaltRealtimeMgrPresent`	0	True if Real Time Manager present
`gestaltSoundHardware`	`'snhw'`	Get the sound hardware
`gestaltASC`	`'asc '`	Component type of sound chip
`gestaltDSP`	`'dsp '`	Component type of DSP
`gestaltClassicSound`	`'clas'`	Macintosh Classic® sound
`gestaltVIA1Addr`	`'via1'`	VIA-1 base address
`gestaltVIA2Addr`	`'via2'`	VIA-2 base address
`gestaltVMAttr`	`'vm  '`	Virtual memory attributes
`gestaltVMPresent`	0	True if virtual memory present
`gestaltVMNotInstalled`	0	True if virtual memory not installed

CHAPTER 2

Hardware Details

The Macintosh Quadra 840AV and Macintosh Centris 660AV computers are shipped with built-in floppy disk drives and removable internal hard disk drives. For each model, the addition of an external monitor, a keyboard, and a mouse forms a complete personal computing system.

This chapter provides details of the Macintosh Quadra 840AV and Macintosh Centris 660AV physical equipment.

Physical Forms

The Macintosh Quadra 840AV and Macintosh Centris 660AV computers are generally described in "Models and Accessories," in Chapter 1. The external dimensions of their enclosures are shown in Table 2-1.

Table 2-1 External dimensions

Dimension	Macintosh Quadra 840AV	Macintosh Centris 660AV
Width	7.8 in. (19.7 cm)	16.3 in. (41.4 cm)
Depth	16.0 in. (40.6 cm)	14.8 in. (37.6 cm)
Height	14.3 in. (36.2 cm)	3.2 in. (8.1 cm)

Both models contain essentially the same circuit board and system components, with variations as noted in this chapter. Drawings of certain Macintosh Quadra 840AV and Macintosh Centris 660AV parts that support the mounting of peripheral devices are given in Appendix D, "Mechanical Details."

Parts Layout

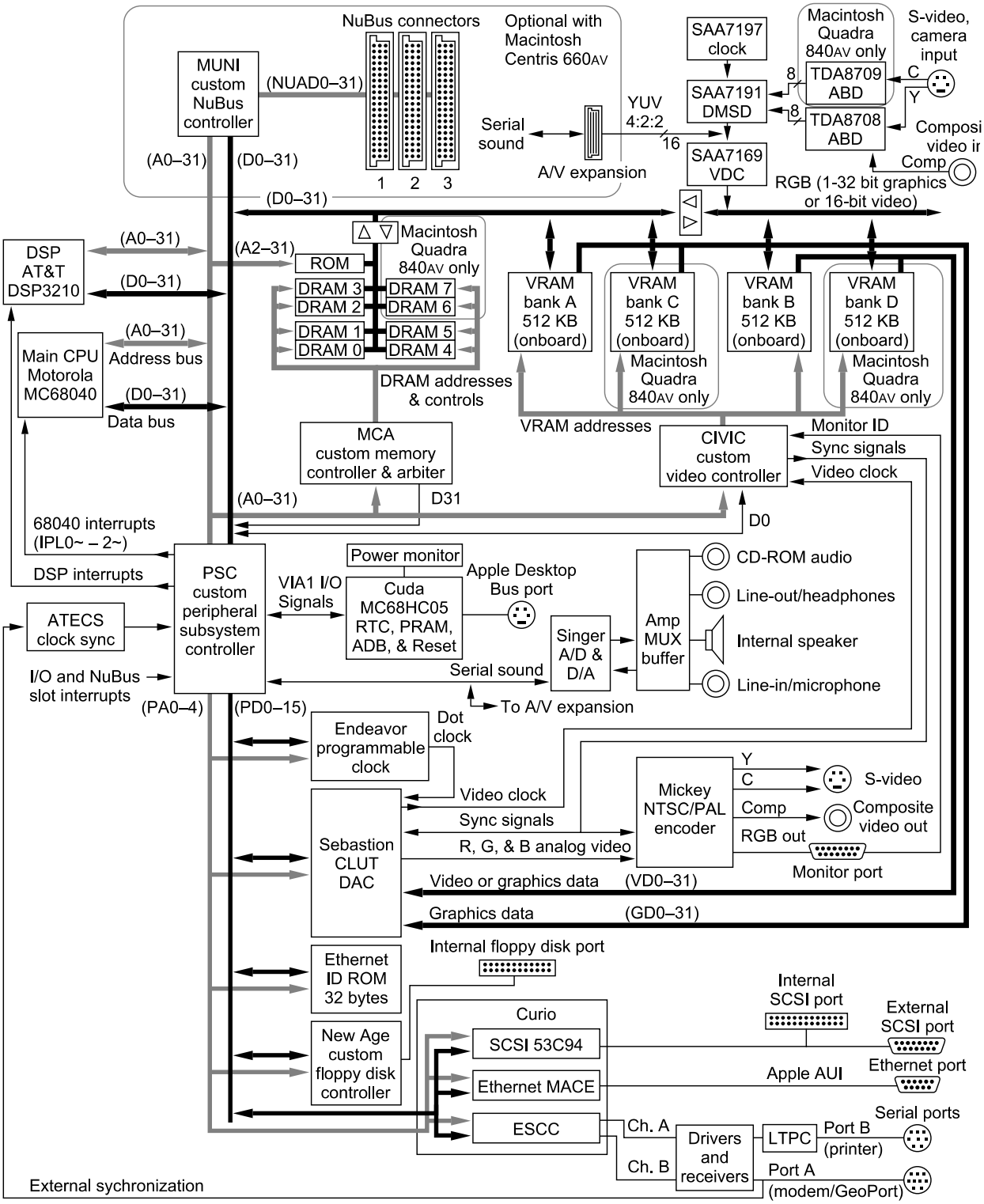
All the Macintosh Quadra 840AV and Macintosh Centris 660AV circuitry, except for the power supply, is contained on a single multilayer circuit board. The chips listed in "Functional Units," later in this chapter, can be identified by markings on the board.

System Architecture

The overall data flow relations among the hardware units of the Macintosh Quadra 840AV and Macintosh Centris 660AV computers are summarized by the block diagram in Figure 2-1. Parts omitted in the Macintosh Centris 660AV are enclosed in dotted lines.

The units shown in Figure 2-1 are described in more detail in the next section.

Figure 2-1 Functional diagram



Functional Units

Features of the major functional hardware units shown in Figure 2-1 are summarized in the next sections.

Main Processor

The main processor of the Macintosh Quadra 840AV and Macintosh Centris 660AV is a Motorola MC68040 microprocessor. This unit has

- an integer processing unit whose instruction set in user mode is compatible with the MC68030 processor
- a floating-point processing unit compatible with the MC68881 and MC68882 processors
- independent demand-paged memory management units for instructions and data
- independent 4 KB instruction and data caches
- multiple execution pipelines and full internal Harvard processing architecture

Neither model uses the optional bus-snooping feature of the MC68040 design.

Read-Only Memory

Both models contain 2 MB of ROM. For details of ROM access timing, see "ROM and RAM Management," later in this chapter.

Random-Access Memory

RAM consists of **dynamic random-access memory (DRAM)** on 72-pin **Single Inline Memory Modules (SIMMs).** Each SIMM contains one or two banks of DRAM with up to 16 MB of capacity per bank. In the Macintosh Centris 660AV, 4 MB of RAM capacity is soldered to the board and there are slots for two expansion SIMMs. In the Macintosh Quadra 840AV, all RAM is on SIMMs, with space for four expansion SIMMs. Thus maximum possible RAM capacity (using 16 MB RAM chips) is 128 MB for the Macintosh Quadra 840AV and 68 MB for the Macintosh Centris 660AV.

The DRAM in the Macintosh Quadra 840AV must have an access time of not more than 60 ns. The DRAM in the Macintosh Centris 660AV may have an access time up to 70 ns. DRAM compatible with either model must accept the column address strobe (CAS) before the row address strobe (RAS) for refresh and may not have more than eight chips per bank. Both models ignore the parity connection on DRAM SIMMs.

RAM addressing and RAM access timing are discussed in "ROM and RAM Management," later in this chapter. Certain changes to virtual memory management are described in Chapter 13, "Virtual Memory Manager."

Memory Controller and Arbiter

The **Memory Controller and Arbiter (MCA)** is a **complementary metal-oxide semiconductor (CMOS)** chip in a 160-pin package. It

- supports the bus interface between RAM and ROM memory and the main processor, DSP, MUNI, and PSC
- controls access to eight banks of DRAM with up to 16 MB capacity per bank
- controls access to ROM
- performs arbitration for control of the CPU bus between the main processor, PSC, MUNI, and DSP
- furnishes bus timeout signals for the main processor, I/O, MUNI, and DSP buses

For details of MCA operation, see "ROM and RAM Management," later in this chapter.

Digital Signal Processor

The Macintosh Quadra 840AV and Macintosh Centris 660AV computers include an AT&T DSP3210 32-bit floating-point **digital signal processor (DSP).** The DSP gives these computers the ability to perform fast, complex real-time data processing tasks, such as speech recognition, audio compression, analog modem signal processing, and so on. In the Macintosh Quadra 840AV, the DSP runs at 66.6667 MHz; in the Macintosh Centris 660AV, it runs at 55.5000 MHz. The DSP chip contains its own 8 KB of internal RAM, which minimizes its use of system memory. A summary of DSP operation and programming is given in Chapter 3, "Introduction to Real-Time Data Processing," with further details in Chapters 4 and 5.

Peripheral Subsystem Controller

The **Peripheral Subsystem Controller (PSC)** is a CMOS chip in a 208-pin package. The PSC

- provides nine dedicated DMA channels
- decodes the I/O memory mapping
- handles all internal system interrupts
- handles system interrupts from the Versatile Interface Adapter (VIA) inputs
- contains 16-byte buffers for sound data to and from the Singer sound encoder and decoder **(codec)**

For details of PSC operation, see "PSC Functions," later in this chapter.

Macintosh Universal NuBus Interface

The **Macintosh Universal NuBus Interface (MUNI)** is a CMOS chip in a 208-pin package. For a general discussion of NuBus, including its software details, see *Designing Cards and Drivers for the Macintosh Family,* third edition. The MUNI version of NuBus

- supports the full range of NuBus master/slave transactions with single or block moves, including dumps and runs in which the main processor is master and NuBus is slave
- supports faster data transfer rates to and from the CPU bus
- supports NuBus '90 data transfers between cards at a clock rate of 20 MHz
- provides first-in, first-out (FIFO) buffering of data between the CPU bus and accessory cards

In the Macintosh Quadra 840AV, the MUNI is mounted on the main circuit board; in the Macintosh Centris 660AV, it is on an optional NuBus adapter card. Details of the MUNI operation are given in "NuBus Interface," later in this chapter.

Cyclone Integrated Video Interfaces Controller

The **Cyclone Integrated Video Interfaces Controller (CIVIC),** used in both computers, is a CMOS chip in a 144-pin package. The CIVIC

- manages either 1 MB or 2 MB of video RAM (VRAM)
- controls data transfers between VRAM and the Video Data Path Chip and between VRAM and the Sebastian video color palette chip (described next)
- provides 32-bit or 64-bit data paths between VRAM and the main processor or a slot card; supports data bursts from the main processor in all transfer modes
- performs convolution of graphics data for line-interlaced displays
- provides NTSC and PAL timing signals (see Table 2-2)
- generates vertical blanking and video-in interrupt signals

For details of CIVIC operation, see "Video and Graphics I/O," later in this chapter.

Sebastian

The **Sebastian** is a video color palette and video digital-to-analog converter (DAC) in a 100-pin CMOS chip. The Sebastian

- accepts up to 64 bits of digital input, either as one 64-bit port or as one or two 32-bit ports
- lets one 32-bit port handle digital video while the other processes graphics (including QuickTime), using the same or different color lookup tables
- supports mixing video with still graphics, even with different color depths

- supports both Truecolor and pseudocolor with alpha color lookup
- supports a transparency effect when blending video with still graphics under the control of alpha bits
- uses a convolution filter to minimize flicker in line-interlaced displays
- supports displays with dot clocks up to 100 MHz

For details of Sebastian operation, see "Video and Graphics I/O," later in this chapter.

Video Data Path Chip

The **Video Data Path Chip (VDC)** is a Phillips CMOS chip in a 100-pin package. The VDC

- performs input video window scaling with horizontal and vertical filtering
- accepts YUV 4:2:2 color-encoded input from the Digital Multistandard Decoder or the digital audio/video (DAV) expansion slot card bus
- produces 16-bit 1:5:5:5 RGB, 8-bit grayscale, or YUV 4:2:2 output

For details of VDC operation, see "Video and Graphics I/O," later in this chapter, and the Phillips 7169 data sheet.

Mickey

The **Mickey** is a composite video encoder in a 28-pin advanced bipolar CMOS chip. The Mickey

- accepts analog video signals from the Sebastian video color palette chip
- encodes to NTSC or PAL digital format
- produces S-video, composite, and RGB video outputs

For details of Mickey operation, see "Video and Graphics I/O," later in this chapter.

New Age

The **New Age** is a floppy disk controller in a 64-pin CMOS chip. The New Age

- controls an Apple SuperDrive for all its recording densities
- uses a command set compatible with MFM and Apple GCR formats
- generates an interrupt on disk insertion
- performs 16-byte first-in, first-out data buffering
- supports full asynchronous operation for DMA

The New Age supports the standard Macintosh floppy disk software interface, as described in *Inside Macintosh.*

Curio

The **Curio** is a multipurpose I/O chip that contains a Media Access Controller for Ethernet (MACE), a SCSI controller, and a Serial Communications Controller (SCC). New serial driver code in the Macintosh Quadra 840AV and Macintosh Centris 660AV system software is discussed in Chapter 10, "DMA Serial Driver."

The SCC section of the Curio includes 8-byte FIFO buffers for both transmit and receive data streams.

Curio functions are discussed in "External Device Interfaces" and "PSC Functions," later in this chapter.

Apple Telecom External Clock Synchronizer

The **Apple Telecom External Clock Synchronizer (ATECS)** is a control chip that can synchronize the DSP and sound subsystems to an external clock signal received through the Apple GeoPort serial port connector. In the absence of an external clock, it generates crystal-controlled 49.152 MHz timing signals for 48 KHz operation or 45.1584 MHz timing signals for 44.1 KHz operation. For a description of Apple GeoPort, see "Serial Ports," later in this chapter.

Cuda

The **Cuda** is a microcontroller chip. It

- turns system power on and off
- manages system resets from various commands
- maintains parameter RAM
- manages the Apple Desktop Bus (ADB)
- manages the real-time clock
- lets an external signal through the Apple GeoPort serial port control system power

Cuda functions are discussed in more detail in "External Device Interfaces," later in this chapter. For a description of Apple GeoPort, see "Serial Ports," later in this chapter.

Singer

The **Singer** is an I/O chip that constitutes a 16-bit digital sound codec. It conforms to the IT&T *ASCO 2300 Audio-Stereo Codec Specification*. For details of its operation, see "Sound I/O," later in this chapter.

Endeavor

The **Endeavor** is a programmable video clock chip used in the Macintosh Quadra 840AV; the equivalent in the Macintosh Centris 660AV is called **Clifton Plus.** For details of the operation of these chips, see "Video and Graphics I/O," later in this chapter.

Digital Multistandard Decoder

The **Digital Multistandard Decoder (DMSD)** is a Phillips chip that decodes the color information in NTSC, PAL, and SECAM video formats using a clock synchronized to their line frequency. For details of DMSD operation, see "Video and Graphics I/O," later in this chapter, and the Phillips 7191B data sheet.

System Clocks

Operation of the Macintosh Quadra 840AV and Macintosh Centris 660AV is driven by several different clocks running at different frequencies. These clocks are listed in Table 2-2, where their frequencies are given in MHz.

Table 2-2 Clock frequencies

Location	Signal name	Frequency (MHz)	Source	Usage
CPU bus	PClk	80.0000/50.0000*	Divider	Main processor, MCA, CIVIC†
	BClk	40.0000/25.0000*	Divider	Main processor, MCA, CIVIC, PSC, MUNI
	PClk/4	20.0000/12.5000*	Oscillator	Divider
I/O bus	C22_5792M	22.5792	PSC	Singer (44.1 KHz)
	C24_576M	24.5760	PSC	Singer (48 KHz)
	C16M	15.6672	PSC	New Age, Curio
	C32M	31.3344	Oscillator	PSC
	C25M	25.0000	Oscillator	SCSI
	C15_0528M	15.0528	Crystal	ATECS (44.1 KHz)
	C16_384M	16.3840	Crystal	ATECS (48 KHz)
	C45_1584M	45.1584	ATECS	PSC (44.1 KHz)
	C49_1520M	49.1520	ATECS	PSC (48 KHz)
	C20M	20.0000	Crystal	MACE Ethernet
	CudaClk	0.032768	Crystal	Cuda

continued

Table 2-2 Clock frequencies (continued)

Location	Signal name	Frequency (MHz)	Source	Usage
DSP	CKI	66.6667/55.5000*	Oscillator	DSP, MCA
NuBus	C40M	40.0000	Oscillator	MUNI
	C20M	20.0000	MUNI	Accessory card slots
	CN10M	10.0000	MUNI	Accessory card slots
Video	Video in	26.8000	Crystal	DMSD
Video	Dot clock	Various‡	Endeavor	Sebastian
	NTSC	14.31818	Oscillator	Sebastian, Mickey
	PAL	17.734475	Oscillator	Sebastian, Mickey

* The two values are the frequencies in the Macintosh Quadra 840AV and Macintosh Centris 660AV, respectively.
† In the Centris 660AV only.
‡ Up to 100 MHz maximum, depending on the monitor; see Table 2-14.

Signal Buses

The Macintosh Quadra 840AV and Macintosh Centris 660AV contain several internal signal buses. The principal ones are shown in Figure 2-1. They are

- the CPU bus, containing 32 address lines and 32 data lines
- NuBus, containing 32 combined data and address lines
- the digital audio/video (DAV) expansion connector bus, containing 16 video data lines and five audio data lines
- the video bus, containing two sets of 32 lines each (or a combined set of 64 lines) for video or graphics
- the I/O bus, containing five address lines and 16 data lines

For detailed information about NuBus, see *Designing Cards and Drivers for the Macintosh Family*, third edition. In the Macintosh Centris 660AV, NuBus exists only if an adapter card has been installed in the PDS connector. The PDS connector is described in "Processor-Direct Cards for the Macintosh Centris 660AV," later in this chapter.

Bus Arbitration

Four chips are able to take control of the CPU bus: the main processor, the MUNI, the PSC, and the DSP (which is asynchronous with respect to the main processor). The MCA performs arbitration between these chips for control of the CPU bus.

Priority among accessory cards for control of NuBus depends on which slots they occupy. Lower-numbered slots have higher priority.

Control of the I/O bus is managed by the PSC chip, as described in "Bus Arbitration Performed by the PSC," later in this chapter.

Bus Timeouts

The MCA chip performs two timeout functions for the CPU bus:

- If the CPU, PSC, or MUNI does not respond to a cycle start signal within a critical time, the MCA terminates that chip's bus control and issues a bus error signal. The critical time is 32 µs for NuBus address space ($6000 0000 to $FFFF FFFF) and 16 µs for the rest of the address space ($0000 0000 to $5FFF FFFF).
- If the DSP does not issue a cycle start signal within 16 DSP clock cycles after it is granted bus control, the MCA terminates the DSP's control and issues a bus error signal.

The MUNI chip generates a bus error if any Nubus transaction takes longer than 25.6 µs.

ROM and RAM Management

During the system startup process, the system software programs the MCA for the configuration of ROM and RAM actually present in the user's hardware.

The CPU bus can read from and write to RAM, as well as read from ROM, in either single-address accesses or four-address bursts.

DRAM Configurations

Possible DRAM configurations are shown in Table 2-1.

Table 2-1 DRAM configurations

Bank size (MB)	Organization	Row address bits	Column address bits
1	256 Kbit x 4	9	9
1	1 Mbit x 4	10	10
2	512 Kbit x 8	10	9
4	4 Mbit x 4	11	11
8	2 Mbit x 8	11	10
4	4 Mbit x 4	12	10
8	2 Mbit x 8	12	9
16	1 Mb x 16	11	9

Startup Memory Addressing

At the beginning of the system startup process, the MCA maps the ROM code to the lower end of the RAM address space, starting at address $0000 0000. When the main processor is reset, it sets the program counter to the 32-bit address found at $0000 0004, which transfers execution to the actual system software entry point in the space $4000 0000 to $4FFF FFFF. After this first access, ROM is no longer mapped to the bottom of the RAM space.

Access Timing

The Macintosh Quadra 840AV and Macintosh Centris 660AV use 60-ns DRAM chips. Access to RAM in both models may occur under either of two conditions:

- Multiple access occurs when the CPU bus requests a new access immediately after the end of the previous access.
- Single access occurs when there is an interval of at least one main processor clock cycle after the previous access.

The number of clock cycles required for various chips to access RAM under these two conditions in various read and write modes is shown in Table 2-3. The clock rate for determining cycle times is BClk for the main processor, the MUNI, and the PSC; it is CKI for the DSP. These clock rates are listed in Table 2-2.

Table 2-3 DRAM access times

		Main processor		MUNI and PSC		
Access type	**Condition**	Macintosh Quadra 840AV	Macintosh Centris 660AV	Macintosh Quadra 840AV	Macintosh Centris 660AV	**DSP**
Single read	Single	6	4	5	4	9
	Multiple	7	5	6	5	11
Single write	Single	6	3	4	3	8
	Multiple	7	5	6	5	11
Burst read	Single	6-3-3-3	4-2-2-2	5-3-3-3	4-2-2-2	9-4-4-4
	Multiple	7-3-3-3	4-2-2-2	6-3-3-3	4-2-2-2	11-4-4-4
Burst write	Single	6-2-2-2	3-2-2-2	4-3-3-3	3-2-2-2	8-7-7-7
	Multiple	7-2-2-2	4-2-2-2	6-3-3-3	4-2-2-2	11-7-7-7

The DRAM refresh cycle takes eight main processor clock cycles, but does not affect RAM access timing. DRAM refresh does not occur when the DSP controls the CPU bus.

Both computers use 120-ns ROM chips. CPU bus accesses to ROM take five bus clock cycles in the Macintosh Centris 660AV and seven bus clock cycles in the Macintosh Quadra 840AV.

For additional information about burst write actions on the processor bus, see "Processor Bus Burst Write Timing," later in this chapter.

External Device Interfaces

This section discusses the interfaces between the Macintosh Quadra 840AV and Macintosh Centris 660AV computers and external devices through

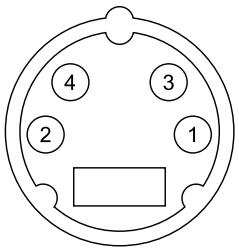
- the ADB, which supports keyboards, mouse devices, trackballs, and so on
- an Ethernet port for wide area network access
- two serial ports for printers, modems, AppleTalk, and other serial I/O
- a SCSI connection for devices such as hard disk drives
- an interface to the Apple SuperDrive floppy disk drive

For video interface information, see "Video and Graphics I/O," later in this chapter. For sound interface information, see "Sound I/O," later in this chapter.

Apple Desktop Bus

The **Apple Desktop Bus (ADB)** is an asynchronous serial communication bus used to connect relatively slow user-input devices to Macintosh computers. Its software characteristics are described in *Inside Macintosh.* One ADB connector is located on the back panel. It is a mini-DIN 4-pin socket, as shown in Figure 2-2.

Figure 2-2 ADB socket



The ADB pin assignments are shown in Table 2-4.

Table 2-4 ADB pin assignments

Pin	Description
1	Data; grounded by an open collector or pulled to +5 V through 470 Ω
2	Power on, fed by +5 V through 100 kΩ; connect to pin 4 to turn on the system
3	+5 V at 500 mA maximum drain; protected by a 1.25-A circuit breaker
4	Ground return

Ethernet Port

Both the Macintosh Quadra 840AV and Macintosh Centris 660AV contain built-in support for Ethernet. The user can plug a drop-box cable available from Apple or from third-party vendors into a standard Ethernet connector on the back panel.

The Ethernet port pin assignments are shown in Table 2-5.

Table 2-5 Ethernet port pin assignments

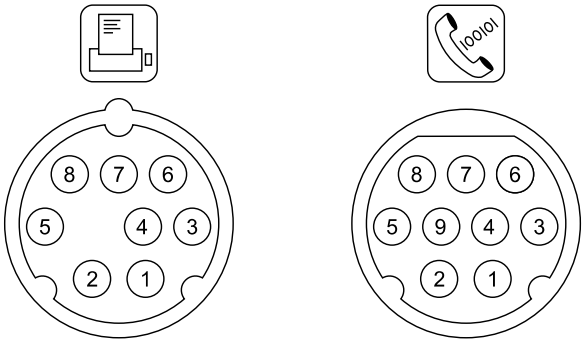
Pin	Description	Pin	Description
1	+5 V	8	+5 V
2	DI+	9	DO+
3	DI–	10	DO–
4	Ground	11	Ground
5	CI+	12	NC
6	CI–	13	NC
7	+5 V	14	+5 V

Serial Ports

The back panel on both the Macintosh Quadra 840AV and Macintosh Centris 660AV contains two serial data I/O ports. An 8-pin mini-DIN socket is marked as a printer port, and a 9-pin mini-DIN socket is marked as a modem port. Both sockets accept 8-pin plugs, but only the modem port accepts 9-pin plugs.

The physical patterns for the serial port sockets are shown in Figure 2-3.

Figure 2-3 Serial port connectors



Printer Modem

Either port can be independently programmed for asynchronous or synchronous communication formats up to 9600 baud, including AppleTalk. The printer port supports LocalTalk hardware protocols by means of a **LocalTalk Patch Chip (LTPC).** In addition, the port marked "Modem" supports the full range of Apple GeoPort protocols, helping the computer communicate with a variety of ISDN and other telephone transmission means by using external pods.

For information about serial driver software in the Macintosh Quadra 840AV and Macintosh Centris 660AV, see Chapter 10, "DMA Serial Driver."

Table 2-6 gives the pin assignments for the two serial ports. The Both ports column shows how both connectors support AppleTalk and common serial communications; the GeoPort columns show how the 9-pin connector can also support Apple GeoPort protocols.

Table 2-6 Serial port pin assignments

Pin	Both ports	GeoPort	Special GeoPort functions
1	HSK_o	$SCLK_{out}$	Reset pod or get pod attention
2	HSK_i	$Sync_{in}/SCLK_{in}$	Serial clock from pod (up to 920 Kbits/sec)
3	TxD–	TxD–	
4	Gnd/shield	Gnd/shield	
5	RxD–	RxD–	
6	TxD+	TxD+	
7	GP_i	Wakeup/TxHS	Wake up CPU or do DMA handshake
8	RxD+	RxD+	
9		+5 V	Power to pod

SCSI Connection

The SCSI interface in the Macintosh Quadra 840AV and Macintosh Centris 660AV exists in two forms: an internal 50-pin ribbon connector for internal devices and an external DB-25 connector for external devices. Internal device mounting is shown in Appendix D, “Mechanical Details.”

The Macintosh Centris 660AV can support one 3.5-inch internal hard disk and an optional 5.25-inch CD-ROM drive. The Macintosh Quadra 840AV can support an additional internal disk drive. Both models accept up to a total of seven SCSI devices, internally and externally.

The SCSI interface in the Macintosh Quadra 840AV and Macintosh Centris 660AV is electrically and mechanically compatible with SCSI interfaces on other computers of the Macintosh family. For information about SCSI Manager software in the Macintosh Quadra 840AV and Macintosh Centris 660AV, see Chapter 9, “SCSI Manager 4.3.”

Power Budgets

The maximum continuous power budgets available for each SCSI device attached to a Macintosh Quadra 840AV or Macintosh Centris 660AV computer are shown in Table 2-7.

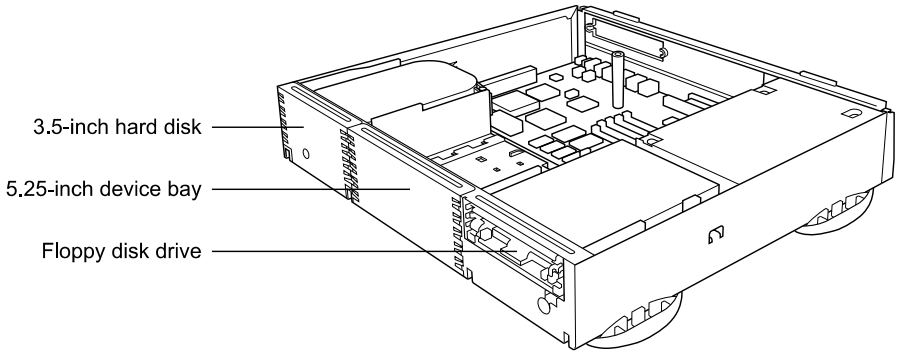
Table 2-7 SCSI power budgets

Computer	+5 V	+12 V
Macintosh Quadra 840AV	1.5 A	4.3 A
Macintosh Centris 660AV	1.5 A	1.5 A

Internal SCSI Locations

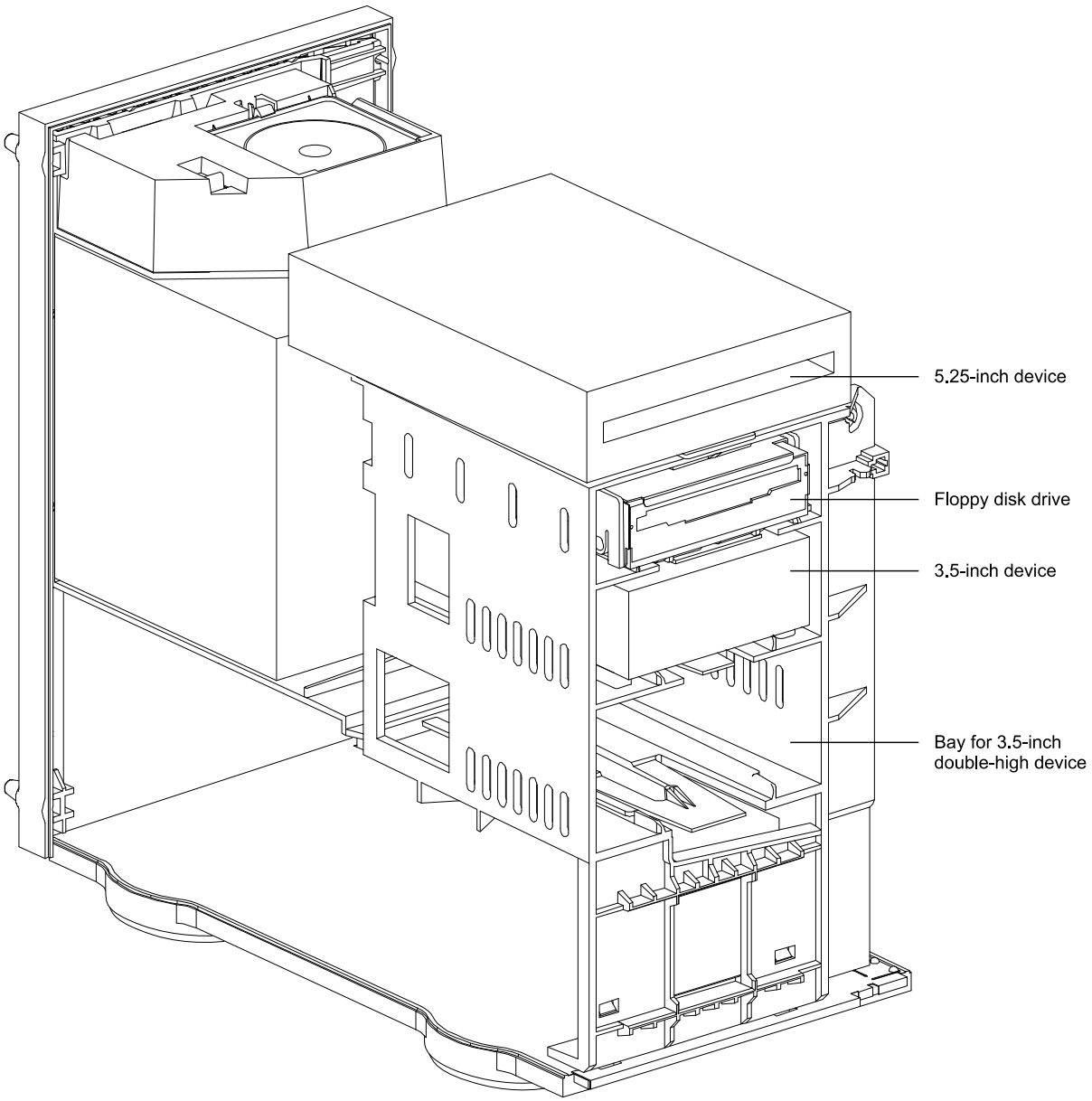
The locations of the Macintosh Centris 660AV computer’s internal SCSI devices are shown in Figure 2-4.

Figure 2-4 Macintosh Centris 660AV internal SCSI device space



The locations of the Macintosh Quadra 840AV computer's internal SCSI devices are shown in Figure 2-5.

Figure 2-5 Macintosh Quadra 840AV internal SCSI device space



Pin Assignments

The standard internal and external SCSI pin assignments are shown in Table 2-8.

Table 2-8 SCSI pin assignments

Pin number			Pin number		
Internal	External	**Description**	Internal	External	**Description**
1	7	Ground	2	8	/DATA0*
3	9	Ground	4	21	/DATA1
5	14	Ground	6	22	/DATA2
7	16	Ground	8	10	/DATA3
9	18	Ground	10	23	/DATA4
11	24	Ground	12	11	/DATA5
13		Ground	14	12	/DATA6
15		Ground	16	13	/DATA7
17		Ground	18	20	/DATAP
19		Ground	20		Ground
21		Ground	22		Ground
23		NC	24		NC
25		NC	26	25	TERMPWR
27		NC	28		NC
29		Ground	30		Ground
31		Ground	32	17	/ATN
33		Ground	34		Ground
35		Ground	36	6	/BUSY
37		Ground	38	5	/ACK
39		Ground	40	4	/RST
41		Ground	42	2	/MSG
43		Ground	44	19	/SEL
45		Ground	46	15	/C/D
47		Ground	48	1	/REQ
49		Ground	50	3	/I/O

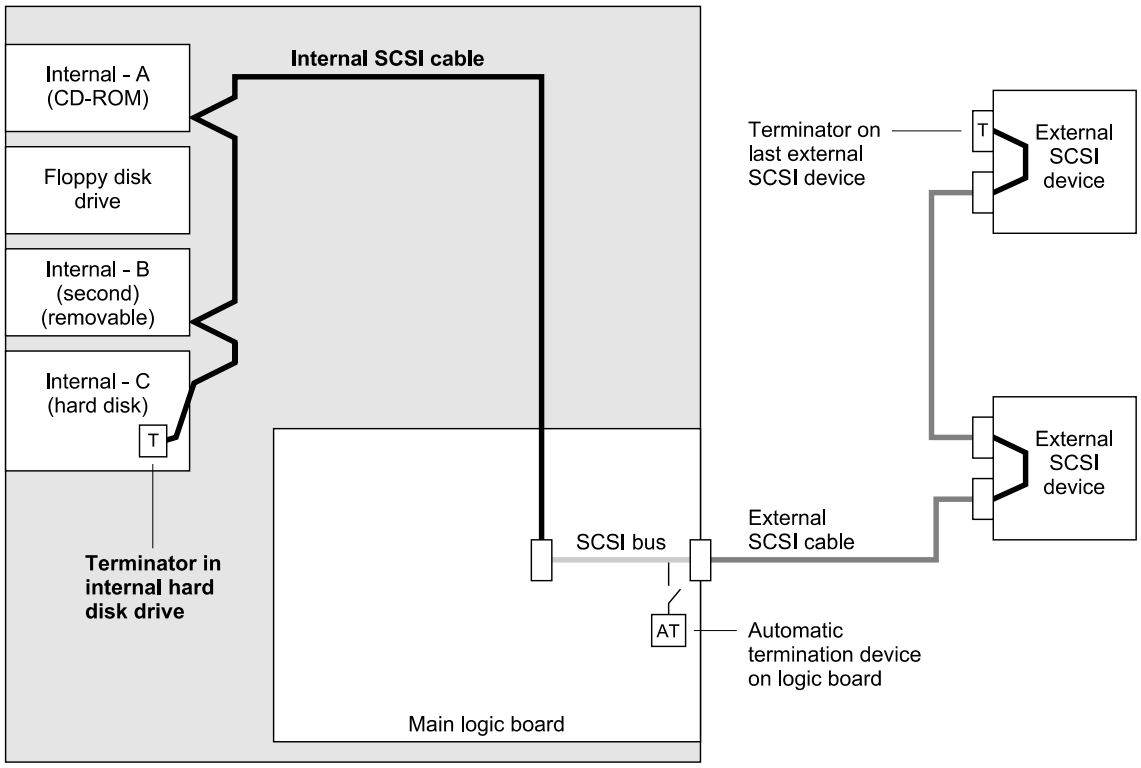
* A slash before a signal name indicates that it is in the low state when active.

Automatic SCSI Termination

Because the internal portion of the SCSI bus must be long enough to connect multiple devices, the bus requires termination at both ends. As on other Macintosh models, the external end of the bus is normally terminated at the last external device. On the Macintosh Quadra 840AV and Macintosh Centris 660AV, the internal end of the bus—the end at the last internal hard disk drive—is terminated in the drive itself.

Figure 2-6 shows the arrangement of the SCSI cables in a typical Macintosh Quadra 840AV configuration. The bus is continuous across the internal SCSI cable, the SCSI bus traces on the logic board, and the external SCSI cable (if any). The boxes with the letter T represent terminators. The Macintosh Centris 660AV has a similar arrangement, but contains a maximum of two internal SCSI devices.

Figure 2-6 SCSI bus terminators in a typical Macintosh Quadra 840AV configuration



Both computers include a new feature that automatically provides the proper termination when no external device is connected, that is, when the SCSI bus ends at the external connector. When no external device is connected, special circuitry terminates the bus on the logic board near the external connector. When one or more external SCSI devices are connected, the circuitry detects the external termination during system reset and disconnects the termination on the logic board. In Figure 2-6, the box marked AT on the logic board indicates the automatic termination device.

Signals on the SCSI bus are usually connected to open-collector devices that can pull the line low but that depend on external power to pull it high. The bus includes a line called TERMPWR that provides pull-up power. The standard Macintosh terminator block used at the last external SCSI device terminates each line with a 220 Ω pull-up resistor and a 330 Ω resistor to ground.

Installing Internal SCSI Devices

In the Macintosh Quadra 840AV and Macintosh Centris 660AV, the device at the end of the internal SCSI cable includes terminators; all other internal devices do not. When installing internal SCSI devices, the installer must make sure that the device at the end of the cable has terminators and must remove terminators from any other internal SCSI devices.

SCSI termination can be present on only the last internal device—the one at the end of the internal SCSI cable. If none of the internal devices is terminated, the computer will malfunction; if more than one internal device includes terminators, the computer will malfunction and the logic board may be damaged.

Physical provisions for internal SCSI device mounting are given in Appendix D, “Mechanical Details.”

As in all SCSI installations, all devices on the SCSI bus must have different ID numbers.

Floppy Disk Drive Connection

Both models contain one internal Apple SuperDrive floppy disk drive. Table 2-9 gives the pin assignments for the 20-pin floppy disk drive connector.

Table 2-9 Floppy disk drive connector pin assignments

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	11	+5V	+5 V
2	PH0	Phase 0 state control	12	SEL	Head select
3	GND	Ground	13	+12V	+12 V
4	PH1	Phase 1 state control	14	/ENBL*	Drive enable
5	GND	Ground	15	+12V	+12 V
6	PH2	Phase 2 state control	16	RD	Read data
7	GND	Ground	17	+12V	+12 V
8	PH3	Phase 3 register write strobe	18	WR	Write data
9	NC	NC	19	+12V	+12 V
10	/WRREQ	Write data request	20	NC	NC

* A slash before a signal name indicates that it is in the low state when active.

PSC Functions

The PSC contains nine programmable DMA channels that transfer data between random-access memory and various I/O interfaces. The PSC also performs address decoding for many I/O memory allocations.

DMA Channels Controlled by the PSC

The PSC provides nine DMA channels that can access RAM or ROM but cannot access the I/O or NuBus address spaces. The characteristics and uses of these DMA channels are shown in Table 2-10. The "Width" column lists the number of bits of data that the PSC transfers over the I/O bus during each transaction. The "Buffer" column lists the capacity of the PSC's internal FIFO buffer for each DMA channel.

Table 2-10 PSC DMA channels

Name	Width (bits)	Buffer (bytes)	I/O function served
SCSI	16	16	SCSI port
ENetRd	16	16	Ethernet read
ENetWr	16	16	Ethernet write
FDC	8	4	Floppy disk controller
SCCA	8	4	SCC Channel A (SCC Rx or Tx, GeoPort)
SCCB	8	4	SCC Channel B (SCC Rx or Tx)
SCCATx	8	4	SCC Channel A (Scc Tx, GeoPort)
SndIn	1	16	Singer sound input
SndOut	1	16	Singer sound output

Each DMA channel is controlled by two sets of programming registers. Using two register sets helps software optimize data transfers to and from physical memory and increases the limit of system interrupt latency when the data input is continuous (such as from Ethernet). In a virtual memory environment, software must guarantee that memory pages are contiguous when DMA transfers controlled by the PSC cross a page boundary.

Bus Arbitration Performed by the PSC

The PSC controls access to the I/O bus by the main processor and by the DMA channels described in the previous section. At the first level of arbitration, the PSC grants its DMA channels two accesses for every one access granted to the main processor. When DMA

channels contend with one another, the PSC grants them access to the I/O bus in the order of priority shown in Table 2-11. This table also shows the order of priority in which the PSC controls access by its DMA channels to the CPU bus.

Table 2-11 Priority of DMA channel access

Priority	To the I/O bus	To the CPU bus
Highest	FDC	SndOut
	SCCA	SndIn
	SCCA Tx	FDC
	SCCB	SCCA
	ENetRd	SCCA Tx
	ENetWr	SCCB
	SCSI	ENetRd
		ENetWr
Lowest		SCSI

Video and Graphics I/O

The Macintosh Quadra 840AV and Macintosh Centris 660AV contain a sophisticated video and graphics I/O system that handles video input and output signals and supports a wide variety of Apple and third-party monitors.

The video I/O system also lets the user connect a television set as a monitor, using either NTSC or PAL format. For further information, see "Video Television Output," in Chapter 11.

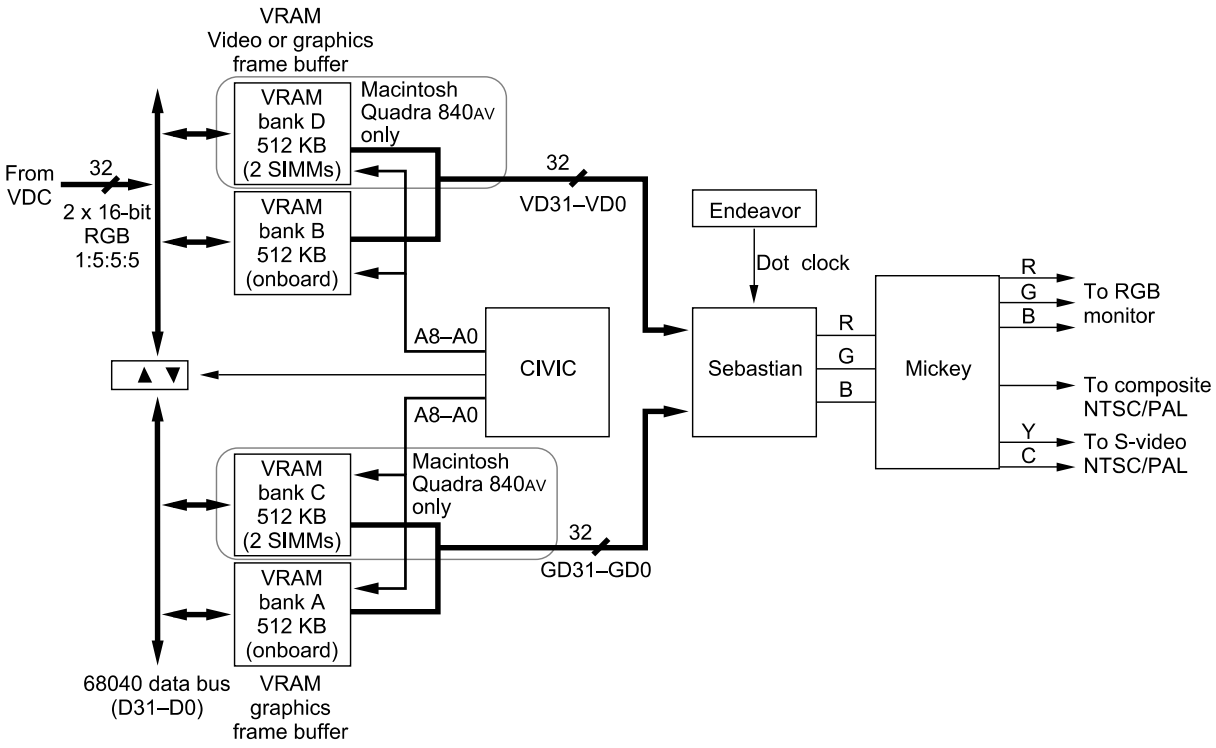
Some monitors go into power-saving mode when the sync signals are disabled. New routines in the video driver support this feature, as described in "New Control and Status Routines," in Chapter 11.

The output part of the video system is shown in Figure 2-7.

As shown in Figure 2-7, the video and graphics I/O system is built around two banks of VRAM. Each bank holds 512 KB and is expandable in the Macintosh Quadra 840AV to 1 MB. Thus, total VRAM capacity in the Macintosh Quadra 840AV may be either 1 MB or 2 MB; in the Macintosh Centris 660AV it is limited to 1 MB. The VRAM is controlled by the CIVIC chip. By programming the CIVIC, an application can configure it in either of the following two ways:

- as a single frame buffer that uses all the VRAM capacity
- as two frame buffers, one for video and one for graphics

Figure 2-7 Video and graphics output system block diagram



If the VRAM is configured as a single video frame buffer, it can all be used for graphics and the video input can be disabled. In this case, the CIVIC controls data access to VRAM from the following sources:

- the main processor
- the PSC, using I/O direct memory access
- the MUNI chip

If the VRAM is configured as two frame buffers, it can store video as well as graphics. In Figure 2-7, the VRAM banks shown at the top of the figure can store video frames and the lower banks can store only graphics. In this configuration, the CIVIC can provide access to all VRAM from the sources just listed and it can also store video data from the VDC in the video VRAM. The video input subsystem that provides data to the VDC is described in the next section.

Video images and graphics images stored in VRAM may have different color depths. The two images exit VRAM through its serial access memory port and pass to the Sebastian color palette chip. Sebastian provides independent color lookup tables for video and graphics images and mixes them into a single digital RGB data stream. The Sebastian then converts the result into analog RGB video, using internal DAC circuits.

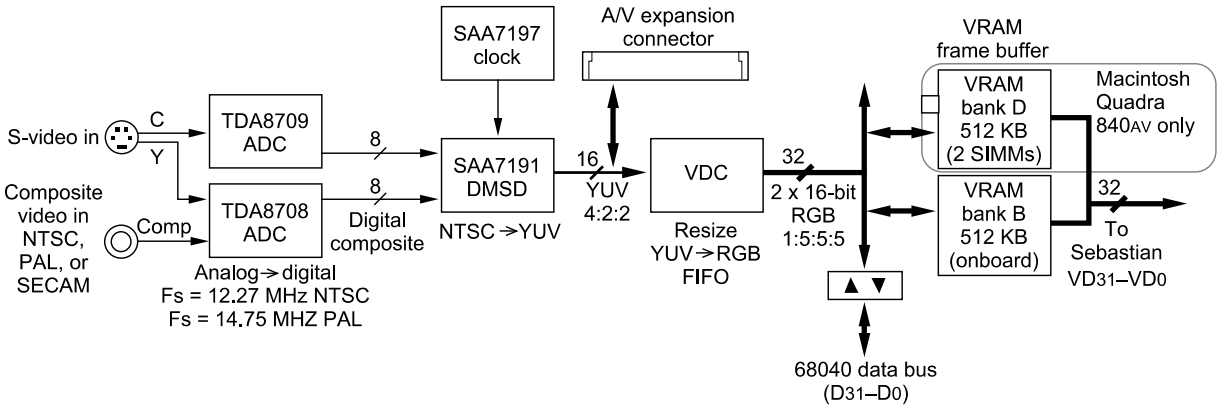
Analog RGB data passes to the Mickey encoder chip. Mickey either sends RGB directly to the monitor connector or encodes it into NTSC or PAL video signals in composite or

S-video format and sends it to other connectors located on the back panel. Monitors available for the Macintosh Quadra 840AV and Macintosh Centris 660AV are discussed in "Video Monitor Interface," later in this chapter.

External Video Input

Figure 2-8 shows details of the processing of video input from an external source such as a videocam or videocassette deck.

Figure 2-8 Video input subsystem



The input signal, which may be analog composite or S-video in NTSC, PAL, or SECAM format, enters through an external 7-pin mini-DIN socket. A cable adapter is provided to receive composite video from external devices that have RCA connectors. TDA8708 and TDA8709 video ADC chips digitize the composite video waveform, and the DMSD chip decodes the result into YUV format. This common digital video format, also known as YCrCb, is described in CCIR Recommended Standard 601-2.

Digital video in YUV format then passes to the digital audio/video (DAV) expansion connector, where it may be picked up by a NuBus expansion card, and to the VDC. A slot card that uses the DAV connector may disable the DMSD and feed its own YUV video to the VDC—for example, a slot card containing a video decompression engine. The DAV connector is described in "Digital Audio/Video Expansion Connector," later in this chapter.

The VDC scales down the video image and converts its format to either 8-bit grayscale, 15-bit RGB, or 16-bit YUV. It stores the result in the VRAM buffer under the control of the CIVIC chip. The video input connector is shown in Figure 2-9.

The pin assignments for the video input connector are shown in Table 2-12.

Figure 2-9 Video input connector

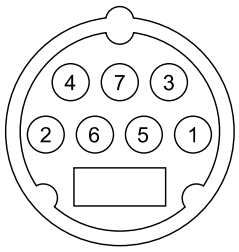


Table 2-12 Video input connector pin assignments

Pin	Description
1	AGND (signal)
2	AGND (power)
3	Video Y
4	Video C
5	I^2C clock (Phillips serial bus)
6	+12 V at 20 mA maximum drain
7	I^2C data (Phillips serial bus)

The data rate for full-screen NTSC video (640 by 480 pixels at 30 frames per second) is 18.43 MB per second. The data rate for full-screen PAL video (768 by 576 pixels at 25 frames per second) is 22.12 MB per second. This means that it is practical to record a video image up to one-quarter screen in size on an output device such as a hard disk drive in real time, without data compression.

Video RAM Usage

Each computer is delivered with two banks of VRAM soldered in, each bank providing 0.5 MB of storage. One of the two banks can supply a graphics screen image for monitors of small size or low color depths, letting the other bank supply live video to be mixed with the graphic image. Two banks together can support graphics alone on monitors that are larger or use more bits per pixel. The maximum video window size on the Macintosh Quadra 840AV is 640 by 480 pixels; the maximum video window size on the Macintosh Centris 660AV is 512 by 384 pixels.

The Macintosh Quadra 840AV also contains provision for VRAM expansion. When the user installs two more banks of VRAM in the SIMM expansion sockets, the resulting VRAM capacity can support mixed video and graphics in full 24-bit color on small and medium-sized monitors and in 16-bit or 8-bit color on larger monitors.

The color depths available when the Macintosh Quadra 840AV drives Apple monitors with and without VRAM expansion are listed in Table 2-13. Expanded VRAM is available only in the Macintosh Quadra 840AV; color depths and monitor configurations that are also supported by the Macintosh Centris 660AV (using standard VRAM) are printed in **boldface.**

Table 2-13 VRAM sizes and monitor color depths

	Screen size	Standard VRAM (1 MB)		Expanded VRAM (2 MB)	
Monitor type	Hor. x vert.	Graphics	Graphics/video	Graphics	Graphics/video
12-inch RGB*	512 x 384	**32**	**8 / 16**	32	8 / 16
	560 x 384	**32**	**8 / 16**	32	8 / 16
13-inch RGB or 12-inch mono*	512 x 384	**32**	**8 / 16**	32	8 / 16
	640 x 400	**32**	**8 / 16**	32	8 / 16
	640 x 480	**16**	**8 / 16**	32	8 / 16
Full-page mono*	640 x 870	**8**	**4 / 16**	8	8 / 16
Full-page RGB	640 x 870	**8**	**4 / 8**	16	8 / 16*
16-inch RGB*	832 x 624	**16**	**8 / 16**	32	8 / 16
19-inch RGB	1024 x 768	**8**	**4 / 8**	16	8 / 8
Two-page mono	1152 x 870	8	4 / 8	8	8 / 8
Two-page RGB	1152 x 870	8	4 / 8	16	8 / 8
VGA*	640 x 480	**16**	**8 / 16**	32	8 / 16
Super VGA 56 Hz*	800 x 600	**16**	**8 / 16**	32	8 / 16
Super VGA 72 Hz*	800 x 600	**16**	**8 / 16**	32	8 / 16
Super VGA 60 Hz	1024 x 768	**8**	**4 / 8**	16	8 / 8
Super VGA 70 Hz	1024 x 768	**8**	**4 / 8**	16	8 / 8
NTSC	640 x 480	**16**	**8 / 16***	32	8 / 16
	512 x 384	**32**	**8 / 16***	32	8 / 16
Convolved NTSC	640 x 480	**8**	n.a.	8	n.a.
	512 x 384	**8**	n.a.	8	n.a.

continued

Table 2-13 VRAM sizes and monitor color depths (continued)

	Screen size	Standard VRAM (1 MB)		Expanded VRAM (2 MB)	
Monitor type	Hor. x vert.	Graphics	Graphics/video	Graphics	Graphics/video
PAL	768 x 576	**16**	**8 / 16***	32	8 / 16
	640 x 480	**16**	**8 / 16***	32	8 / 16
Convolved PAL	768 x 576	**8**	n.a.	8	n.a.
	640 x 480	**8**	n.a.	8	n.a.

* With a color depth of 16 bits in these configurations, the maximum video window size is limited. If the video window width is 512 pixels or less, the height may be as large as 512 pixels; if the video window width is more than 512 pixels, the height is limited to 340 pixels.

The color depths in Table 2-13 are shown as the number of bits in which the color or grayscale value of each pixel can be encoded. The refresh rates and pixel clocking rates at which these monitors run are shown in Table 2-14, later in this chapter.

VRAM expansion requires 80-ns chips, using the same configuration of SIMM cards as VRAM expansion in other Macintosh Quadra computers. Mechanical details, timing, and pin assignments are given in "VRAM Expansion Cards," at the end of this chapter.

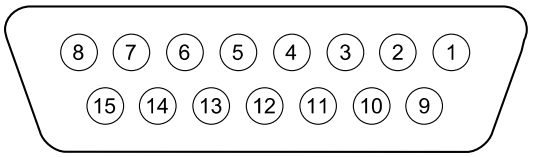
Video Monitor Interface

Either computer can be connected to a wide variety of external monitors by means of a DB-15 socket located on their back panel. Some popular monitor types are listed in the left column of Table 2-13. Signal timing diagrams for certain of these monitors are given in "Video Output Timing," later in this chapter.

Apple Technical Note 326 contains full information about connecting various monitors to the video monitor interface, including details of connector pin assignments and ID codes assigned to Apple and some third-party monitors. It also describes hard-wire connections that allow monitors to assert their ID codes and therefore automatically configure the system when they are connected. Apple Technical Note 144 contains additional information about color monitors.

Figure 2-10 shows the physical form of the DB-15 video monitor connector.

Figure 2-10 Video monitor connector



Video Output Timing

Figure 2-11 shows a general video timing diagram for Apple monitors.

Figure 2-11 Video timing diagram

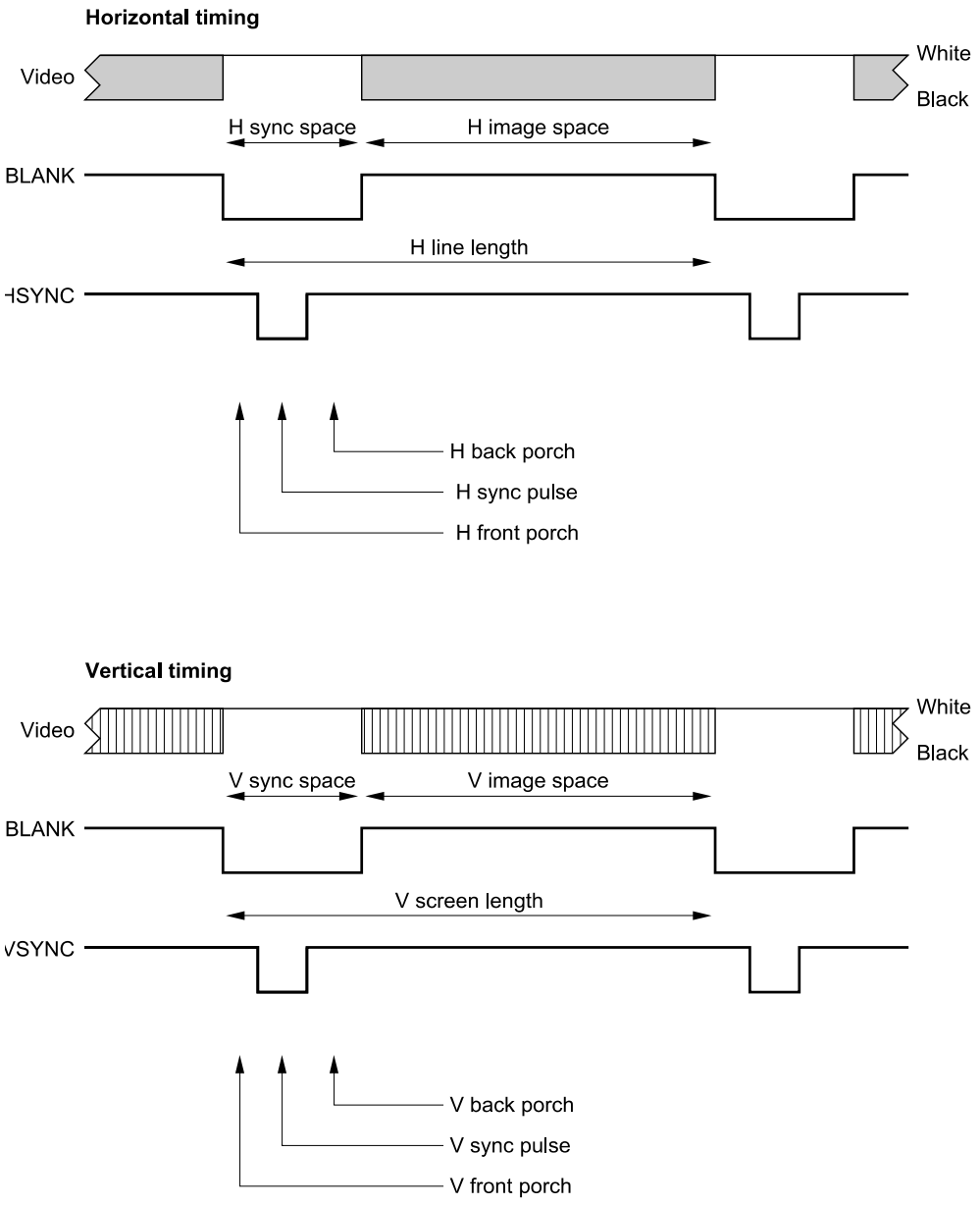


Table 2-14 gives monitor timing values. Some of these values are shown in Figure 2-11.

Table 2-14 Apple monitor timing values

Parameter	640 x 480	VGA	640 x 870	1024 x 768	1152 x 870
Dot clock, MHz	30.240	25.175	57.273	80.000	99.958
Dot interval, ns	33.069	39.722	17.460	12.500	10.004
Line rate, kHz	35.00	31.469	68.837	60.241	68.652
Line interval, µs	28.571	31.778	14.527	16.600	14.566
Frame rate, Hz	66.67	59.94	74.99	74.93	75.03
Frame interval, ms	15.000	16.683	13.336	13.346	13.328
H sync space, dots	224	160	192	304	304
H image space, dots	640	640	640	1024	1152
H line length, dots	864	800	832	1328	1456
H front porch, dots	64	16	32	32	32
H sync pulse, dots	64	96	80	96	128
H back porch, dots	96	48	80	176	144
V sync space, lines	45	45	48	36	45
V image space, lines	480	480	870	768	870
V screen length, lines	525	525	918	804	915
V front porch, lines	3	10	3	3	3
V sync pulse, lines	3	2	3	3	3
V back porch, lines	39	33	42	30	39

Miniature Videocam

Apple offers an inexpensive miniature videocam for the Macintosh Quadra 840AV and Macintosh Centris 660AV computers that uses a light-sensitive matrix on a chip with a built-in lens. The user can mount the mini-videocam above the monitor for videophone imaging or can move it about on the end of its cable to take pictures of objects or documents. With supplementary lenses, the videocam can make images of detail as fine as the wire bonds on an integrated circuit.

The mini-videocam has these general characteristics:

- image: 360 by 288 pixels, monochrome with 256 gray levels
- nominal view angle: 66°
- sensitivity: adequate for use in a dimly lit office
- depth of field (without supplementary lenses): 45 cm to infinity

- output signal: 1 V, 75 Ω composite video with PAL or NTSC timing
- software controls: exposure, gamma, image capture interval, video timing
- unit identification in firmware: camera type and features
- power drain: 50 mA at 12 V

Sound I/O

The system contains external ministereo sockets for sound I/O, connected through amplifiers to the Singer codec. The Singer uses only frame 0, leaving other frames available for other sound processing (for example, through the DAV connector). External plugs carry the left channel on the tip and the right channel on the ring, with the sleeve common. Sound I/O signals are described in Table 2-15.

Table 2-15 Sound I/O signals

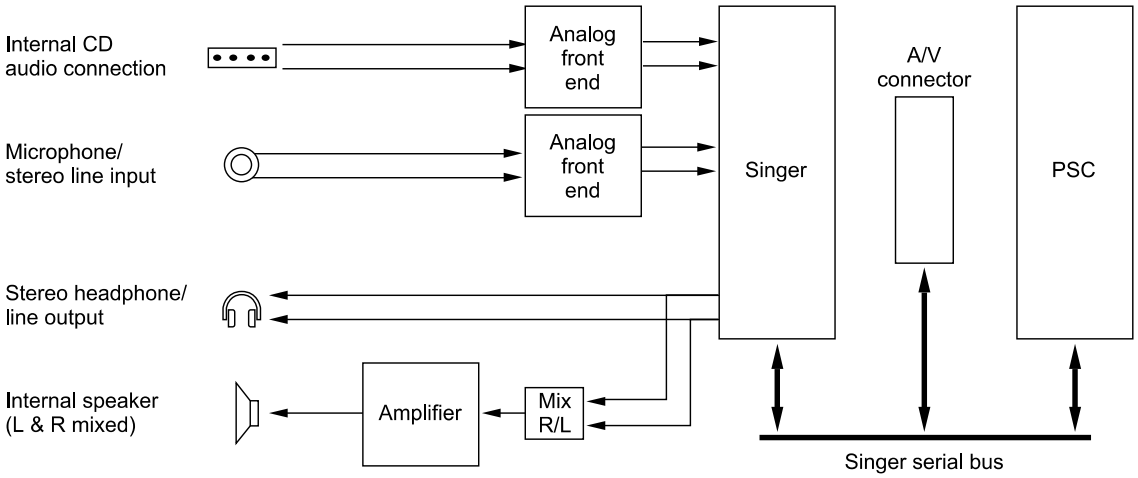
Panel label	Description
Audio In	8 kΩ impedance, 2 V rms maximum, 22.5 dB gain available
Audio Line Out	37 Ω impedance, 0.9 V rms maximum, attenuated –22.5 dB (crosstalk degrades from –80 dB to –32 dB when the audio output is connected to 32 Ω headphones)

Sound I/O bandwidth is 20 Hz to 20 kHz, plus or minus 2 dB. Total harmonic distortion and noise is less than 0.05% over the bandwidth with a 1 V rms sine wave input. The input signal-to-noise ratio (SNR) is 82 dB and the output SNR is 85 dB, with no audible discrete tones.

Both models are supplied with built-in speakers. Apple also offers a compatible high-quality microphone that is specifically designed for speech recognition applications. The components that support sound I/O are shown in Figure 2-12.

For details of speech generation and recognition in the Macintosh Quadra 840AV and Macintosh Centris 660AV, see Chapter 6, “Speech Manager,” and Chapter 7, “Introduction to Speech Recognition.”

Figure 2-12 Sound I/O components



NuBus Interface

The NuBus expansion card interface provides access between RAM or ROM and plug-in accessory cards. It is not designed to let plug-in cards access peripheral devices directly. The Macintosh Quadra 840AV accepts up to three cards; the Macintosh Centris 660AV accepts one. The expansion card implementation is based on the NuBus ’90 specification (ANSI/IEEE Std 1196-1990) and has the following new features:

- Each of the three Macintosh Quadra 840AV slots has a 4-bit geographic address. The addresses are $C, $D, and $E, corresponding to slots 4, 5, and 6 in the Macintosh II family of computers. The Macintosh Centris 660AV slot is address $C.
- All data transfers on NuBus are synchronized by a 10 MHz clock. An additional 20 MHz clock supports burst transfers in cards that conform to the NuBus ‘90 specification. This permits faster data transfers than are possible with earlier NuBus designs.
- NuBus supports a 32-bit addressing space (4 GB), accessible through justified 8-bit, 16-bit, and 32-bit data transfers.
- MUNI generates a bus error if any transaction takes longer than 25.6 µs.

For full technical details about NuBus, including NuBus ’90, see *Designing Cards and Drivers for the Macintosh Family,* third edition. For information about enabling NuBus block moves, see “NuBus Block Moves,” in Chapter 11.

The NuBus interface supports several address ranges for data transfer between the 32-bit NuBus address space and the 32-bit physical address space (which may be different from the logical space used by software).

MUNI provides separate FIFO buffers for data on the CPU bus and on NuBus. These buffers can operate concurrently. Buffer capacities are shown in Table 2-16.

Table 2-16 MUNI buffer capacities

Buffer	Read capacity	Write capacity
CPU bus	4 longwords (1 burst)	16 longwords (4 bursts)
NuBus	16 longwords (1 block 16)	32 longwords (2 block 16s)

Slot Connections

Macintosh Quadra 840AV NuBus slots accept both long (4 by 13 inches) and short (4 by 7 inches) accessory cards of the same physical configuration as those used with the Macintosh II and Macintosh Quadra families. The Macintosh Centris 660AV accepts only short accessory cards, which may be the same as short Macintosh Quadra 840AV cards. For mechanical details of long and short accessory cards, see *Designing Cards and Drivers for the Macintosh Family,* third edition.

The single Macintosh Centris 660AV NuBus slot requires an adapter card that places its NuBus accessory card parallel to the main circuit board, as shown in Figure 2-13. The adapter card carries the MUNI chip, so this chip is present in the system only when the adapter card is installed. For card mounting information, see Appendix D, "Mechanical Details."

Figure 2-13 Macintosh Centris 660AV accessory card mounting