

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HTC CORPORATION and HTC AMERICA, INC.,¹
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

Case IPR2015-01502
Patent 7,542,045 B2

Before JAMES B. ARPIN, MATTHEW R. CLEMENTS, and
SUSAN L. C. MITCHELL, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; and LG Electronics, Inc. were terminated from this proceeding. *See* Papers 28 and 41.

I. INTRODUCTION

In its Petition requesting *inter partes* review, HTC Corporation and HTC America, Inc. (collectively, “Petitioner”) asserted the unpatentability of claims 1, 2, 4–7, 9, 10, 12, 13, and 15–17 (“the challenged claims”) of U.S. Patent No. 7,542,045 B2 (Ex. 1001, “the ’045 patent”), owned by Parthenon Unified Memory Architecture LLC (“Patent Owner”). Paper 2 (“Pet.”), 1. The Petition identifies HTC Corporation; HTC America, Inc.; LG Electronics, Inc.; LG Electronics U.S.A., Inc.; LG Electronics MobileComm U.S.A., Inc.; Samsung Electronics Co., Ltd.; and Samsung Electronics America, Inc. as real parties-in-interest. *Id.* at 2. We have jurisdiction under 35 U.S.C. § 6, and this Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during the review. For the reasons discussed below, we determine that Petitioner has met its burden to prove, by a preponderance of the evidence, that claims 1, 2, 4–7, 9, 10, 12, 13, and 15–17 of the ’045 patent are unpatentable on the grounds upon which we instituted *inter partes* review.

A. *Procedural History*

On June 24, 2015, Petitioner filed a Petition to institute an *inter partes* review of claims 1, 2, 4–7, 9, 10, 12, 13, and 15–17 of the ’045 patent. Pet. 1. Petitioner asserted grounds for unpatentability based on the following references and declarations:

Exhibit	References and Declarations
1002	File History of Patent No. US 7,542,045 B2
1003	Patent No. US 5,546,547 (“Bowes”)

Exhibit	References and Declarations
1004	International Organization for Standardization, “ISO/IEC 11172-2: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video,” (1st ed. Aug. 1, 1993) (“MPEG”)
1005	S. Rathnam <i>et al.</i> , “An Architectural Overview of the Programmable Multimedia Processor, TM-1,” PROC. COMPCON, IEEE Computer Society Press, Los Alamitos, CA, 1996, pp. 319–326 (1996) (“Rathnam”)
1007	Patent No. US 5,774,676 (“Stearns”)
1008	Declaration of Santhana Chari, Ph.D.
1030	Declaration of Harold S. Stone, Ph.D.

Pet. vii–viii. Patent Owner filed a Preliminary Response (Paper 7). On January 6, 2016, we issued an Institution Decision (Paper 14, “Inst. Dec.”), instituting *inter partes* review on the following grounds:

References	Basis	Claims challenged
Bowes and MPEG	35 U.S.C. § 103(a)	1, 4, 5, 7, 10, 12, 16, and 17
Bowes, MPEG, and Rathnam	35 U.S.C. § 103(a)	9 and 15
Bowes, MPEG, and Stearns	35 U.S.C. § 103(a)	2, 6, and 13

Inst. Dec. 29; *see* Pet. 5–6.

After institution, Patent Owner filed a Patent Owner Response to the Petition (Paper 21, “PO Resp.”), and Petitioner replied (Paper 32, “Reply”). A hearing for the instant proceeding and related Cases IPR2015-01500 and IPR2015-01501 was held on September 19, 2016. A transcript (Paper 51, “Tr.”) of that hearing is included in the record.

B. *Related Proceedings*

The ’045 patent is involved in several cases pending in the U.S. District Court for the Eastern District of Texas. Pet. 2–4; Paper 5, 2–3. Petitioner also has filed other petitions seeking *inter partes* review of related

patents in related Cases IPR2015-01500 and IPR2015-01501. Pet. 3–4. Further, an unrelated petitioner, Apple Inc., has filed a petition challenging claims of the '045 patent. *See* IPR2016-01134, Paper 7, 2 & 32 (instituting *inter partes* review of claims 1, 4, 5, 7, 9, 10, 12, and 15–17).

II. THE '045 PATENT (EX. 1001)

A. *Subject Matter*

The '045 patent relates generally “to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.” Ex. 1001, col. 1, ll. 36–41. As of the effective filing date of the '045 patent,² a typical decoder included a dedicated memory, which represented a significant percentage of the cost of the decoder and which went unused most of the time. *Id.* at col. 2, ll. 21–63, col. 4, ll. 43–60, Figs. 1a–1c.

To address these and other concerns, the '045 patent discloses an electronic system in which a first device and a video and/or audio decompression and/or compression device are coupled to a shared memory through a bus that may have bandwidth sufficient for the video and/or audio

² The '045 patent claims the benefit of a string of earlier-filed U.S. patent applications, the earliest of which was filed on August 26, 1996. Ex. 1001 at [63]. Petitioner does not challenge the entitlement of the '045 patent to this earliest filing date and argues that the '045 patent expired in August of 2016, presumably based on this earliest filing date. Pet. 12–13. Patent Owner implicitly claims the entitlement of the '045 patent to the benefit of this earliest filing date and expressly states that the '045 patent expired on August 26, 2016. Paper 8, 1.

decompression and/or compression device to operate in real time. *Id.* at col. 4, l. 64–col. 5, l. 7. Figure 2 of the '045 patent is reproduced below.

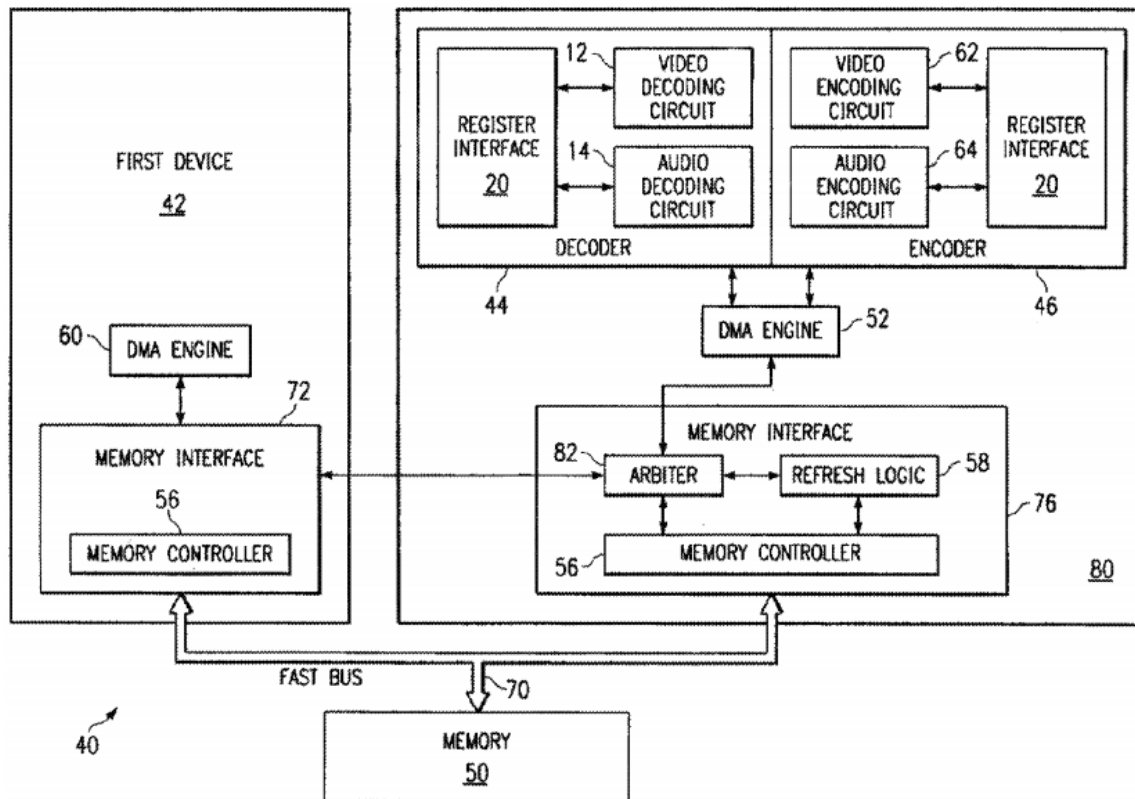


Fig. 2

Figure 2 is a block diagram of an electronic system that contains a device with a memory interface, an encoder and decoder. *Id.* at col. 6, ll. 3–5.

“First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50”

Id. at col. 6, ll. 29–32. Both first device 42 and decoder/encoder 80 have access to memory 50 through memory interfaces 72 and 76, respectively, coupled to fast bus 70. *Id.* at col. 6, ll. 27–29, col. 7, ll. 26–28, 48–51. Fast bus 70 may have at least the bandwidth required for decoder/encoder 80 to operate in real time and, preferably, has a bandwidth of at least

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