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High resolution smart image sensor with integrated parallel analog processing for multiresolution edge extraction

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Abstract

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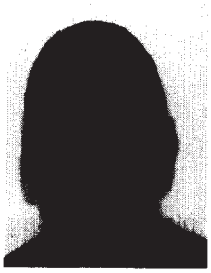
This paper presents a vision sensor which generates a multiresolution edge description using parallel analog processing support. Its multimodule architecture is based on a Multi-port Access of photo-Receptor (MAR) hexagonal sensor coupled to an external but powerful analog processing unit and a microcoded digital interface. The system supports image scanning and edge tracking. Satellite analog processing allows extensive computation using VLSI technology, leaving all the sensor area available for photo-transduction and communication pathways. It is thus possible to design a sensor with up to 500×500 pixels on a single CMOS chip using 1.2 μm technology. The goal of the approach described here is to exploit an imbedded edge tracing algorithm in order to generate a scene description as a list of connected edge segments. Experimental results are presented for the current prototype which implements 256×256 pixels with corresponding multiresolution edge maps.

Keywords: Smart sensor; Image processing; Edge detection; Scale-space integration; Hexagonal image sensor



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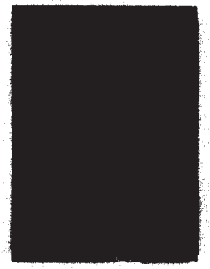
1. Introduction

Visual perception must be developed in relation with the needs of the recognition processes in order to define efficient and adaptative automation tasks or mobile robot applications. A large part of the computational effort in computer vision is related to low level repetitive processing which can best be implemented at the sensor level [12]. It is well known that biological visual systems include aspects of image preprocessing on the first layers of neurons within the retina. It has been suggested that this low level image processing is related to multiresolution edge extraction [9]. This natural organization reduces the amount of data to be routed to the visual cortex for further recognition [3].

Computational sensing is a novel research area which targets the integration of such image processing by merging transduction devices and analog signal processing modules. Interesting solutions exploit natural properties of semi-conductor devices in order to implement simple but powerful computational functions on a very small silicon area [4]. The bidimensional implementation of computational sensors is confronted to trade off between the spatial resolution of the sensor and the complexity of the imbedded electronics. This paradox will be real until microelectronic technology can offer higher integrated level or 3D structures, which would remove limitations of fully parallel implementation of analog processing at the sensor level. In many cases, it is not advantageous to simultaneously compute a large number of edge data if sequential (slow) scanning is required for the extraction of these primary results. Previous work on smart sensing has considered the design of complex photo-sensitive elements [14] with emphasis on the communication between neighbors [7], [8]. Other approaches use the implicit access of parallel row data at one end of the photo-sensitive array for SIMD computation, [5] or a complete sequential processor which is implemented on a same substrate [1]. A common goal of these approaches and of the one discussed in this paper is to integrate photo-sensitive elements on CMOS or CCD technologies [14,16].

The sensor architecture described here uses a serial-parallel approach in order to yield a balance of resolution and computational capabilities. Emphasis is put on an efficient communication strategy in order to extract a local description of focal plane illuminance and exploit it by an external analog processing module. The main interest of this architecture is related to the parallel analog filtering made possible by using several different operators which are driven in common by the set of primary outputs of the sensor. It is thus possible to generate, in a single scan period, a multiresolution edge description of a scene using band-pass filters with different scales. This type of satellite analog processing is discussed in Section 2 with the proposed open architecture for dedicated post-processing on primary edge data. The Multi-port Access of photo-Receptor (MAR) architecture is presented in Section 3 with its pixel electronics and the basic operating mode. Section 4 describes the parallel analog module which implements multiresolution Laplacian-of-Gaussian operators followed by a zero-crossing evaluation module. The microcoded edge tracking algorithm is described in Section 5. The paper concludes with experimental results which have been obtained from a current prototype of 256 × 256 pixels.



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2. The system architecture

2.1. Satellite analog processing

The implementation of focal plane processing implies a delicate balance between pixel complexity, spatial resolution, and data flow. It is clear that the small cell size of a 2D photo-sensing array leaves only a limited area available for computation. In the case of large arrays, until technology allows much denser circuits (or 3D structures), most of the non-photosensitive area

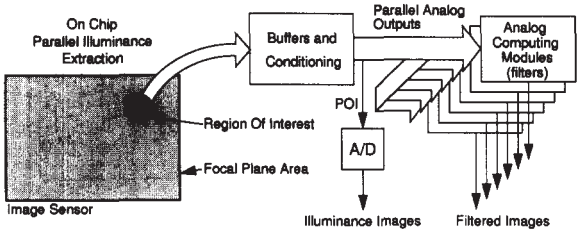

Fig. 1. Satellite processing approach. The set of primary analog outputs which represents the illuminance of the region of interest addressed within the sensor is used by several analog filters in order to implement the extraction of multiresolution primitives. The pixel of interest itself is also routed to an A/D converter in order to output illuminance data.

will have to be dedicated to communication, with little built-in processing. Furthermore, there exist serious I/O limitations. For instance, even if edge information could be computed in parallel within each pixel, a simultaneous read-out of such data over large image regions shall remain challenging. Current technologies favor simple operators with great spatial homogeneity. The MAR architecture recognizes such a trade-off between the simplicity of the basic pixel design and the complexity and penalty of rapid communication by making use of external, but tightly coupled, processing support.

This so-called *satellite processing* is illustrated in Fig. 1, which shows the conceptual representation of a device with relatively high resolution and its associated off-chip parallel analog processing. The dark circle on the sensor delineates a region of interest (ROI) centered on the pixel of interest (POI) from which illuminance data is retrieved and routed to a conditioning module. These channels are commonly used by a set of N different analog filters which may implement multiresolution and/or directional edge extractors, Gaussian filters, etc.

2.2. Post-processing module integration

While computational sensor development remains our main research topic, several other projects are in progress as VLSI co-processing modules which will operate in the immediate periphery of the sensor. These modules share a single memory block with the sensor and other co-processing modules. Such processing could include scale-space integration, shape from shading, stereo disparity evaluation using two MAR sensors, image calibration for further photometric use of the sensor, and others. A main digital controller is designed for driving specific protocol signals, data flow and memory addressing on a hexagonal tessellation. It also implements a microcoded instruction set which defines complex sequences displacement for the POI within the sensing array. Finally, the controller is responsible for interfacing the MAR system with the host computer and provides bidirectional interrupt capabilities which offer interactive feature extraction, especially during the edge tracking process. This open and modular architecture facilitates the development of other co-processing elements because none have direct functional consequences on the others.

3. Basic organization of the hexagonal MAR sensor

In conjunction with the satellite processing approach, the present sensor development has been oriented towards the following objectives: (1) highest possible spatial resolution using current VLSI technology, (2) possibility of using multiresolution edge analysis in order to extract relevant characteristics from a scene, (3) access to custom video rate and format for automatic light adaptation without constraint emerging from historical video standards, and (4) emphasis on data base description of early primitives rather than real-time display of illuminance images: *it is not an imaging sensor*. This section explains how these objectives have been met by using a hexagonal multi-port addressing strategy and presents its associated design and operating constraints.

3.1. Multi-port access on a hexagonal tessellation

The pixel architecture is based on a multi-port addressing strategy. The selection circuitry is similar to a multi-port memory except that selection busses are routed geometrically in order to define the shape of the kernel and that retrieved data are analog and represent pixel illuminance. The implementation of computational sensors is not restricted to a conventional rectangular grid. Even if low level algorithms in computer vision are often designed Cartesian tessellation, the hexago-

nal pattern was chosen for three main reasons: (1) Immediate neighbors of any pixel of interest are located at a same radial distance, which facilitates the implementation of circularly symmetric operators, (2) multi-port addressing of hexagonal pixels is naturally implemented using a set of colinear data busses, and (3) a hexagonal tessellation is highly regular and facilitates the representation of curved lines or surfaces [6].

Fig. 2 shows an overall block diagram of the MAR sensor. The core area is composed of a 2D matrix of multi-port access pixels where the POI is addressed by three concurrent selection lines. The white star represents the addressed pixels which are simultaneously extracted from the sensor. The topology allows access to the illuminance data of the POI together with the illuminances of all neighbors located on the three axes of symmetry of the array (corners of the concentric hexagon). Each illuminance signal is routed from the sensor on an individual channel and is fed to the external analog module for spatial filtering operations. Each set of selection busses (named Y, X_1 and X_2) is activated by a bidirectional shift register. A fourth register (named T) is used to control the parallel analog multiplexor on the upper region of the sensor. Unlike in conventional video sensors, the POI may be moved along any of the axes of the underlying hexagonal structure, thus allowing very flexible scanning strategies. A direction code which uses 3 bits is internally decoded in order to control shift regis-

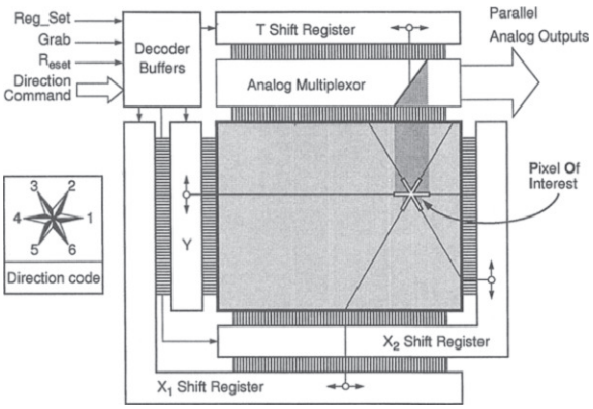

Fig. 2. Block diagram of the MAR Sensor. A set of four bidirectional shift registers drive selection lines which converge upon the POI. A decoder module uses a direction code of three bits in order to drive each shift register. The analog data path is shown in the shadowed area until it reaches the analog multiplexor.

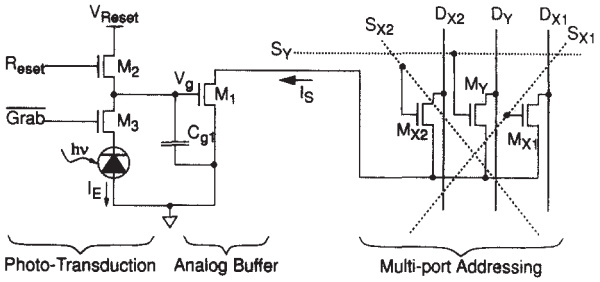

Fig. 3. Multi-port addressing architecture of each pixel and non-destructive read-out of illuminance data. The photo-diode drives the gate voltage V_g of transistor M_1, which is then translated to a proportional output current I_s.

ters for both motion and direction. *Reg_Set* is used to initialize the four shift registers, R_{eset} initializes the integration process which is discussed in Section 3.2 while the $\overline{Grab}$ signal is used to stop the integration process during scanning.

The circuit organization of each pixel is presented in Fig. 3. It can be divided in three main parts: (1) photo-transduction, (2) signal buffering, and (3) multi-port addressing. The single current I_S which is generated by the integration of photo-current I_E on the gate capacitance of transistor M_1, is retrieved through a set of three N transistors (M_Y, M_{S1} and M_{X2}) according to the status of the selection lines. It may be shown [15] that the output current I_S may be expressed by the following expression:

$$I_S = \frac{\beta}{2}\left(\left[\left(\sqrt{V_{Reset} - V_{SN} + V_\gamma} - \frac{K}{2C_{g1}}E_{in}t_i\right)^2 - V_\gamma\right] - V_t\right)^2, \quad (1)$$

where K is a CMOS process constant, β is the current gain of the transistor M_1, V_{SN} is the voltage drop of an N transistor due to threshold effect, V_γ is the forward voltage drop of a PIN diode (approx. 0.6 V), V_t is the threshold voltage of the transistor M_1, t_i is the photo-current integration time and E_{in} is the input illuminance of the pixel.

3.2. Non-destructive read-out of pixel information

Transistor M_1 operates as an analog transconductance buffer and is required to ensure a non-

destructive read-out of the illuminance data during pixel access. This property is critical because each pixel is addressed several times due to the parallel analog nature of the MAR architecture. The MAR sensor has a global *Reset* signal for the entire array which applies voltage V_{Reset} on the gate of transistor M_1. The integration process is thus uniform for each pixel of the sensor and the reading of the output current I_S is non-destructive, with voltage V_g remaining unchanged irrespective of the frequency or duration of the access to a pixel element. This property is essential since, after a complete scan of the sensor, each pixel is addressed as often as the number of pixels on the extraction kernel.

3.3. The MAR sensor operation

The typical operating mode of the MAR sensor is presented in Fig. 4 for the two extreme values of scene illuminance in a bright and in a dark region, when only one pixel is selected during the scanning window t_s (for proper biasing of output transistor M_1). For the dark case, photocurrent I_E is limited to the reverse leak current of the photo-diode which causes a small deviation ΔV_g on the gate of M_1. In this condition the output current is maximum. The bright case is illustrated for an unsaturated pixel which sinks a small current (near zero) until a minimum threshold voltage V_t is applied at the gate of the output transistor. If an isolated region has a very high level of illuminance (caused by a light source in the scene or specular reflections for instance)

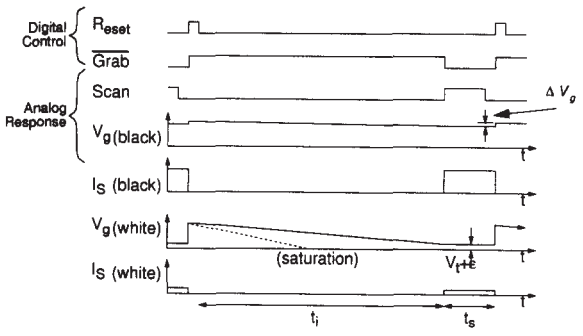

Fig. 4. The timing diagram shows a typical illuminance integration cycle and its associated scan (read-out) cycle for the two extreme cases of scene illuminance. The maximum output current is associated with a dark region while a null output corresponds to a highlighted pixel.

pixels in this region will saturate. In this case (see dotted line in Fig. 4), the gate voltage decreases rapidly, resulting in a zero current output signal in the entire saturated region without any effect on the unsaturated neighbor pixels.

The global $\overline{Grab}$ signal is used to interrupt the integration process during the scan period, especially in conditions of heavy light, in order to avoid that the integration time be longer for the last visited pixels than for the first ones. It is clear that the integration process of the MAR sensor is not limited to proceed at a standard video rate (1/30 sec). This is a very useful characteristic. The integration duration t_i may be adjusted by the operating system depending on the illumination condition of the scene. This parameter is then defined as an equivalent aperture control (or the light source intensity thereof). A simple procedure which uses the histogram of a previous image could dynamically adjust the level of the white saturation of pixels by changing the integration time t_i The range of adjustment for this parameter is only limited by the voltage deviation due to the dark current of the back-biased PN junction.

4. Analog image processing for multiresolution edge extraction

Marr's theory suggests to analyze edges using a multiresolution strategy [9,10,11] in order to discriminate, from noisy (but accurate) edges, those which represent relevant features in the scene. In this approach, edge extraction refers to the zero-crossing location in the resulting filtered image when it is convolved with the Laplacian-Of-Gaussian (LOG) operator. A multiresolution analysis is simply a variation on the standard deviation σ of the Gaussian. A relevant property of the MAR sensor is its parallel analog filtering capability which allows a very fine sampling, in the scale domain, of the zero-crossing maps from the highest frequency filters to the lower ones. The kernel has a sufficiently large diameter in order to implement low frequency filters for significant feature extraction and high frequency rejection. The current version of the analog multiresolution edge extraction implements 16 different LOG filters as a resistor network from $\sigma = 0.5$ (or Laplacian operator) to $\sigma = 6.9$. This section presents some

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