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DECLARATION OF GERARD P. GRENIER

I, Gerard P. Grenier, do hereby state that:

1. I am currently Senior Director of Publishing Technologies for the Institute of Electrical and Electronics Engineers (IEEE), 445 Hoes Lane, Piscataway, New Jersey.

2. I have been asked to confirm certain dates regarding the following article (the "Article"):

   G. Wang, et al., "CMOS Video Cameras," Euro ASIC '91, Paris, France, May 27-31, 1991.

3. A true and correct copy of the Article accompany this declaration as Exhibit A.

4. IEEE is a neutral third party to the dispute in this IPR.

5. Neither I nor IEEE itself is being compensated for this declaration.

6. The Article was published by IEEE. Copies of the conference proceedings were made available to attendees of the conference. The Article is currently available for public download from the IEEE digital library, IEEE Xplore (www.ieeexplore.ieee.org).

7. IEEE maintains records of the dates on which articles were first made available for public download. These records are maintained as part of the ordinary course of business of the IEEE, are updated regularly as articles are published. I have personal knowledge of the records.

8. I have reviewed the IEEE records relating to the Article.

9. IEEE's records confirm the following:

   a) "CMOS" Video Cameras" was presented as part of Euro SIC '91 which occurred May 27-31, 1991.

   b) IEEE has registered this conference with U.S. Copyright Office.

I declare under penalty of perjury that the foregoing statements are true and correct.

Executed on: June 30, 2014

VALEO EXHIBIT 1039
Valeo v. Magna
IPR2015-____

EXHIBIT A

CMOS video cameras

Wang, G. ; Dept. of Electr. Eng., Edinburgh Univ., UK ; Renshaw, D. ; Denyer, P.B. ; Lu, M.

A single chip CMOS video camera is presented, along with design technique and characterization results. The chip comprises a 312*287 pixel photodiode array together with all the necessary sensing, addressing and amplifying circuitry, as well as a 1000 gate logic processor, which implements synchronization timing to deliver a fully-formatted composite video signal and a further 1000 gate logic processor, which implements automatic exposure control over a wide range. There are also simple solutions for gamma correction and test.<>

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