On-chip Automatic Exposure Control Technique

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ABSTRACT

This paper introduces techniques for the electronic variation & automatical control of exposure in solid-state image sensors. A novel electronic aperture and a simple exposure controller are described, which have been integrated on chip with a CMOS image sensor array. The technique can achieve a wide range exposure control of 40,000:1. This is equivalent to 15 stops of a mechanical iris system.

1. INTRODUCTION

Automatic exposure control is of significance to avoid mechanical iris control in electronic vision systems. This paper discusses two related issues: 1) how to electronically settle exposures (electronic aperture), and 2) how to automatically control the exposure (electronic controller). This paper emphasizes on-chip design because recent development in CMOS sensor-processor technology has provided a new method for implementing control logic with the sensor array on the same substrate[1,2].

An on-chip electronic aperture, equivalent to eight stops of a mechanical system has been reported before[3]. We present here a novel scheme, which enables exposure adjustment over a much wider range of 40,000:1, equivalent to 15 stops of a mechanical system. The electronic aperture is achieved by varying the integration period, thus varying the sensitivity of the photo array. The integration time is defined to be the sum of a variable number m of line intervals plus a variable number n of pixel clock intervals. Therefore, the maximum exposure setting is a field time, and the minimum setting is a few pixel clock periods.

If we now alter the exposure setting in response to the monitored image, we can implement fully automatic electronic exposure control. A simple control mode is described in this paper, which costs approximately 1,000 gates to implement. The control is achieved by monitoring the image pixel stream and estimating the fractions of each picture which are very white and very black. On the basis of this information, the device decides whether the picture contrast is acceptable, or too bright, or too dark. If necessary, the exposure time is then changed in the appropriate direction.

The techniques have been used in several designs, covering applications from single-chip CMOS video cameras[4], to single-chip "smart" vision systems such as burglar-alarm verification cameras.

2. ELECTRONIC APERTURE

Algorithm The architecture of the MOS image sensor is shown in Figure 1. The light sensing area consists of a photodiode array. The photodiodes are pre-charged to a fixed bias voltage during a reset cycle and then isolated for a suitable exposure time. During this time incident light partially discharges the junction capacitances, through the generation of photo-current in the diodes. For each pixel, the exposure is determined by the pixel integration time i.e. the time between resetting and sampling. When using the normal scheme of scan registers this integration time has to be a fixed number of clock cycles (usually a field time).

The novel scheme is to define the sample and reset signals in such a way that the time between them can be varied. The integration time t_{int} is then defined to be the sum of a variable number m of line intervals plus a variable number n of clock intervals:

$$t_{int} = m \times t_{line} + n \times t_{clk}$$

where t_{clk} is the pixel clock period and t_{line} is the line period. $(n \times t_{clk} \leq t_{line}, m \times t_{line} \leq t_{field})$. We refer $m \times t_{line}$ as *coarse settlement*, and $n \times t_{clk}$ as *fine settlement*.

-coarse settlement: At a particular line time, row i is being sampled and then reset, rows $i+1$ through $i+m$ are integrating and all other rows are being reset during the line period, as shown in Figure 2.

-fine settlement: Fine settlement is achieved by varying the reset period. The reset time can range between a few clock intervals and nearly one line time, resulting in extra integration time $n \times t_{clk}$ added to the coarse settlement. The fine settlement becomes more important when $m \times t_{line}$ is smaller. In fact, the exposure is dominated by the fine settlement when m equals 0.

Circuitry The problem is then to generate and decode suitable signals in such a way as to enable the correct rows and columns of the array in sequence. The vertical scan register has been replaced by a scan register with decoding, as shown in Figure 3 and Figure 4. The single-bit data-stream has been augmented with other signals, such as scan, sample, and reset.

3. ELECTRONIC EXPOSURE CONTROLLER

Algorithm The image pixel stream is compared with two DC references to pick up "very white pixels" and "very black pixels". A "very black pixel" means its value is below a black reference and a "very white pixel" is above a white reference. These occurrences are counted, and a threshold number is set to judge the present exposure. If "very black pixel" number is greater than the threshold number and "very white pixel" number is less, the picture is thought to be too dark, and the exposure should be increased. On the other hand, if the "very white pixel" number is greater than the threshold number and the "very black pixel" number is less, the picture is thought too bright, and the exposure should be decreased. When the numbers are both greater or both less than the threshold, the exposure is thought to be acceptable. No action will needed in this case.

The new integration time is calculated according to the following formula:

$$T_{new} = T_{pre}(1 \pm step) \quad \text{, if exposure is increased/decreased;}$$
$$= T_{pre} \quad \text{, if no action.}$$

where, T_{new} is new integration time for the next frame, T_{pre} is the present integration time.

Circuitry Figure 5 shows the block diagram of a simple exposure controller, which costs approximately 1,000 gates.

-comparator: The video stream is fed into this block. Two DC voltage references are set to identify "very white pixels" and "very black pixels".

-judge: This block judges the present exposure by counting numbers of "very black" and "very white" pixels according to the above algorithm.

-calculator: The new integration time is calculated here according to the above formula.

-driving block: This block produces the driving signals, according to T_{new}, needed by electronic aperture, such as scan, reset and sample.

4. APPLICATIONS

We report here two working cameras, as examples of on-chip automatic exposure control techniques.

The first example is a single-chip CMOS video camera[4]. It has a 312×287 pixel sensor array, together with the necessary sensing, addressing, and amplifying circuitry. The chip has a 2,000 gate logic processor. Half of these gates generate synchronization timing to format a standard composite video output. The other half of the gates are the exposure controller. The chip measures 7.58×7.56mm, using 1.5 μm, 2 level metal CMOS technology. The exposure controller and decode circuitry occupies 10% of the area.

Our second example is a low-resolution camera for use in security applications. The chip has a smaller sensor array (156×100) but more control functions, measures 5.57×4.00mm in the same technology as the first example. The exposure controller and decode circuitry in this case occupies 20% of the area.

Both camera modules include the camera chip with an attached miniature lens, a clock source, a 5 volt power supply, plus one bipolar transistor and a small number of resistors and capacitors required to match the line impedance to the monitor and decouple the power supply. Satisfactory exposure control performance has been achieved for both. The exposure range is 40,000:1 and quality of the pictures are good across the entire range. The automatic adjustment is fairly smooth and fast.

5. CONCLUSIONS

We have developed a novel electronic aperture and a simple exposure controller, which can be integrated with image sensor to form single-chip vision systems. Comparing with today's solid-state cameras, the control range is much wider, and the cost, power consumption and size are dramatically reduced.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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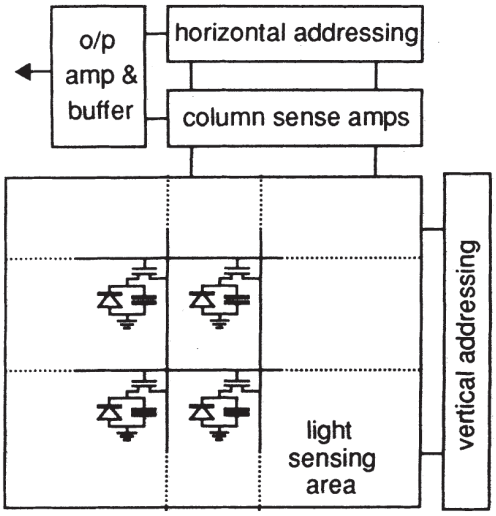

Figure 1. Architecture of the image sensor

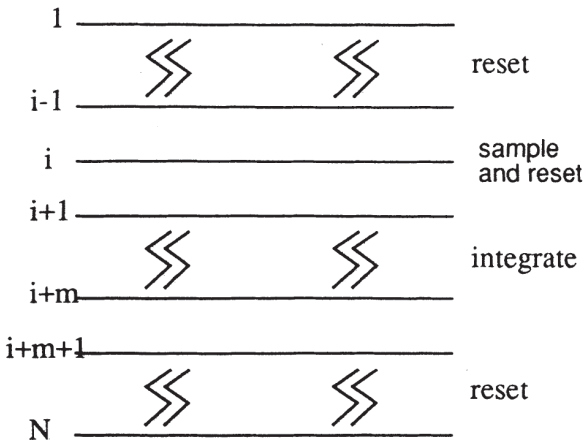

Figure 2. Function at each row

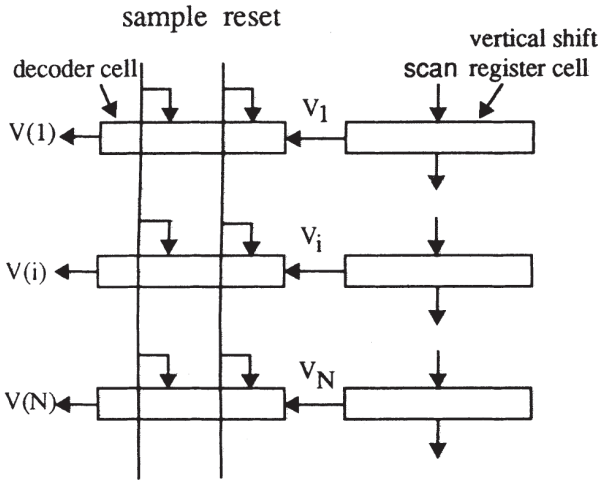

Figure 3 . Vertical shift register with docoding

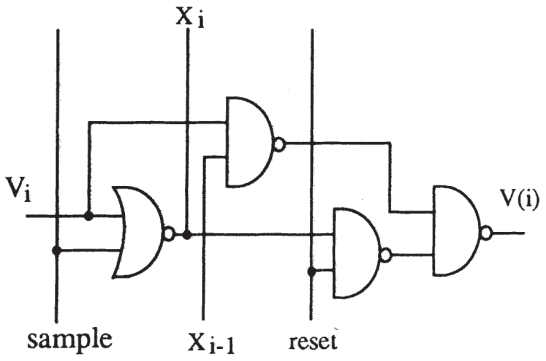

Figure 4 . Decode circuitry

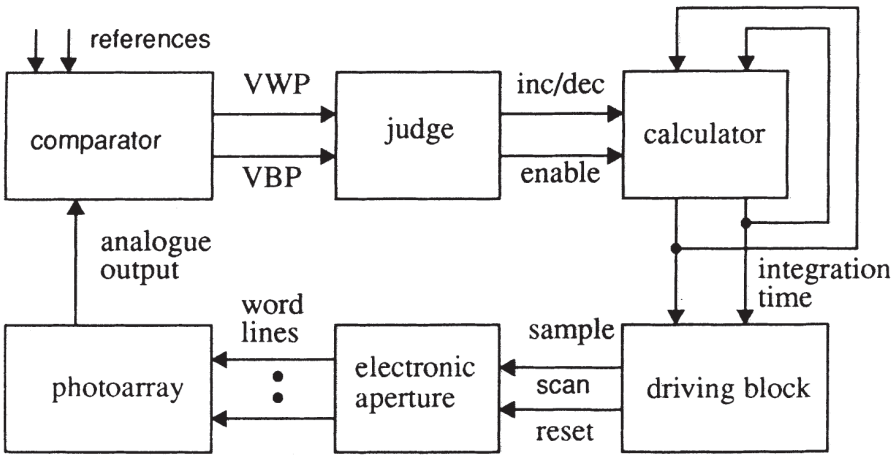

Figure 5. Block diagram of electronic exposure controller