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DECLARATION OF GERARD P. GRENIER

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2. I have been asked to confirm certain dates regarding the following article (the "Article"):

   G. Wang, et al., "CMOS Video Cameras," Euro ASIC '91, Paris, France, May 27-31, 1991.

3. A true and correct copy of the Article and Article abstract accompanies this declaration as Exhibit A.

4. IEEE is a neutral third party to the dispute in this IPR.

5. Neither I nor IEEE itself is being compensated for this declaration.

6. The Article was published by IEEE as part of the conference proceedings on the date of the conference. Copies of the conference proceedings were made available to attendees of the conference. The Article is currently available for public download from the IEEE digital library, IEEE Xplore (www.ieeexplore.ieee.org).

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8. I have reviewed the IEEE records relating to the Article.

9. IEEE's records confirm the following:

   a) "CMOS" Video Cameras" was published and presented as part of Euro SIC '91 which occurred May 27-31, 1991.

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EXHIBIT A

CMOS video cameras

Full Text
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A single chip CMOS video camera is presented, along with design technique and characterization results. The chip comprises a 312*287 pixel photodiode array together with all the necessary sensing, addressing and amplifying circuitry, as well as a 1000 gate logic processor, which implements synchronization timing to deliver a fully-formatted composite video signal and a further 1000 gate logic processor, which implements automatic exposure control over a wide range. There are also simple solutions for gamma correction and test.<>

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CMOS Video Cameras

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Abstract

A single chip CMOS video camera is presented, along with design technique and characterization results. The chip comprises a 312×287 pixel photodiode array together with all the necessary sensing, addressing and amplifying circuitry, as well as a 1,000 gate logic processor, which implements synchronization timing to deliver a fully-formatted composite video signal and a further 1,000 gate logic processor, which implements automatic exposure control over a wide range. There are also simple solutions for γ correction and test.

1. Introduction

We introduce a new capability that extends the CMOS ASIC marketplace in a sector of high growth rates. This market sector is that of image sensing and processing, covering applications from electronic cameras to 'smart' vision systems.

Camera and vision systems addressed by today's CCD technology appear cumbersome, power-hungry and expensive. The experimental work reported here demonstrates that high-quality image sensors can be implemented entirely in commodity ASIC CMOS technology, operating from single 5v supplies.

The reported chip is a highly-integrated CMOS VLSI camera, shown in Figure 1. Most of the core area is a 312×287 pixel image sensor array, together with the necessary sensing, addressing and amplifying circuitry. The output signal can be either linear or γ corrected. γ correction is achieved by a simple solution which uses the nonlinear I_D-V_{GS} characteristic of an MOS transistor. The layout of the sensor is custom designed to make it as compact as possible.

At the top (Figure 1) is the 2,000 gate logic processor, laid out using a semi-custom standard-cell compiler. Half of these gates generate synchronization timing, including line-sync and frame-sync signals to format a 625line/50Hz standard composite video output. The other half of the gates are included to electronically control exposure over a wide range (40,000:1), enabling the use of a single fixed-aperture lens. The chip measures 7.58*mm* ×7.56*mm*, using 1.5 μm, 2 level metal CMOS technology.

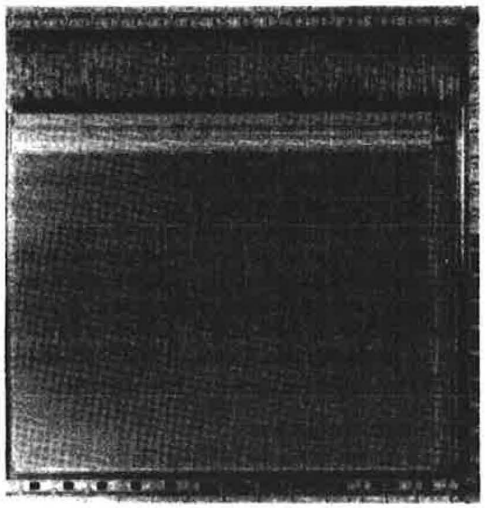

Figure 1. Photo-micrograph of single chip video camera

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A video camera has been built using this chip along with a 6 MHz clock source, a 5 volt power supply, plus one bipolar transistor and a small number of resistors and capacitors required to match the line impedance to the monitor and decouple the power supply. The picture quality is subjectively excellent, and compares well with commercially available cameras.

2. Image Sensor Block

The architecture of the image sensor is shown in Figure 2. The light sensing area consists of a 312×287 diode array matrix, schematically indicated by the columns and rows of individual photodiodes. The pixel size is $19.6\mu m \times 16\mu m$, giving a light sensing area of $6.12mm \times 4.59mm$. This corresponds to the standard 1/2" format.

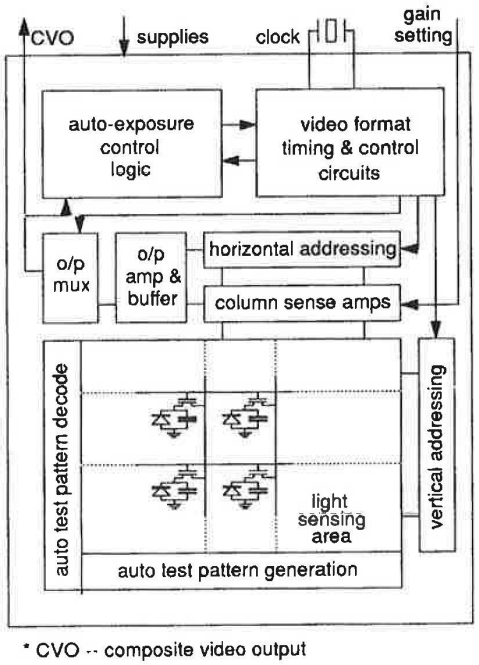

Figure 2. Architecture of the image sensor

The photodiodes are accessed on the basis of sequential selection of each row through a vertical shift register. At the top of each column is a sense amplifier. The sensed information is read out sequentially along the x-direction under control of a horizontal shift register. At the end of the path there is an output amplifier [1,2].

The sense amplifier is a single-ended differential charge integrator. Its performance demands an accurate capacitor, formed by metal1/metal2 and metal1/poly. However, commodity ASIC CMOS technology sometimes can not guarantee the resulting capacitance values. We designed a gain-controllable integrator, shown in Figure. 3, which allows wide range of programmable variation of the capacitance value.

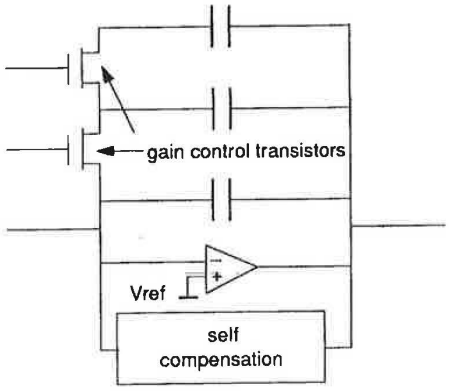

Figure 3. Integrator with programmable gain and self compensation

The main concern in the output stage design is the read-out speed required to achieve high resolution. A 6 MHz clock was chosen for this design; this gives a horizontal resolution of 312 pixels. The resultant picture quality is assured by a two stage output buffer with sample and hold function.

3. Automatic Exposure Control

The device automatically controls its exposure over a range of 40,000:1. Control is achieved by varying the integration time prior to reading each row of pixels. The integration time can be as long as one field, or as short as three cycles of the pixel clock(about 500ns).

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