IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Morton *et al*.

U.S. Patent No.: 7,296,121 IPR Control No.: IPR2015-01376

Issue Date: Nov. 13, 2007 Appl. Serial No.: 10/966,161 Filing Date: Oct. 15, 2004

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR

SYSTEMS

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PETITION FOR INTER PARTES REVIEW OF UNITED STATES PATENT NO. 7,296,121 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42



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		2. "interconnected by a first point-to-point architecture" (claims 1,	
		16, 25)	
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EXHIBITS

APPL-1001	U.S. Patent Number 7,296,121 to Morton et al. ("the '121 Patent")
APPL-1002	Excerpts from the Prosecution History of the '121 Patent ("the Prosecution History")
APPL-1003	U.S. Patent Application Publication Number 2002/0053004 to Pong ("Pong")
APPL-1004	David Chaiken <i>et al.</i> , "Directory-Based Cache Coherence in Large-Scale Multiprocessors," <i>Computer</i> vol. 24, issue 9 (Jun 1990) ("Chaiken")
APPL-1005	Daniel Lenoski <i>et al.</i> , "The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor," <i>ISCA '90 Proceedings</i> of the 17th annual international symposium on Computer Ar- chitecture, pp. 148-159 (May 1990) ("Stanford DASH")
APPL-1006	U.S. Patent Number 6,490,661 to Keller et al ("Keller")
APPL-1007	Excerpts from Jose Duato <i>et al.</i> , INTERCONNECTION NETWORKS – AN ENGINEERING APPROACH (1997) ("Duato")
APPL-1008	Michael John Sebastian Smith, APPLICATION-SPECIFIC INTEGRATED CIRCUITS (1997) ("Smith")
APPL-1009	U.S. Patent No. 7,698,509 to Koster et al. ("Koster")
APPL-1010	U.S. Patent No. 7,315,919 to O'Krafka et al. ("O'Krafka")
APPL-1011	U.S. Patent No. 6,338,122 to Baumgartner <i>et al.</i> ("Baumgartner")



APPL-1012	Anant Agarwal et al., "An Evaluation of Directory Schemes for Cache Coherence," Conference Proceedings of 15th Annual International Symposium on Computer Architecture (1988)
APPL-1013	Louis G. Johnson, "Multiprocessors," ECEN 6253 Lecture Notes (April 28, 2003)
APPL-1014	Declaration of Dr. Robert Horst
APPL-1015	Excerpts from Merriam-Webster's Collegiate Dictionary - 10th Ed. (2001)
APPL-1016	Redacted Letter of March 28, 2014 from Memory Integrity's Counsel to Samsung's Counsel in <i>Memory Integrity LLC v. Samsung Electronics Co., Ltd. et al.</i> , Case No. 1:13-cv-01808-GMS, including "Response to Samsung's Allegation of a Rule 11 Violation"
APPL-1017	Luca Benini and Giovanni De Micheli, "Networks on chips: a new SoC paradigm," <i>Computer</i> vol. 35, issue 1 (Jan. 2002) ("Benini")
APPL-1018	"HyperTransport TM Technology I/O Link - A High-Bandwidth I/O Architecture" (Jul. 20, 2001) ("HyperTransport")
APPL-1019	U.S. Publication No. 2005/0228952 to Mayhew et al. ("Mayhew")
APPL-1020	U.S. Patent No. 6,662,277 to Gaither ("Gaither")



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