FARNEY DANIELS PC

Austin/Georgetown
Dallas
Silicon Valley

Jennifer Towle
800 S. Austin, Suite 200
Georgetown, TX 78626
512-582-2828

www farneydaniels.com

Minneapolis
Wilmington

March 28, 2014

VIA E-MAIL

Brian M. Berliner
O'Melveny & Myers LLP
400 South Hope Street
Los Angeles, CA 90071-2899

Re: *Memory Integrity LLC v. Samsung Electronics Co., Ltd. et al.*, Case No. 1:13-cv-01808-GMS

Dear Mr. Berliner:

I write in response to your letter dated March 14, 2014. In your letter, you claim: (1) that Memory Integrity does not have a sufficient basis under Federal Rule of Civil Procedure 11 for claiming that Samsung infringes U.S. Patent No. 7,296,121 (the "'121 Patent"), [redacted]

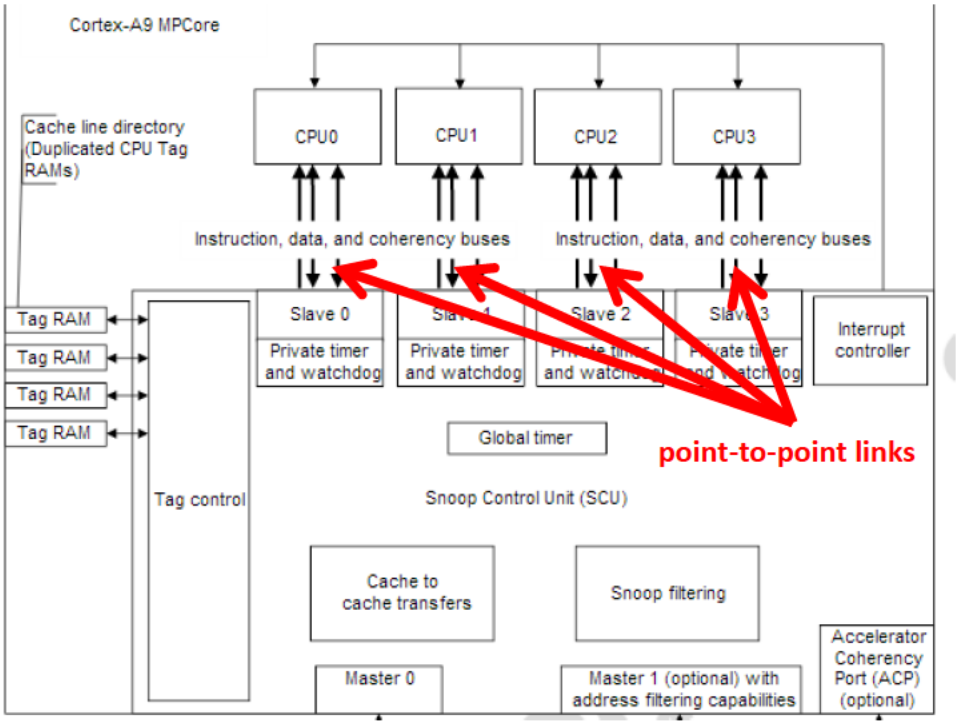
Response to Samsung's Allegation of a Rule 11 Violation:

In your letter you assert that none of the accused Samsung products listed in the Complaint contain a "point-to-point" architecture. You further assert that all CPU communications in these products pass through the Snoop Control Unit using a bus structure rather than a point-to-point architecture. On this basis, you allege that Memory Integrity failed to conduct an adequate pre-filing investigation.[1]

We respectfully disagree with your assertion that the Samsung products identified in the Complaint do not contain a point-to-point architecture and that Memory Integrity failed to conduct an adequate pre-filing investigation. As shown in Figure 1.1 of your letter (reproduced below), the Cortex-A9 contains separate links between each core (e.g., CPU0, CPU1, CPU2, and CPU3) and the Snoop Control Unit (SCU). Thus, the cores do not use a shared-bus architecture

[1] Your letter also states that the Galaxy Tab 7.0 product does not have a multicore processor. However, Samsung's own webpage for the Samsung Galaxy Tab 7.0 Plus indicates that at least that version of the product has a multi-core processor: http://www.samsung.com/global/microsite/galaxytab/7.0/spec.html?type=find.

but rather utilize separate links to the SCU. Indeed, this is consistent with what the '121 Patent shows in Figure 1B, which the Patent's specification describes as a point-to-point architecture that can use the techniques of the patented invention. *See* '121 Patent, Fig. 1B and 6:24-35. Further, the patent notes that the use of a switch as shown in Figure 1B is advantageous because it "allows implementation with fewer point-to-point links." *See id.* at 6:28-30.



See Figure 1.1 of the Cortex-A9 Reference Manual (annotations added in red).

Accordingly, your assertions that Samsung does not infringe the '121 Patent and that Memory Integrity failed to conduct an adequate pre-filing investigation are without merit.

[redacted]

[redacted]

Should you wish to discuss these matters further, please let me know.

Sincerely,

/s/ *Jennifer Towle*
Jennifer Towle