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(54) **ASYNCHRONOUS CACHE COHERENCE ARCHITECTURE IN A SHARED MEMORY MULTIPROCESSOR WITH POINT-TO-POINT LINKS**

(52) **U.S. Cl.** 711/119; 711/146; 711/144; 711/147

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(57) **ABSTRACT**

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In a shared memory, multiprocessor system, an asynchronous cache coherence method associates state information with each data block to indicate whether a copy of the data block is valid or invalid. When a processor in the multiprocessor system requests a data block, it issues the request to one or more other processors and the shared memory. Depending on the implementation, the request may be broadcast, or specifically targeted to processors having a copy of the requested data block. Each of the processors and memory that receive the request independently check to determine whether they have a valid copy of the requested data block based on the state information. Only the processor or memory having a valid copy of the requested data block responds to the request. The memory control path between each processor and a shared memory controller may be implemented with two unidirectional and dedicated point-to-point links for sending and receiving requests for blocks of data.

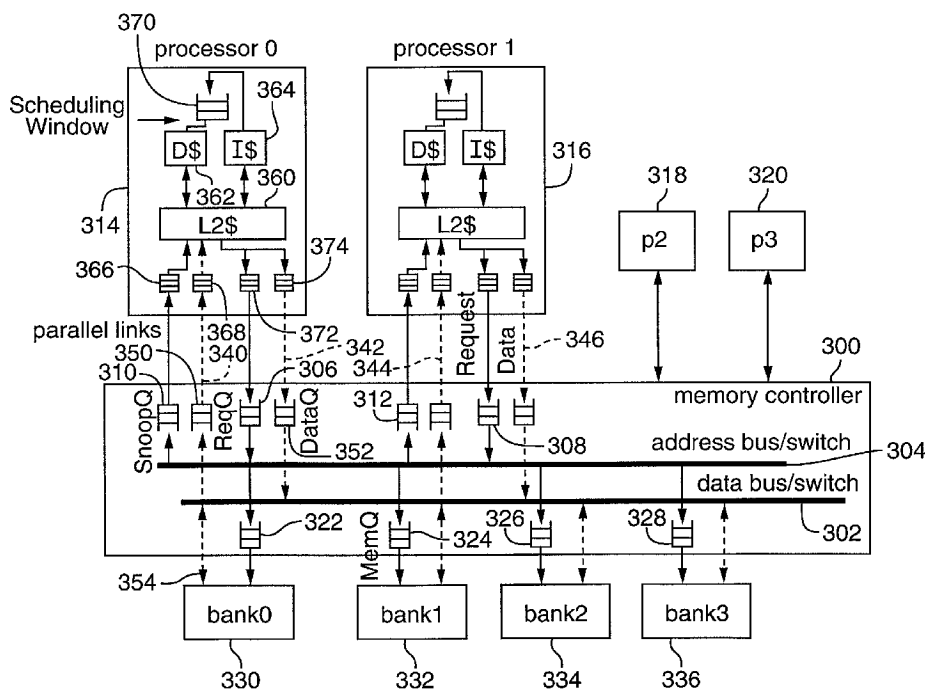
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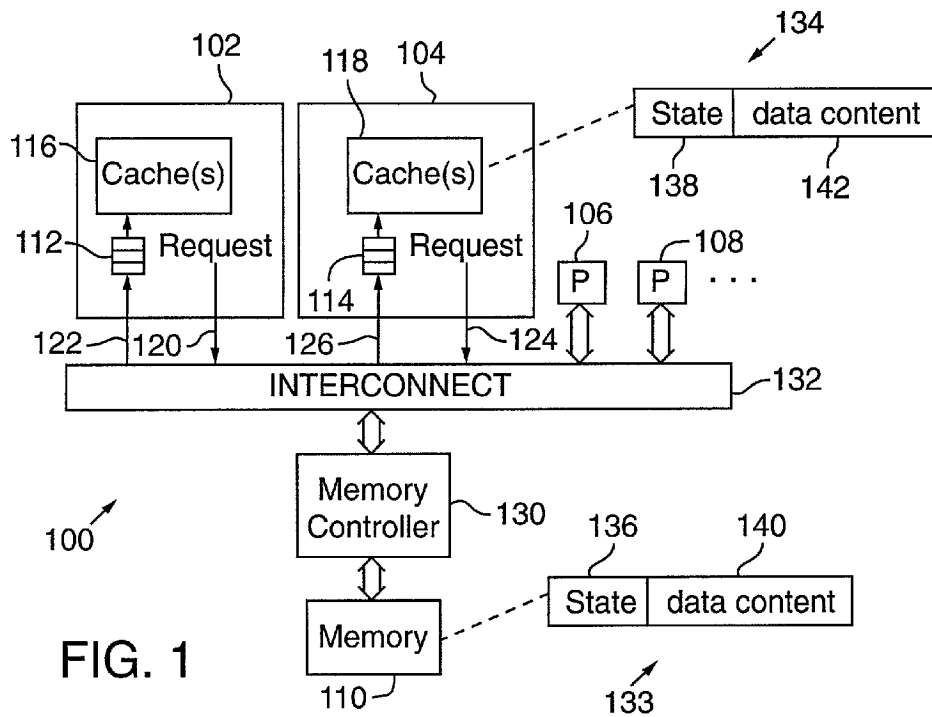
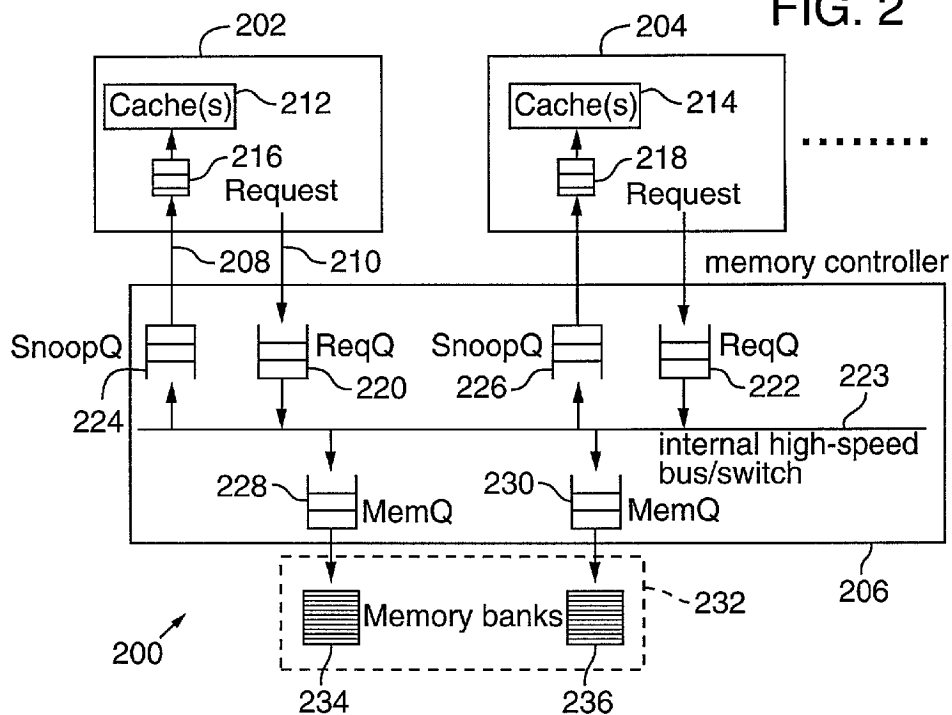
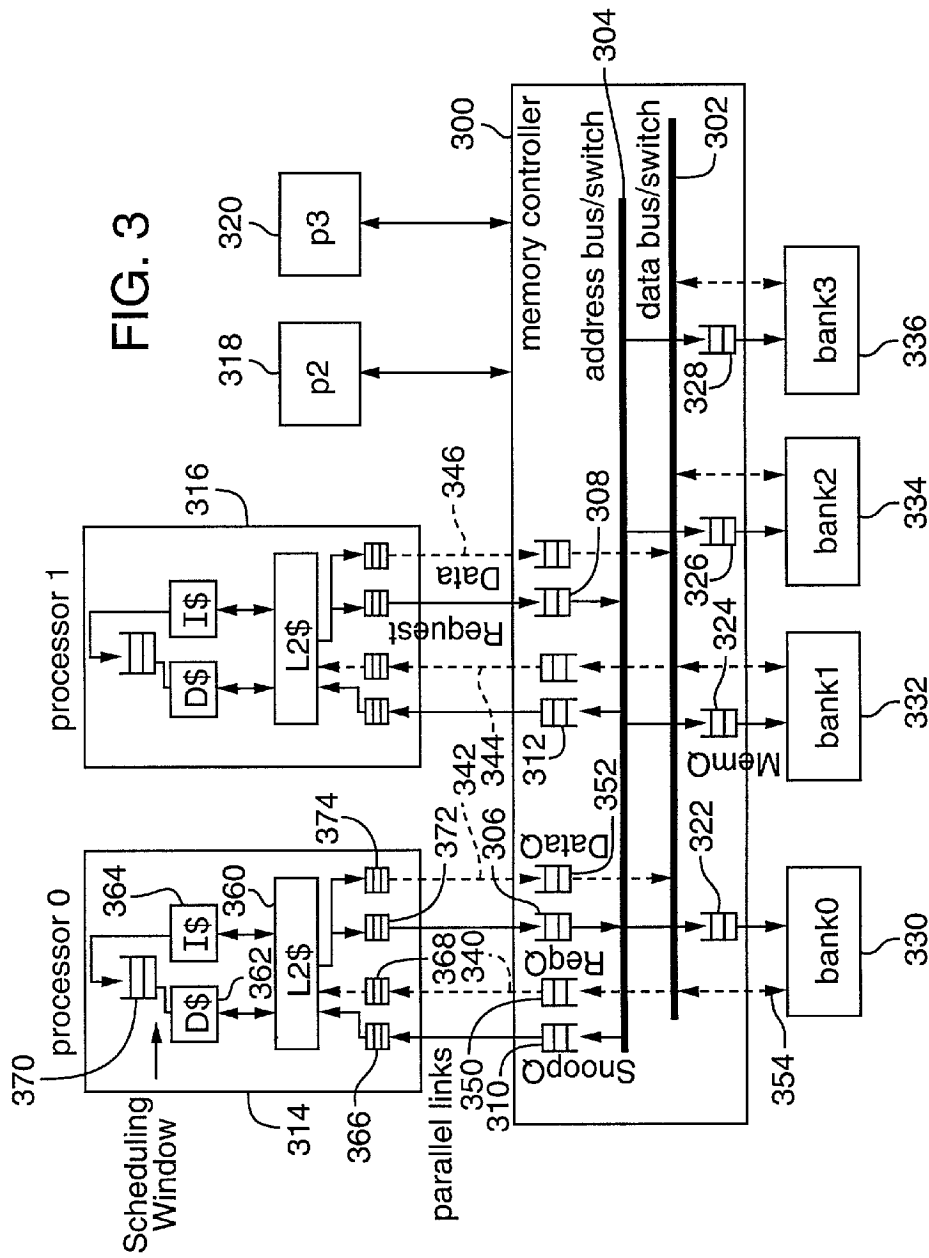


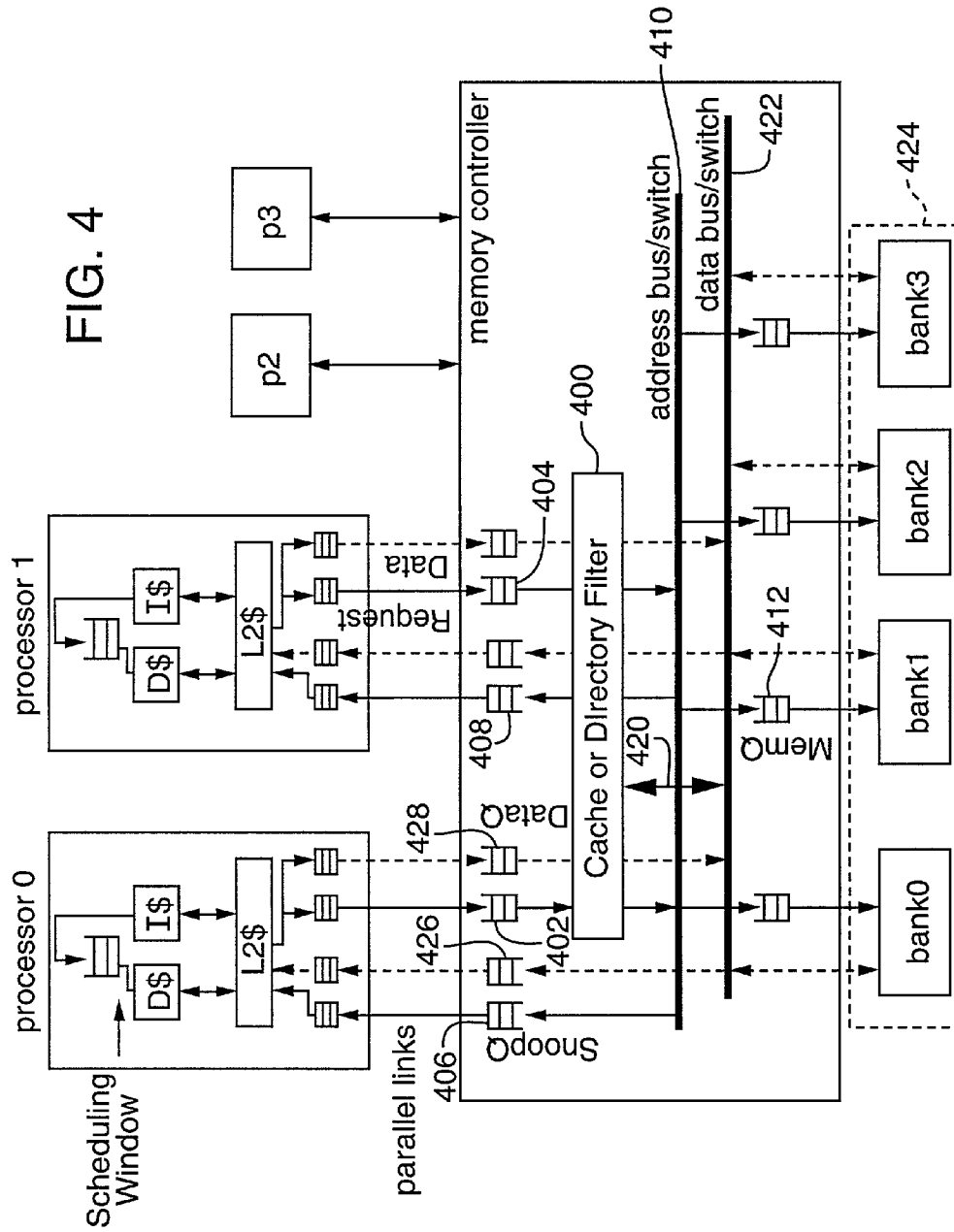
FIG. 1

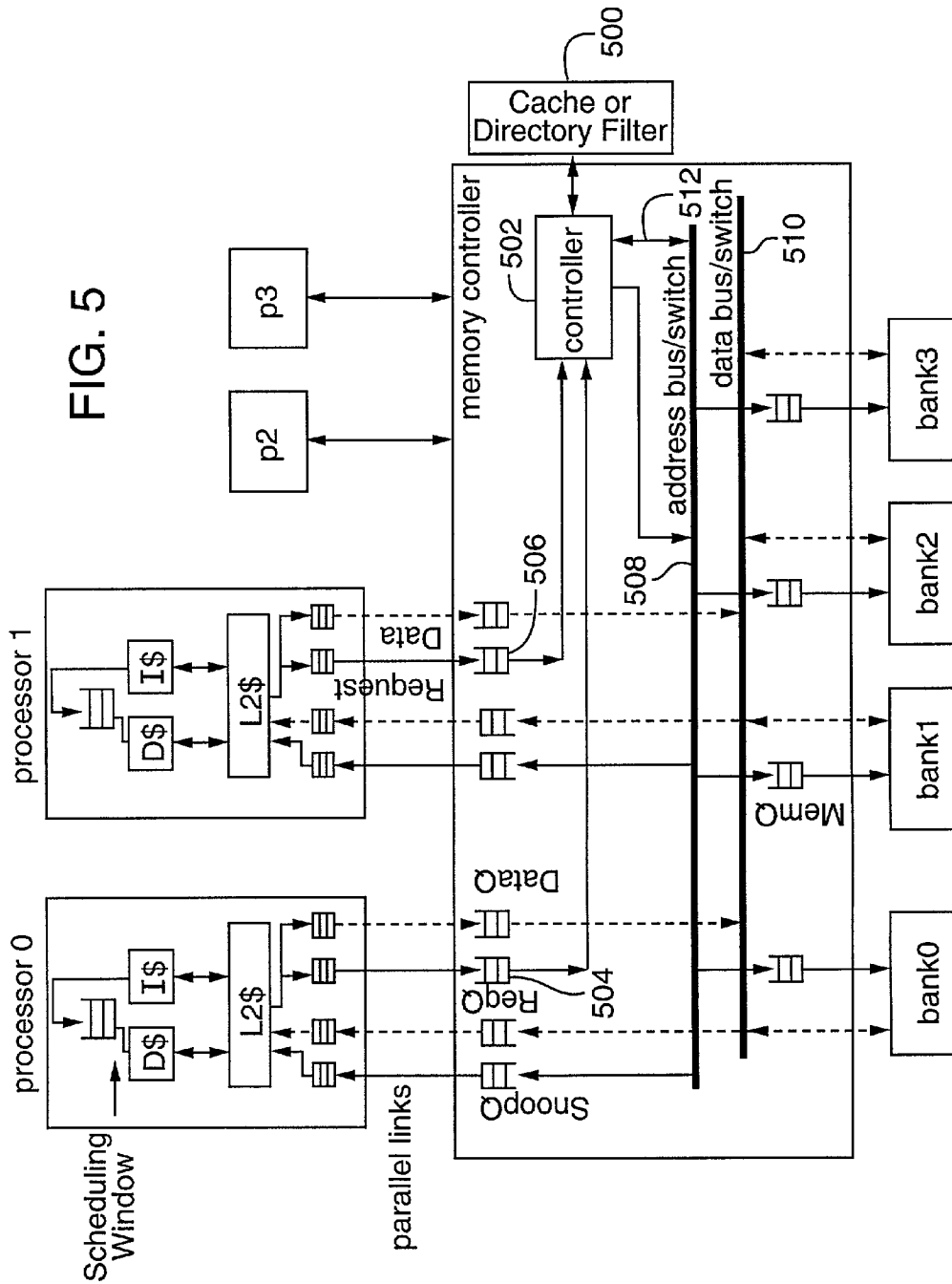
FIG. 2



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