Michael C. Brogioli, Ph.D.

CONTACT INFORMATION

Michael C. Brogioli, Ph.D.
Polymathic Consulting
100 Congress Avenue, Suite 2000
Austin, TX 78701 USA

Office: (512) 370-4936
Cell (preferred): (713) 732-0217
Fax: (512) 469-6306
E-mail: michael@polymathicconsulting.com

EDUCATION

Rice University, Houston, Texas USA

Ph.D., Electrical and Computer Engineering, 2007

- Dissertation Topic: "Reconfigurable Heterogeneous DSP/FPGA Based Embedded Architectures for Numerically Intensive Embedded Computing Workloads."
- Advising Committee: Dr. Joseph R. Cavallaro, Dr. Keith D. Cooper, Dr. Scott Rixner

Rice University, Houston, Texas USA

M.S., Electrical and Computer Engineering, 2003

- Dissertation Topic: "Dynamically Reconfigurable Data Caches in Low Power Computing."
- Advising Committee: Dr. Keith D. Cooper, Dr. Scott Rixner, Dr. Robert Jump

Rensselaer Polytechnic Institute, Troy, New York USA

B.S., Electrical Engineering, Cum Laude - 1999

- Advisor: Dr. William Pearlman

PROFESSIONAL EXPERIENCE

Polymathic Consulting, Austin, TX USA
Managing Director **October 2011-Present**
Founder and managing director at Polymathic Consulting, servicing clients ranging from early stage technology start up endeavors to Fortune 100 and beyond. Clients turn to Polymathic for expansive, proven engineering, research and development, intellectual property and technical leadership to effectively advance their real world business needs.

Scout Island Ventures, Austin, TX USA
Managing Director **October 2011 - Present**
Scout Island Ventures holds diversified investments in various stage startup companies, including but not limited to enterprises engaging in software, SaaS, PaaS, embedded computing, medical, mobile, and education.

Rice University, Houston, TX USA
Adjunct Professor, Electrical and Computer Engineering **July 2009 - Present**
Professor of Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware optimization in modern computing systems utilizing modern high level programming languages. Advisor of senior and graduate student based projects revolving around multi-core heterogeneous systems as they pertain to wireless telecommunications, medical and video.

Osmek, Austin, TX USA
Interim CTO, Advisory Board Member **March 2012 - February 2014**
Interim CTO and board member advising in the areas of large scale cloud based content management software systems. Providing innovative media content management for heterogeneous web enabled devices with geolocational services.

Freescale Semiconductor, Austin, TX USA

Chief Architect, Senior Member Technicial Staff **November 2009 - October 2011**
Technical architect of Freescale's DSP compilers and related technology. Responsible for management of technology, engineering roadmaps, design lead on compiler infrastructure and optimizations (high level and low level), next generation ABI definitions and next generation architecture solutions. Technical lead on multi-year engagement with processor architects in design of next generation DSP cores. Developed software infrastructure for migrating OEM competitor software stacks to Freescale solutions, tools generation, software packages, migration strategies and white papers. Technical lead on Tier-1 OEM customer relationships, evaluations of 3rd party technologies for potential partnerships and acquisitions, lead various university research collaborations on behalf of Freescale. Development and deployment of internal software engineering policies and practices.

Freescale Semiconductor, Austin, TX USA
Senior Compiler Engineer V
High Performance Compiler Design, Processor Architecture **2008 - 2009**
Team leader on compiler engineering effort to provide intuitive, interactive end user experience for DSP compiler tool suite. Designed a framework to guide users in achieving highly optimized compiled VLIW code. Assembly listing reports for optimization failure advice, porting advice when migrating from competitor architectures, advice on code modifications for optimization enablement. Lead designer, engineering effort director, project planning and scoping, release schedule, and drafting of specification. Development of various compiler optimizations for VLIW processing as well as software emulation layers for running competitor software solutions on Freescale silicon.

Advising of next-gen DSP core architecture team in creating a highly orthogonal, compiler targetable multi-clustered VLIW based digital signal processor architecture. Work with future basestation architecture teams on designing next-gen basestation architecture for 4G LTE incorporating control and data plane processing with appropriate programming models.

Method Seven, Boston, MA USA
Technical Co-Founder
High Performance Software and Hardware Systems Architecture **June 2006 - August 2007**
Founded Method Seven, a financial engineering company applying biologically inspired machine learning to financial market analysis. Principal software systems architect and hardware systems architect for both research and deployment platforms. Lead research and development of platform for scans and overlays covering the NASDAQ, NYSE, and AMEX markets using proprietary technologies.

Texas Instruments, Stafford, Texas USA
Advanced Architecture and Chip Technologies
DSP Architecture (Intern) **Jun, 2005 - Sept 2005**
System modelling and architectural exploration of Davinci^{TM}system-on-chip (SOC) architecture designed for embedded video processing. SystemC based simulation models of on–chip crossbars, bus arbitration and bridge technology, as well as on–chip and off–chip memory controllers within application specific heterogeneous SOC architectures.

Fulbright and Jaworski LLP, Houston, Texas USA
Intellectual Properties
Intellectual Property Consultant **January 2005 - August 2007**
Intellectual property consultant and technology advisor on litigation and prosecution work including, but not limited to: CDMA2000 3G wireless standards, wireless communications systems, embedded computing, and large scale modular software systems. Reverse engineering of source code varying from VHDL to high level object oriented applications, as well at patent prosecution and litigation work.

Intel Corporation, Santa Clara, California USA

Microprocessor Research Labs
Compiler Engineering (Intern) **May, 2000 - Aug, 2000**
Implemented speculative multi–threading support in Intel's IA–64 compiler. Developed new program analysis and back end code generation phases to support speculatively launching threads at runtime. Analyzed the performance potentials of SPEC95 benchmarks with respect to speculatively multi–threaded execution.

Vicarious Visions, Albany, New York USA
Lead Software Engineer (Intern) **April, 1999 - Aug, 1999**
Principal engineer on Activision's "AMF Extreme Bowling" for Nintendo's Color Gameboy gaming console. Developed PC based audio and graphics development tools suite for use with Color Gameboy game production. Coded innovative, highly optimized assembly routines for real time speech and full motion video on the console's limited Zilog Z80 processor resources.

Stratus Computer, Marlboro, Massachusetts USA **May, 1998 - Aug, 1998**
Hardware Engineering (Intern) **June, 1997 - Dec, 1997**
Debugged locked step CPU operation and memory management issues in Stratus' fault tolerant UNIX release 3.4. Qualified Hewlett Packard PA–8000 series CPU modules under Stratus' proprietary OS release, VOS 14.0, during alpha and beta test phases. Wrote C code and UNIX shell scripts for recreating documented system failures, and to automate remote kernel updates and OS installs as well as data logging.

Rensselaer Polytechnic Institute, Troy, New York USA
Digital Microelectronics Design (Undergraduate Instructor) **1997 - 1998**
Undergraduate instructor of undergraduate courses in digital microelectronics and circuit design. Instructed weekly lessons, computer design labs, graded exams and problem sets.

Rensselaer Polytechnic Institute, Troy, New York USA
Rensselaer Electric Motorsports (Undergraduate Hardware and Software Engineer) **1995 - 1997**
Hardware and software design of embedded operating system and hardware platform for electrical vehicle prototypes, running on 16-bit Motorola 68K dual processor platform. Power enginering test platform for dynamometers. Project was sponsored by General Motors and Honda.

Books and Contributed Chapters

Brogioli, M. C., *On Cloud Computing, Data Security, and Medical Devices*, Software Development for Networking Applications – Expert Guides Series, pp. TBD, Elsevier Publishing, Atlanta, GA, 2016 (print).

Brogioli, M. C., *A Brief History of Wireless Telecommunications Networks*, Software Development for Networking Applications – Expert Guides Series, pp. TBD, Elsevier Publishing, Atlanta, GA, 2016 (print).

Brogioli, M. C., *Networking Protocols, OSI 7 Layer Model In Networking and Communications Protocols for Data, Voice, and Beyond.*, Software Development for Networking Applications – Expert Guides Series, pp. TBD, Elsevier Publishing, Atlanta, GA, 2016 (print).

Brogioli, M. C., *Case Study: Mobile Computing, Cloud Computing, and Data Security*, Software Development for Networking Applications – Expert Guides Series, pp. TBD, Elsevier Publishing, Atlanta, GA, 2016 (print).

Wu, Michael and Sun, Yang and Wang, Guohui and Brogioli, M.C. and Cavallaro, J. R., *Implementation of a High Throughput 3GPP Turbo Decoder on GPU Architectures*, Software Development for Networking Applications – Expert Guides Series, pp. TBD, Elsevier Publishing, Atlanta, GA, 2016 (print).

Brogioli, M. C., *On The C++ Programming Language for Embedded Software, Systems, and Platforms*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Brogioli, M. C., *Software Optimizations for Memory Performance in Embedded Systems*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Invited Co-Author, *Signal Processing Systems Handbook, Second Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2012.

Brogioli, M. C., *Software Programmable DSP Architectures*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 63-75, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *The DSP Hardware / Software Continuum*, Expert Guide DSP for Embedded and Real-Time Systems,, pp. 103-113, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *DSP Optimization - Memory Optimization*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 217-241, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C. and Dew, Stephen, *Optimizing DSP Software - High level Languages and Programming Models*, Expert Guide DSP for Embedded and Real-Time Systems,, pp. 167-179, Elsevier Publishing, Atlanta, GA, 2012.

Sun, Yang, Amiri, Kiarash, Brogioli, Michael, Wang, Guohui, and Cavallaro, Joseph R., *DSP Hardware Accelerator Architectures for Communication Applications*, Springer Publishing, New York, NY, Spring 2012.

Invited Co-Author, *Signal Processing Systems Handbook, First Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2010.

PUBLICATIONS

Invited Paper, Arokia I, Brogioli, Michael, Jain, Nitjin and Garg, Umang, *LTE Layer 1 Software Design on Heterogeneous Multicore DSP Platforms*, IEEE 45th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2011.

Kyriakopoulous, Konstantinos, Brogioli, Michael C., and Zhang, Ruihao, *Improving Software Systems Quality through Well Defined Development Methodologies*, 2011 Test Methodology and Efficiency Symposium, Freescale Semiconductor, Austin, TX, USA, 2011.

Brogioli, M.C., and Cavallaro, J.R., *Compiler Driven Architecture Design Space Exploration for Embedded DSP Workloads: A Study in Software Programmability Versus Hardware Acceleration*, IEEE 43rd Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2009.

Brogioli, M.C., and Zhang, Ruihao, *Compiler Feedback: Guiding Performance of Compiled C Code*, Freescale Semiconductor White Paper, Austin, TX, 2009.

Brogioli, M.C., and Cavallaro, J., *RISD: A Retargetable Compiler Infrastructure for Scalable Multi-Clustered VLIW DSP Architectures*, IEEE 5th Dallas Circuits and Systems Workshop, Dallas, TX, 2007.

Brogioli, M.C., Radosavljevic, P., and Cavallaro, J., *A General Hardware/Software Codesign Methodology for Embedded Signal Processing and Multimedia Workloads*, IEEE 40th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2006.

Brogioli, M.C., Radosavljevic, P., and Cavallaro, J., *Hardware/Software Co-design Methodology for*

DSP/FPGA Partitioning: A Case Study for Meeting Real-Time Processing Deadlines in 3.5G Mobile Receivers, 49th IEEE International Midwest Symposium on Circuits and Systems, San Juan, Puerto Rico, 2006.

Brogioli, M.C., Willmann, P.D., and Rixner, S., *Parallelization Strategies for Network Interface Firmware*, IEEE/ACM 4th Annual Workshop on Optimizations for DSP and Embedded Systems (In Conjunction with IEEE/ACM International Symposium on Code Generation and Optimization), Manhattan, NY, 2006.

Brogioli, M.C., Gadhiok, M., and Cavallaro, J., *Design and Analysis of Heterogeneous DSP/FPGA Based Architectures for 3GPP Wireless Systems*, IEEE Real-Time and Embedded Technology and Applications Symposium Work-in-Progress Sessions, San Jose, CA, 2006.

Brogioli, M.C., and Cavallaro, J., *Modelling Heterogeneous DSP-FPGA Based System Partitioning with Extensions to the Spinach Simulation Environment*, IEEE 39th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2005.

Brogioli, M.C., Pai, V.S., Willmann, P.D., *Spinach: A Liberty–Based Simulator For Programmable Network Interface Architectures*, ACM SIGPLAN/SIGBED Conference on Languages Compilers and Tools for Embedded Systems, San Diego, CA, 2004.

Brogioli, M.C., *Dynamically Reconfigurable Data Caches in Low Power Computing*, Masters Thesis, Rice University, Houston Texas, 2002.

Patents

Michael C. Brogioli, Ph.D., Cesar Taylor M.D., and Howard Roberts, *Location Agnostic Platform for Medical Condition Monitoring and Prediction and Method of Use Thereof*, Patent No: 147145.010100/US, 2014.

Cesar Taylor M.D., and Michael C. Brogioli Ph.D., and Howard Roberts, *System for Holistic Pain Monitoring and Prediction and Method of User Thereof*, Patent No: 147145.010200/US, 2014.

Cesar Taylor M.D., and Michael C. Brogioli Ph.D., and Howard Roberts, *System for Prevention of Narcotic Diversion and Method of Use Thereof*, Patent No: 147145.010300/US, 2014.

Howard Roberts, Cesar Taylor M.D., and Michael C. Brogioli Ph.D., *Magnetometer Breathing Sensor and Method of User Thereof*, Patent No: 147145.010400/US, 2014.

Corporate Board Membership

Southwest Angel Network for Social Impact, TX USA
Board of Directors, Co-Founder **October 2015 - Present**
The Southwest Angel Network for Social Impact (SWAN Impact) is a community of like-minded investors who enjoy working together to *Make the world a better place, one company at a time.* We believe that we can have the most significant impact by funding for-profit start-up companies who are building sustainable businesses.

NewCrew, TX USA
Advisory Board **April 2015 - Present**
Board member advising in the areas of mobile computing, social computing, and geofencing technologies. Business development, marketing, and fund raising.

Joule Enableware, TX USA
Advisory Board, Co-Founder **April 2015 - Present**
Board member advising in the areas of Internet of Things technologies, specifically related to product developer solutions, programming languages and platforms. Business development, marketing, and

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.