



US006662277B2

(12) **United States Patent**
Gaither

(10) **Patent No.:** **US 6,662,277 B2**
(45) **Date of Patent:** **Dec. 9, 2003**

(54) **CACHE SYSTEM WITH GROUPS OF LINES AND WITH COHERENCY FOR BOTH SINGLE LINES AND GROUPS OF LINES**

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- (73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/919,309**

(22) Filed: **Jul. 31, 2001**

(65) **Prior Publication Data**

US 2003/0028730 A1 Feb. 6, 2003

- (51) **Int. Cl.⁷** **G06F 12/00**
- (52) **U.S. Cl.** **711/145; 711/141; 711/144; 711/146; 711/147; 711/148**
- (58) **Field of Search** **711/141, 145, 711/146, 147, 148**

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Primary Examiner—Donald Sparks

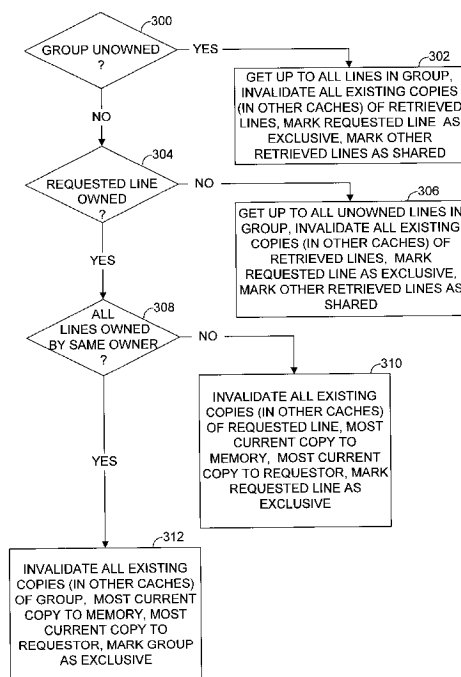
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(57) **ABSTRACT**

In a computer system with caching, memory transactions can retrieve and store groups of lines. Coherency states are maintained for groups of lines, and for individual lines. A single coherency transaction, and a single address transaction, can then result in the transfer of multiple lines of data, reducing overall latency. Even though lines may be transferred as a group, the lines can subsequently be treated separately. This avoids many of the problems caused by long lines, such as increased cache-to-cache copy activity. In one alternative, when a cache memory requests a group of lines, and when the group of lines is partially owned by another cache memory, then the requesting cache receives fewer than all the lines in the requested group.

9 Claims, 5 Drawing Sheets



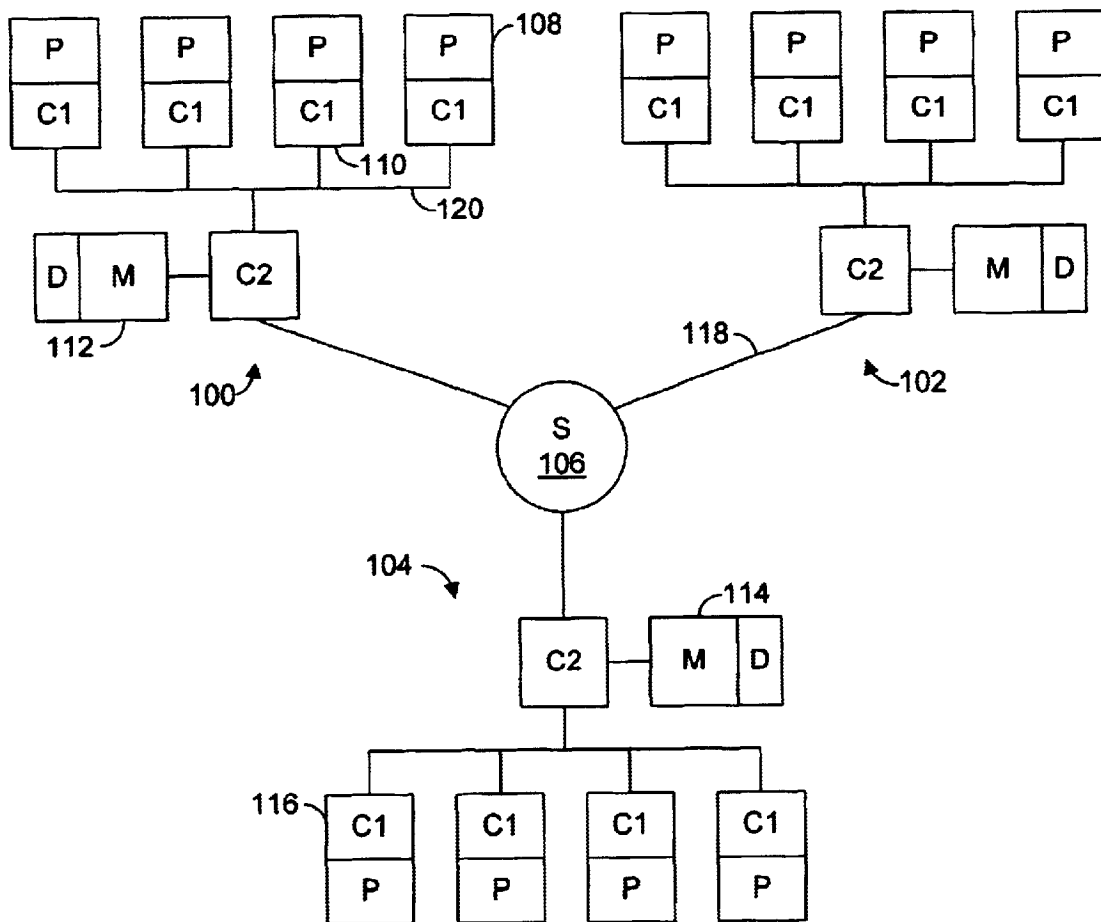


FIG. 1

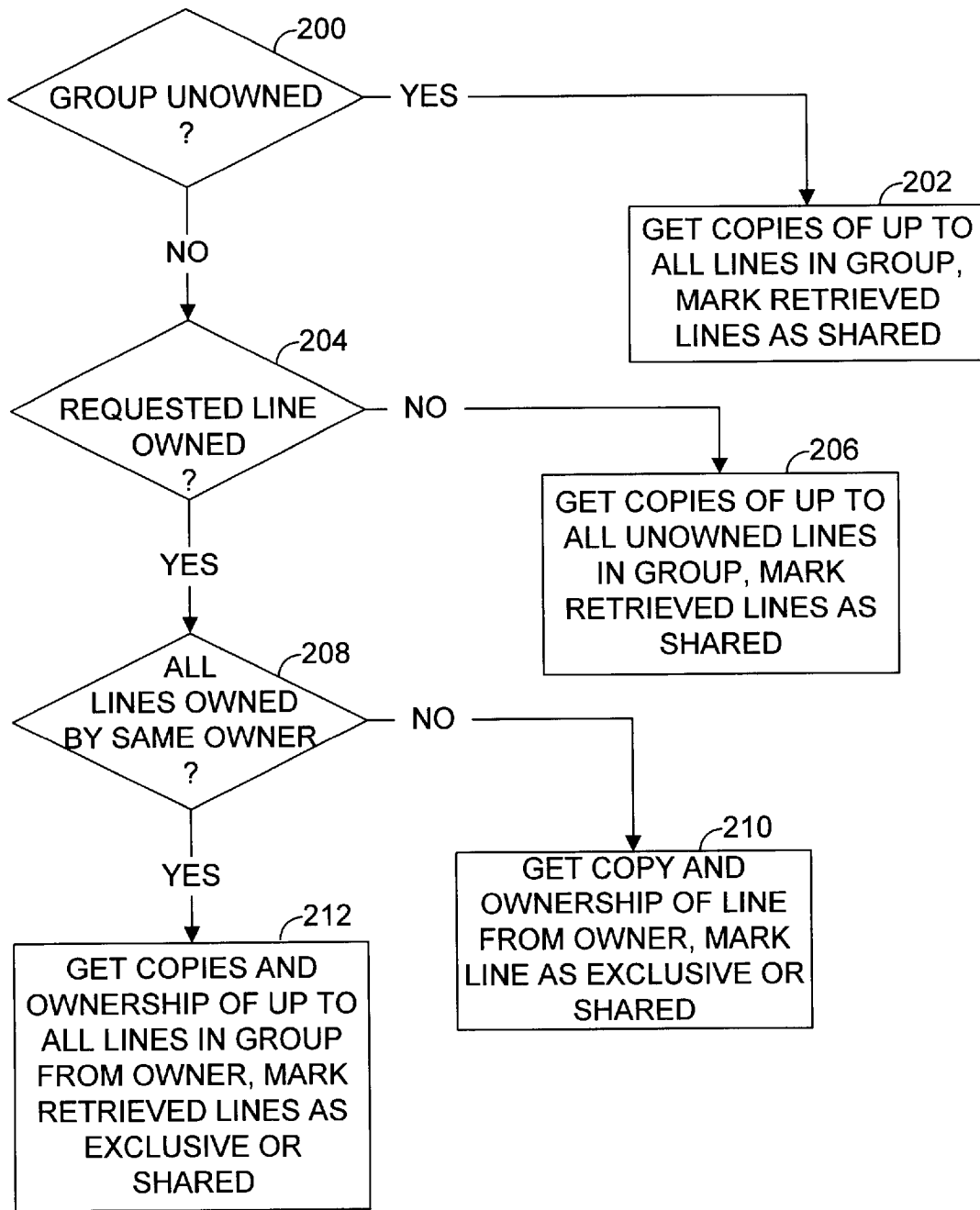


FIG. 2

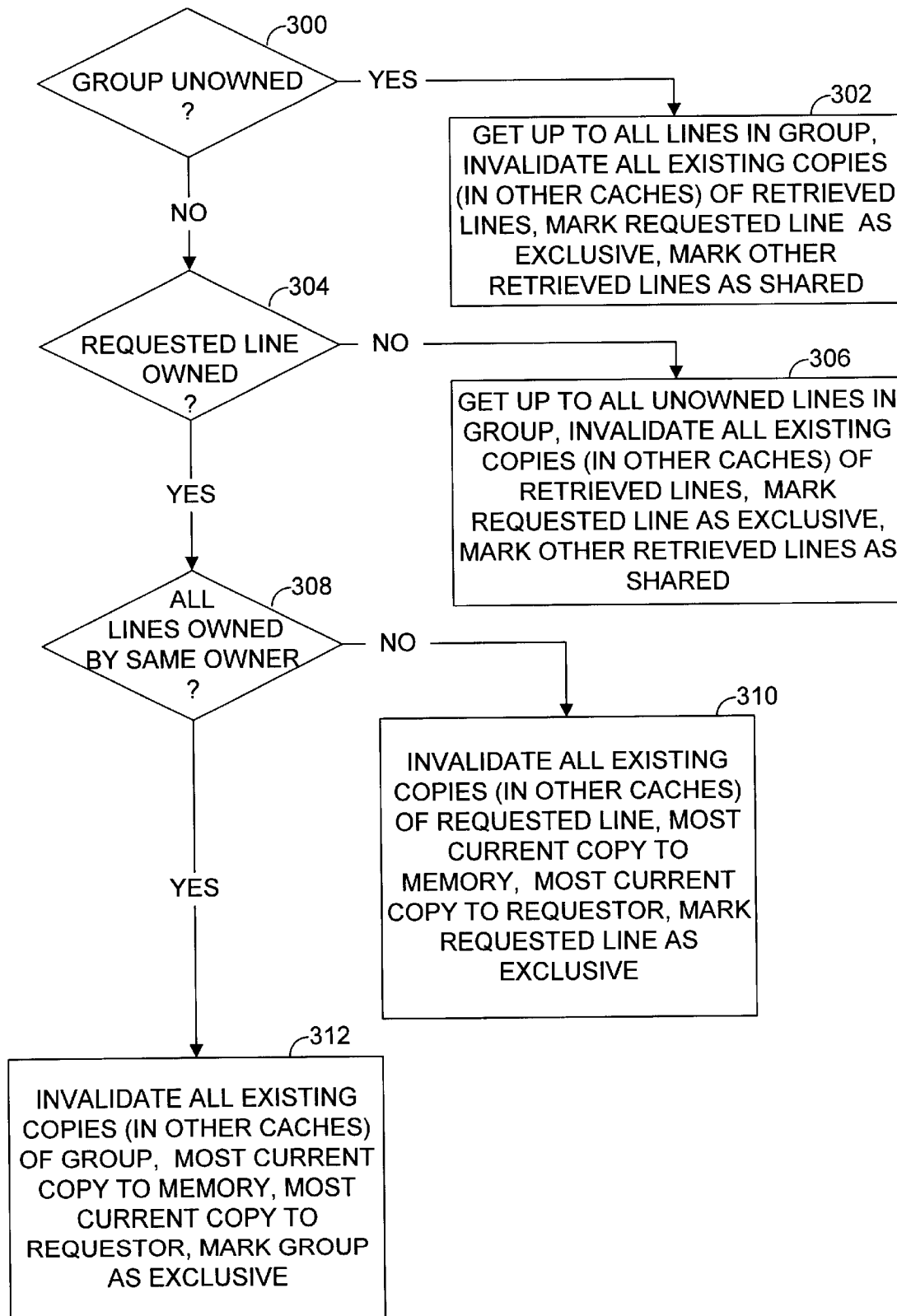


FIG. 3

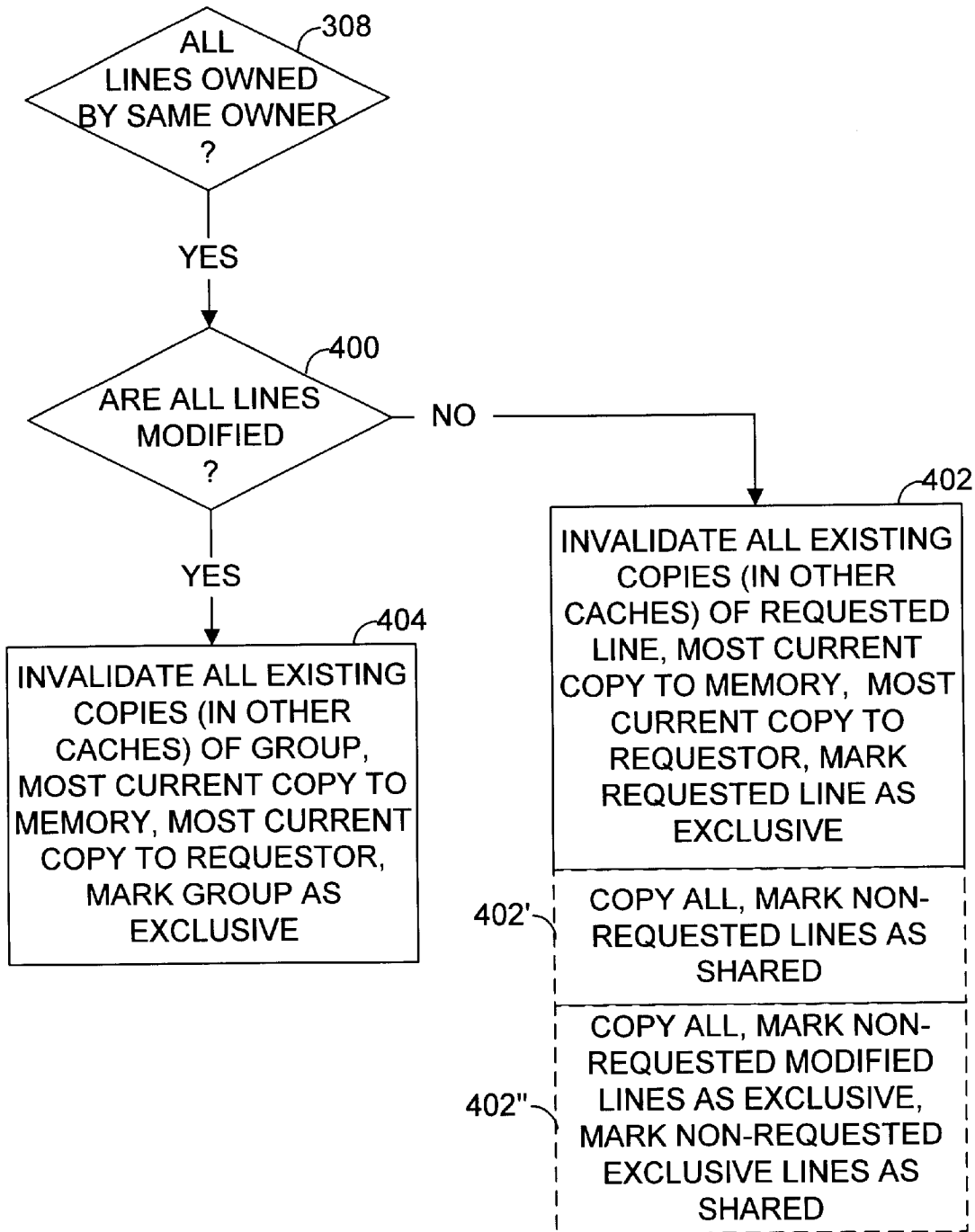


FIG. 4

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