The 3-D lattice formulation is a logical extension of the 2-D Burg algorithm and, analogously, a set of 3-D reflection coefficients $\{\rho(n,m,u)\}$ can be derived. Again, the reflection coefficients are calculated directly from the input data samples. This method is basically a 3-D AR model fitting algorithm.

This algorithm is essentially a 3-D Burg algorithm which given an optimal MMSE estimate for stationary processes when the image extent is much greater than the extent of the filter $H_{N,M,U}(z_1,z_2,z_3)$. Signal flow diagrams for the 3-D FIR and IIR prediction filters are similar to 2-D lattice filters with additional delay elements.

D. Results

The most significant results to arising out of these investigations can be summarized as follows:

1) Reflection Coefficients - Calculated by the harmonic mean method are extremely good means of characterizing 2-D imagery data in a MMSE sense. As demonstrated experimentally herein, very low residual errors remain after only a few stages of lattice filtering.

2) Experimentally Verified - That the 2-D Burg algorithm as implemented here with appropriate support can be used for imagery compression purposes in the spatial domain. Heretofore, no 2-D LPC imagery coding of this nature had been investigated. This paper described a valuable new spatial compression technique. It is suitable for real-time applications yielding impressive (50-90 percent) image compression factors with, in most cases, imperceptible image fidelity deterioration. When 2-D LPC-induced distortion occurs, it can be removed by simple image enhancement type filtering techniques.[8]

3) A New 2-D In-Place Method - For real-time computation of the 2-D lattice filter coefficients and subsequent imagery data filtering has been derived and verified experimentally with actual imagery data. This method provides intermediate results at any filter stage and is amenable to multidimensional MMSE digital filtering in excess of 2-D. This new method of in-place lattice forward and reverse filtering was utilized for display of intermediate imagery results display after each stage of the 2-D LPC process. With this algorithm, it is possible to form 'imagery' composed from only selected stages of residuals. In other words, imagery from which selected nearest-neighbor pixel correlations have been removed can be generated. This methodology is, in effect, capable of selective decoupling, in a MMSE sense, multivariate function variables. This behavior is afforded by to the Gram-Schmidt orthogonalization realized by the lattice filter structure itself.

4) Extension of 2-D LPC Techniques - To 3-D demonstrating that with the appropriate ordering of multidimensional digital signal points into 'past' and 'future', the resulting LPC filters retain the same stability and analytical properties attributed to 2-D and experimentally demonstrated herein. These 2-D lattice filter designs can readily be extended to N dimensions, as well as to n stages in each dimension. The prediction error results for each dimension can be independently obtained and the final prediction value calculated as a root-sum-square composite. This methodology can be utilized effectively to realize a multivariate function analysis MMSE prediction capability.

As a result of these investigations, several areas remain prime candidates for further work. These areas include:

1) 2-D Filter Stability - To include additional algorithms for both forward and backward prediction.

2) New and Automated 2-D Filter Design Methods - Investigations of the performance of reflection coefficient determination algorithms in addition to the 2-D Burg algorithm harmonic-mean method.

3) Determination of a Quantitative Fidelity Criterion - More representative of imagery utility.

4) Development of Precise Methods - Imagery testing, evaluation, and performance verification.

5) Utilization of Evolving State-of-the-Art Hardware - Laser disks, VHSIC/VLSI integration, memories, CPU interfaces, etc.

6) Practical Extension of these LPC Methods-correlation, experimental behavior, and adaptive prediction in a MMSE sense. This 2-D formalism is also suitable for analysis of other 2-D or multi-dimensional stochastic processes.

7) Comparison with the Discrete Cosine Transform (DCT) - 2-D data compression applications via a suitable quantitative measure.

The above candidate research areas all constitute promising topics for future work. The full benefit of MMSE LPC analysis is applicable to other than just the multidimensional digital data compression problem.

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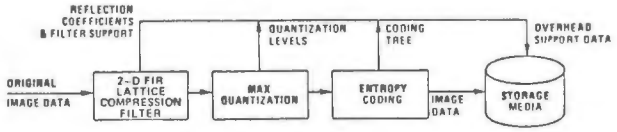
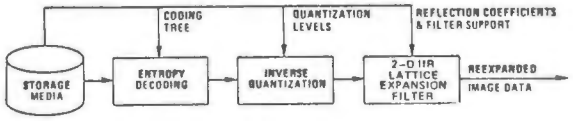
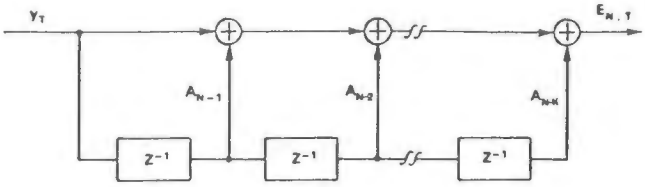


a) Forward Image Compression Process

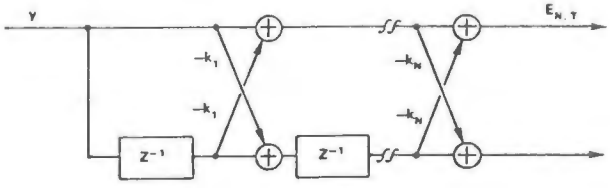


b) Reverse Image Expansion Process

Figure 1

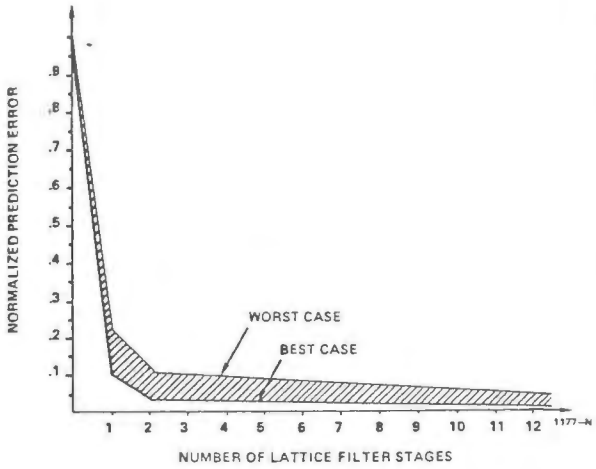


a) Direct Realization of FIR Least Squares Error Filter (A_N = Filter Coefficients)



b) Lattice Implementation of a FIR Least Squares Error Filter ($-k_i$ = Reflection Coefficients)

Figure 2



Normalized Prediction Error vs. Number of Lattice Filter Stages

Figure 3

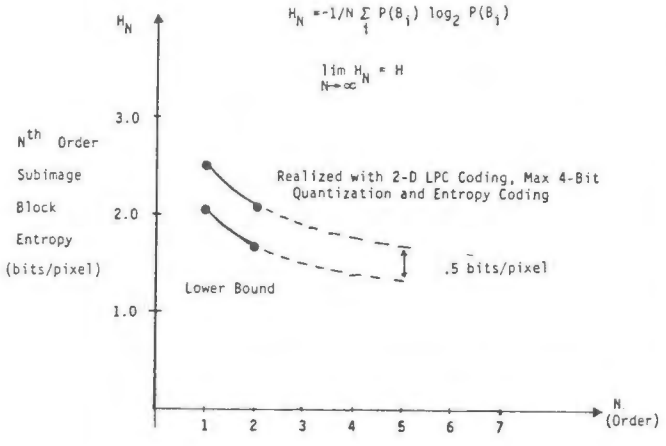


Image Compression Efficiency Achieved

Figure 4

A TERRAIN DATA/DIGITAL MAP SYSTEM FOR LHX

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Abstract

The Light Helicopter (LHX) is a new aerial platform designed to perform vertical lift missions for Army aviation in the air/land battle of 1995 and beyond. This paper briefly describes the avionics functions required to support LHX missions, including mission management and digital map data retrieval. Presented are some preliminary ideas on terrain data system functions and a discussion of how implementing these functions in the LHX integrated architecture would impact the overall avionics suite.

Overview

The Air/Land Battle 2000 concept employs Army aviation in whole or in part in all mission areas and battlefield tasks. Army aviation must rapidly deploy and engage enemy forces; conduct reconnaissance and airmobile and logistic operations; and provide C^3I, airborne fire direction, intelligence and electronic warfare operations, and battlefield interdiction. The threat is real, both quantitatively and qualitatively. In facing this projected enemy threat the Army Aviation Mission Area (AAMA) analysis identified many deficiencies in their current aircraft fleet, including aging and obsolescent aircraft that cannot be upgraded satisfactorily to meet tactical challenges. The Light Helicopter (LHX) family is envisioned as the Army aircraft that will overcome this. It is a new aerial platform designed to perform vertical lift missions for Army aviation in the air/land battle of 1995 and beyond. Depending on mission requirements and cost-effectiveness analyses, it may or may not be a multiple-version aircraft. If more than one version (e.g., scout attack and utility/observation) evolves, all versions will employ many common subsystems such as engines, rotors, drive trains, and core avionics.

Avionic processing equipment has been traditionally designed for specific subsystems in which it was intended to operate. This approach has led to different architectures, hardware, and software support within the same system. Providing a low-cost, sustainable, mission-effective avionics system requires fault-tolerant, modular processing architecture and processing modules. Essential in this development is the timely and cost-effective insertion of very-high-speed integrated circuit (VHSIC) technology. With full-scale engineering development of LHX scheduled for FY86, it is imperative to initiate development of a VHSIC-based avionics architecture to ensure feasibility of an avionics system capable of meeting the processing requirements dictated by the missions and functions of LHX and to avoid early obsolescence or costly retrofitting.

One of the functions to be implemented into the LHX avionics is a terrain data system capable of working in conjunction with the navigation system to provide accurate terrain correlation navigation updates as well as various displays critical to low-level NOE flights.

LHX System

Table 1 lists the avionics functions required to support LHX missions. The LHX processing architecture has been defined to provide the signal and data processing necessary to implement these functional subsystems. The processing which they require, coupled with stringent physical constraints of an advanced rotorcraft, dictate an integrated architecture approach that crosses functional boundaries to permit the sharing of processing resources. The processing architecture implements the sensor fusion algorithms that combine the data of multiple subsystems to create a highly synergistic system; however, the control structure also

TABLE 1. LHX PROCESSING REQUIREMENTS

Function	Preprocessing (MOPS)	Array Processing (MOPS)	Data Processing (MIPS)	Program Memory (KWDS)	Data Memory (MBITS)
Target acquisition	978	125	20	150	33
Fire control	—	—	0.75	139	1.5
Aircraft survivability equipment	70	2	5	40	0.2
Terrain data	—	343	7.5	120	81
Navigation	—	10	9	96	4
Communication	—	138	3.5	127	4
Mission management	—	0	24	148	27
Flight control (3)	—	0	2.3	48	—
Total	1,048	618	72	868	151

allows autonomous operation of the subsystems while maintaining deterministic processing time lines.

Table 1 also presents estimates of the required program memory, data memory, and processing. Three types of processing are required: complex vector, real array, and scalar. Five processing modules have been defined: complex vector processing module, array processing module, data processing module, memory module, and mission computer executive module.

LHX Mission Management Subsystem

The objective of the mission management subsystem is to integrate and coordinate all activities within the overall system. These components, Figure 1, include a central manager, data base manager, display manager, and subsystem manager for each subsystem. It should be understood that the functions of the central manager, data base manager, and display manager are distributed among the various subsystems.

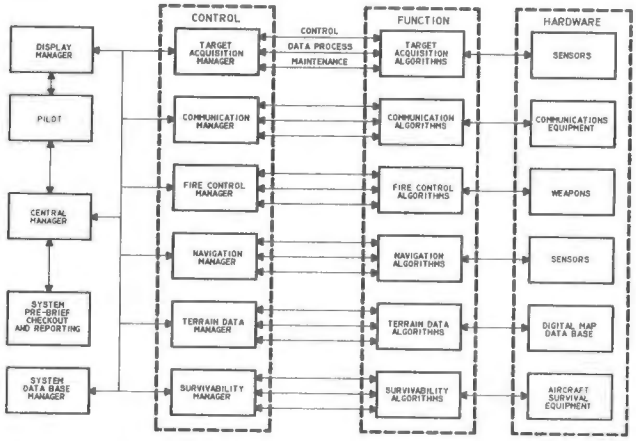

Figure 1. Mission Management Functions

The central manager manages the various high-level functions of the system, e.g., those that are common to all subsystems or those that either involve more than one subsystem or take more than a few seconds to perform or require interaction with the pilot. The central manager must maintain models of the system's configuration, the overall mission, and the status of the various aircraft systems. These models primarily provide the pilot with a summary and tentative evaluation of the current situation. The central manager interacts with the pilot to refine its internal models and to plan appropriate activities (route planning, tactic selection, weapon handoff, etc.). It also interacts with the subsystem managers to optimize resource allocation, execute pilot requests or planned activities, and coordinate sensor assignments. At the same time, the central manager must monitor the status of the various subsystems, perform inflight testing/reconfiguration, log all mission activities, and handle routine situations. It is the central manager's duty to process pilot inputs (voice commands, keyboard entries, etc.) appropriately and to integrate the output of subsystem data (video displays and speech output). When doing this, the central manager tries to predict the pilot's current information needs and to provide suitable default inputs. Often, when several tasks are to be performed, the central manager prioritizes and sequences them, including any set-up, follow-up, or subtasks. This is particularly important when some of the tasks must be performed by the pilot.

The data base manager maintains a shared central data base. The subsystems initiate requests for the storage or retrieval of certain data. The data base manager then transforms all references to actual memory addresses and performs the necessary data base functions. Since there will be various types of memory storage in the system (perhaps with different access times, word lengths, error correction or detection capability, EMP protection, power backup, etc.), the data base manager decides before and during the mission where and how data shall be stored to optimally meet mission requirements. It also performs any automatic or periodic data functions on its own.

The display manager meets the changing information needs of the pilot. As different subsystems produce information to be displayed, the display manager must decide the best way to make this information available to the pilot, taking into consideration the data's priority. Choices include merging the new data with the data currently being displayed, overwriting part of the display, waiting until the pilot finishes with the current task before interrupting, letting the pilot know that the data is available but will not be displayed until requested, or using an attention-getting device such as color, high-intensity or flashing graphics, audible tone, or spoken phrase. The display manager must keep track of what the pilot is currently viewing as well as what he has just viewed. Using this information and a description of the current situation, the display manager predicts what the pilot will want to see next, labels the programmable keys appropriately, and starts computing the highest probability displays to minimize the processing time required once the pilot makes a choice.

Certain functions are common to all subsystem managers. Each must keep the central manager informed of any changes in the subsystem's status, mode, or configuration. In addition to the shared data base managed by the data base manager, each subsystem will also have local memory storage for its own use. Each subsystem manager is responsible for controlling access to its local storage and any data transfer to or from the shared system data base or other subsystems. To a large extent, fault monitoring and inflight testing will be performed at the subsystem level by each subsystem manager. While the final decision on sensor assignments and reassignments is made by the central manager, each subsystem manager generates requests for the sensors it needs and controls the sensors it has already been assigned. In addition, certain data areas, processors, sensors, or equipment may be dedicated to a specific subsystem manager. What procedures to call and what parameters to call with them are decided at the subsystem level. If a procedure needs to communicate with another subsystem, with the central manager or pilot, or with the system data base, the subsystem manager is responsible for constructing an appropriate symbolic request and addressing it to the central manager, data base manager, display manager, or the desired subsystem manager.

The target acquisition subsystem manager's functions also include determining the area to be

searched with the subsystem's sensors, locating targets (azimuth and elevation), identifying and classifying targets (using data from other subsystems, digital terrain maps, prebriefed data, the pilot, and external sources), and maintaining the current target list.

The communications subsystem manager maintains and uses prebriefed frequency and call sign data; controls the message conditioning functions; manages target handoff, radio navigation, and IFF communications; is responsible for distributing the system's data to the outside world; and routes incoming data (such as inflight updates).

The fire control subsystem manager is the primary weapon manager. When using certain weapons, it determines what maneuvers are required to properly align the aircraft before launch. It contributes recommendations for weapon and platform assignments and processes target designations and fire commands. When target data is sent or received via communications, this subsystem is responsible for the message content.

The navigation subsystem manager maintains status and control of the Kalman filters and controls and updates the state vectors. It calculates the optimal trajectory to follow, taking into account the automatic flight and obstacle avoidance algorithms. It is in charge of the passive ranging and the offboard or non-line-of-sight target cueing functions. It controls the primary vehicle reference system and manages coordinate transformations.

The terrain data subsystem manager maintains the aircraft's current position relative to the digital map data base during all maneuvers. It resolves about line-of-sight conditions. It must handle regeneration of the appropriate map resolution from the compressed data, combine map data with any overlay data, and provide smooth map scrolling through the data base for both calculations and display functions. This manager fine-tunes route plans to take maximum advantage of the terrain. During internal or external updates or temporary loss of external navigation data, this system selects and orients the digital map from prominent local terrain features to maintain the aircraft's position at all times.

The survivability subsystem manager constantly monitors and categorizes threats, maintains the current threat list, warns the pilot of any threats, recommends and sets up appropriate maneuvers and countermeasures, and initiates any automatic or requested countermeasures or threat surveillance.

In summary, the pilot communicates with the system via the central manager. The central manager coordinates (sets priorities, resolves conflicts, assigns modes, etc.) the interactions between the subsystem managers. The data manager supports symbolic data access and maintains the system data base. Each subsystem manager controls all activity internal to its own subsystem, including management of any assigned sensors or memory storage, processing, testing, and reconfiguration.

Terrain Data Subsystem (TDS)

The TDS is a digital map data retrieval system that conditions stored digital map data into a form useful for avionics system algorithms. Modern avionics systems use digital data to perform terrain correlation navigation functions (e.g., SITAN) and to aid in TF/TA schemes, mission planning, and visual presentation of stored terrain information. An LHX TDS must provide digital imagery to allow the crew to quickly orient itself georgraphically, determine and display threat envelopes as a function of aircraft position, calculate and display the optimum flight path between two geographic points, automate mission planning, and allow precise prepointing of targeting sensors by supplying 3-D relative position between aircraft and prestored or mission-acquired targets. Figure 2 presents an example of functional flow.

Terrain data processing includes three major sections: data retrieval, processing algorithms, and display formatting. Data retrieval involves the control and interfacing of the bulk/cache memory section. The processing algorithms contain the functional algorithms associated with a terrain data system (e.g., SITAN or passive ranging). Display formatting the data produces information in the correct form to be displayed.

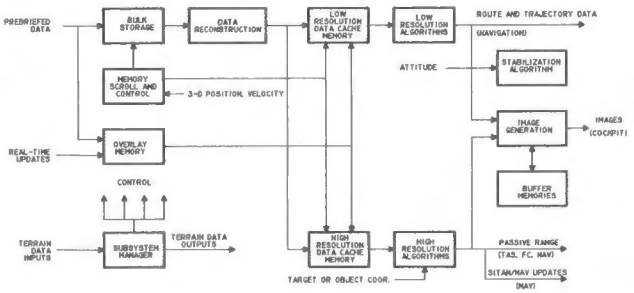

Figure 2. Terrain Data Functional Flow

The referenced map data is stored in a compressed format in a nonvolatile bulk memory system that contains terrain features, elevations, threat information, and cultural data. This information will come from the Defense Mapping Agency (DMA) and intelligence missions. The resolution of this data defines the accuracy of the system; therefore, system error is a determining factor in the selection of the data compression scheme.

Data accessed from the bulk memory undergoes data reconstruction (the inverse of the data compression algorithm) and is stored in small, fast-access time cache memories. These cache memories are large enough to allow for platform dynamics between refreshes; i.e., the storage area of these memories is based on the flight dynamics of the helicopter. The memory scroll and control function scrolls data into the cache memories when needed and provides the overall control for the retrieval system. Scrolling is dependent on vehicle speed and attitude. Real-time updates of terrain, cultural, and threat data acquired during the mission are needed. This information may be received either offboard or onboard and is stored in an update memory that is addressed and scrolled into the cache memories in a fashion similar to that of the bulk system.

High- and low-resolution data algorithms are performed after data retrieval. Passive ranging of targets from the TAS inputs is an example of a high-resolution algorithm. The TAS provides FLIR-derived target azimuth and elevation information to the terrain data subsystem, allowing the terrain system to trace a line-of-sight radial through the

map data to determine target range and the local slope of the terrain at the target. The target range is determined by the intersection of a ray from the platform, defined by azimuth and elevation to the target, with the terrain along the line-of-sight vector. The local slope is useful in many target identification algortihms. In an active radar mode, the TAS could provide target azimuth and range to the terrain system, which would then give local slope and target elevation.

High-resolution data is needed when creating realistic digital imagery. A perspective image of encountered terrain requires three steps: radial addressing, hidden-line computations, and scene generation. Radials of sight defined by display resolution, field of view, and sight distance are addressed in the cache memories. The elevations of the radial samples are scaled with respect to distance from the observation point and compared to see which points are hidden. A projection of the points not hidden is used to generate the scene to be displayed. A plan view image is created by displaying the elevations, features, and/or cultural data from a rectangularly addressed array of points about a reference observation point. Other examples of high-resolution algorithms are data conditioning for SITAN updates and data overlay of display images.

An example of a low-resolution data algorithm is a route-planning algorithm that uses stored threats, targets, terrain, and cultural data with a coarse mission route and mission parameters to plan optimal mission routes. These routes will take into account terrain variations and the line of sight of the identified threats. Given the start and end points of a mission, approved waypoints (points between start and end that are safe to travel) are determined and all possible routes through these points plotted. Deterministic rules are then used to pick the optimal route, with mission-acquired information being used to update and change the route when necessary.

The display formatting function converts the processed data into a display format. Examples are the overlaying of threat and target information onto scenes and perspective radial combinations in which all radials in the field of view are combined and filtered to create a pleasing scene. A stabilization algorithm is required to take roll and pitch into account in image displays.

TABLE 2. LHX TERRAIN DATA SYSTEM REQUIREMENTS PRELIMINARY

• AREA COVERAGE	100 KM × 100 KM, EXPANDABLE TO 1,000 KM BY 1,000 KM
• DATA SOURCE	DMA LEVEL I
• I/O	ELEVATION DATA TO TF/TA, NAV, WEAPON DELIVERY, THREAT AVOIDANCE
• I/O DATA QUALITY	
• DISPLAY	1 DISPLAY LEVEL MSE
• NAVIGATION	100 METER CEP FOR SITAN
• TF/TA	NO UNDERESTIMATES OF TERRAIN ELEVATION
• DISPLAY MODES (256 × 256 PIXELS)	
• PLAN VIEW	
• LINE-OF-SIGHT	
• PERSPECTIVE VIEW (OPTIONAL)	
• AIRCRAFT VELOCITY	450 KNOTS
• DISPLAY UPDATE RATES	
• FRAME	60 FRAMES/SECOND
• COMPLETE SCENE	10 TO 30 SECONDS
• SIZE, WEIGHT, POWER	1.5 ATR, 45 POUNDS, 450 WATTS

Baseline Requirements. Table 2 summarizes the baseline requirements for the TDS. It can be seen that the minimum area to be covered is 100 km x 100 km expandable to larger coverage by adding more memory or by exchanging memory modules. The source data will consist of DMA Level-I Digital Terrain Elevation Data (DTED), Digital Feature Analysis Data (DFA), plus imagery and information from other sources such as Landsat and intelligence sources. The TDS data will be distributed in a raw or preprocessed form; for example, information sent to the TF/TA processor could be an array of elevation values and/or vertical obstructions and heights, or range and angle information required to generate TF/TA commands.

Because of the large data storage requirements, some form of data compression will be required to minimize memory requirements. For this purpose, techniques are suitable, e.g., discrete cosine transforms, Block Truncation Coding, Hadamard transforms, and polynomial surface coding. Texas Instruments is conducting studies as part of the Air Forces Integrated Terrain Access and Retrieval System (ITARS) program to determine the impact of data compression reconstruction techniques and the performance of TF/TA, navigation, display, threat avoidance and weapon delivery algorithms on system hardware and software implementation. As a result of the studies, it will be possible to match the data compression technique to the application and select the optimal implementation. Examples of criteria for selecting data compression/reconstruction algorithms appear in Table 2 under the heading I/O data quality. The TDS will be able to provide plan views and direct line-of-sight views and be capable of generating real-time perspective views if required.

Present design goals are to have a TDS that will operate for aircraft velocities up to 450 knots,

display at 60 frames/second and have favorable size, weight, and power characteristics as shown in Table 2.

Again, it must be stated that Table 2 represents a baseline set of requirements which will evolve as new technology and new user requirements are identified and defined.

Terrain Data Subsystem Implementation Issues. Several areas inherent in the defined TDS require innovative design to allow implementation of the subsystem within the physical constraints of LHX. The bulk memory must be nonvolatile and lightweight and have reasonable access times. The leading technologies in this area are bubble memories and medium-density magnetic-tape technology. Data compression techniques currently in use may need to be improved to reduce the required storage to a more manageable level. Real-time generation of digital imagery requires very-high-speed address and graphics generation. This task seems to be ideally suited for VHSIC processors. Two architectures currently being used for terrain processing are the (DMG) and the alternative DMG.

The DMG which was developed under contract with the U.S. Army Avionics Research and Development activity, reconstructs compressed digital map information and provides outputs suitable for driving a CRT display. The DMG has three major sections: block-oriented functions, per-frame functions, and video processor functions.

Initally, functions are performed on blocks of data. The magnetic-tape loader (MTL) stores 81 Universal Transverse Mercator (UTM) blocks of digital terrain data. Each UTM block represents 12.5 x 12.5 kilometers. The intermediate memory acts as a cache memory, feeding data to the elevation and cultural reconstruction processors.

Elevation data is reconstructed with a Discrete Cosine Transform/Differential Pulse Code Modulation method. A footprint method is used to reconstruct cultural features. Reconstructed data is then stored in the scene memory, which acts as another cache memory, feeding data to the per-frame functions. Functions are then performed each display

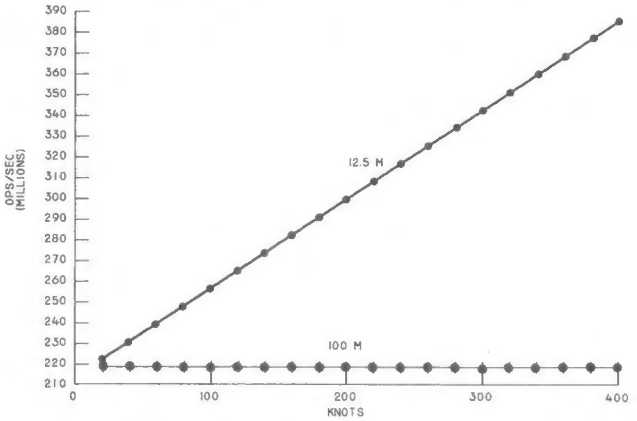

Figure 3. Digital Map Generator (Operations Per Second)

TABLE 3. DMG THROUGHPUT REQUIREMENTS

(DMG Operations per Second (12.5 meter data)
300 Knots

Tasks	Adds	Lookup	Compares	Logical	Shift	Mults
Elevation reconstruction	3.60E+07	6.83E+03	1.02E+04	6.83E+03	2.71E+05	3.55E+07
Feature reconstruct	4.35E+06	3.47E+03	1.12E+04	1.69E+02	1.74E+04	
Per-frame tasks	6.29E+07		5.60E+07	2.45E+07		3.50E+06
Totals	9.93E+07	1.03E+04	5.60E+07	2.45E+07	2.08E+05	3.90E+07
Tasks	**Sin-Cos**	**Inv Tan**	**Divides**	**Square Root**	**Ex Add**	**Ex Mult**
Elevation reconstruction	3.54E+07					
Feature reconstruct						
Per-frame tasks	6.00E+05	6.00E+01	6.00E+01	6.00E+01	7.00E+06	3.50E+06
Totals	4.23E+07	6.00E+01	6.00E+01	6.00E+01	7.00E+06	3.50E+06

Total OPS/second 3.43E+06
Total memory 46 MBITS

DMG Operations per Second (100 meter data)
300 Knots

Tasks	Adds	Lookup	Compares	Logical	Shift	Mults
Elevation reconstruction	1.37E+05	1.09E+03	2.99E+03	1.99E+03	2.01E+03	1.30E+05
Feature reconstruct	1.27E+05	1.01E+03	3.26E+03	4.94E+01	5.06E+03	
Per-frame tasks	6.29E+07		5.60E+07	2.45E+07		3.50E+06
Totals	6.32E+07	3.00E+03	5.60E+07	2.45E+07	7.06E+03	3.63E+06
Tasks	**Sin-Cos**	**Inv Tan**	**Divides**	**Square Root**	**Ex Add**	**Ex Mult**
Elevation reconstruction	1.30E+05					
Feature reconstruct						
Per-frame tasks	6.00E+06	6.00E+01	6.00E+01	6.00E+01	7.00E+06	3.50E+06
Totals	7.03E+06	6.00E+01	6.00E+01	6.00E+01	7.00E+06	3.50E+06

Total OPS/second 2.15E+08
Total memory 46 MBITS

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL SUPERHYBRID

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ABSTRACT

This paper describes the performance, physical and electrical characteristics of the BUS-65112 Superhybrid, which performs as a fully compliant MIL-STD-1553 Dual Redundant Remote Terminal Unit (RTU).

A discussion of the Custom Monolithic LSI components implemented in the Superhybrid will be included. The RTU's special features and capabilities will be highlighted, along with special programming options which facilitate a broad array of applications.

The BUS-65112 Superhybrid contains all the necessary control lines to allow easy Direct Memory Access (DMA). The interface timing, operational philosophy, and a block diagram highlighting the Superhybrid's functional architecture are included.

INTRODUCTION

A full array of LSI Monolithic IC's has been developed by ILC Data Device Corporation (DDC) specifically for MIL-STD-1553B RT implementation. It was the development of these LSI Chips that made the BUS-65112 Superhybrid possible. Figure 1 shows the internal placement of the Monolithic devices in the BUS-65112.

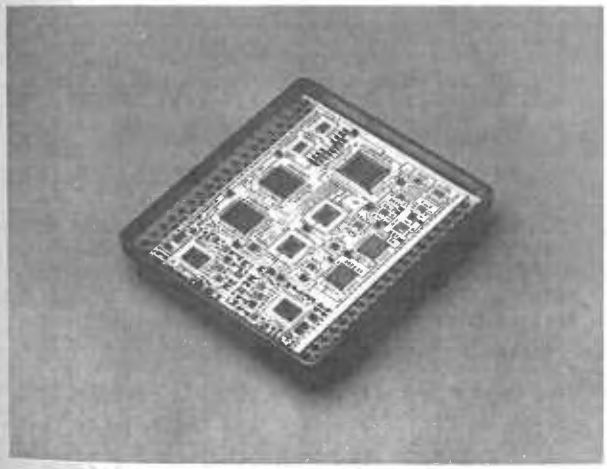

Figure 1: BUS-65112 Superhybrid

DDC embarked on an Internal R&D Monolithic Program to attain versatility, small size, low power and reduced end product cost. The development of the four Monolithic IC's really started following the success of the first Monolithic Transceiver. This Monolithic first appeared as the BUS-63105 Transceiver, which replaced the former BUS-8553 discrete version. This Bi-Polar Custom Monolithic not only replaces its predecessor but offers some additional features such as a 12 microsecond encoder input, time-out circuit and a short circuit protected driver output stage, using current limiting. A better mean time between failure (MTBF) computation was realized from the inherently low power density of the Custom Monolithic.

These monolithics were designed to interface with the Harris HD-15530 Encoder/Decoder and include a terminal bit processor (A'), interface logic (AB') and RT protocol sequencer called (B'). Figure 2, BUS-65122 Block Diagram shows how the superhybrid has been configured for implementation of a complete Dual Redundant MIL-STD-1553B Remote Terminal Unit.

The A' terminal bit processor LSI was developed to interface with the Harris Encoder/Decoder, providing Dual Rank Registers and three-state interface buffers that can be used for 8 bit/16 bit parallel transfers or serial transfers. It was designed to Flag Broadcast and mode code commands if enabled via accessible control lines. It also has 1553 MUX BUS Driver Watch Dog Time-out Logic.

The most important feature of the A' is the Built-In-Test (BIT) capability. This BIT consists of a 16 bit latch that captures the last 16 bit parallel word loaded into the Encoder for transmission. When the word is transmitted onto the 1553 MUX BUS, the transceivers' receiver, if enabled, will then wrap it around to the Decoder, which will permit logic to compare this decoded data with that already stored in the 16 bit latch. If it doesn't match, a Fault Flag is generated.

The AB' LSI Monolithic Multiplex CMOS IC interfaces with the two (A') Terminal Bit Processors and the RTU Protocol (B') Sequence Logic. Its main function is to validate incoming commands from the A' monolithics and then latch key control signals. The two sets of control signals are multiplexed so the 1553 protocol LSI chip sees only one set of key signals. The AB's allow the Dual Redundant 1553 MUX BUS implementation and proper handling of superseding valid commands. It also latches the bit results for the protocol internal bit register.

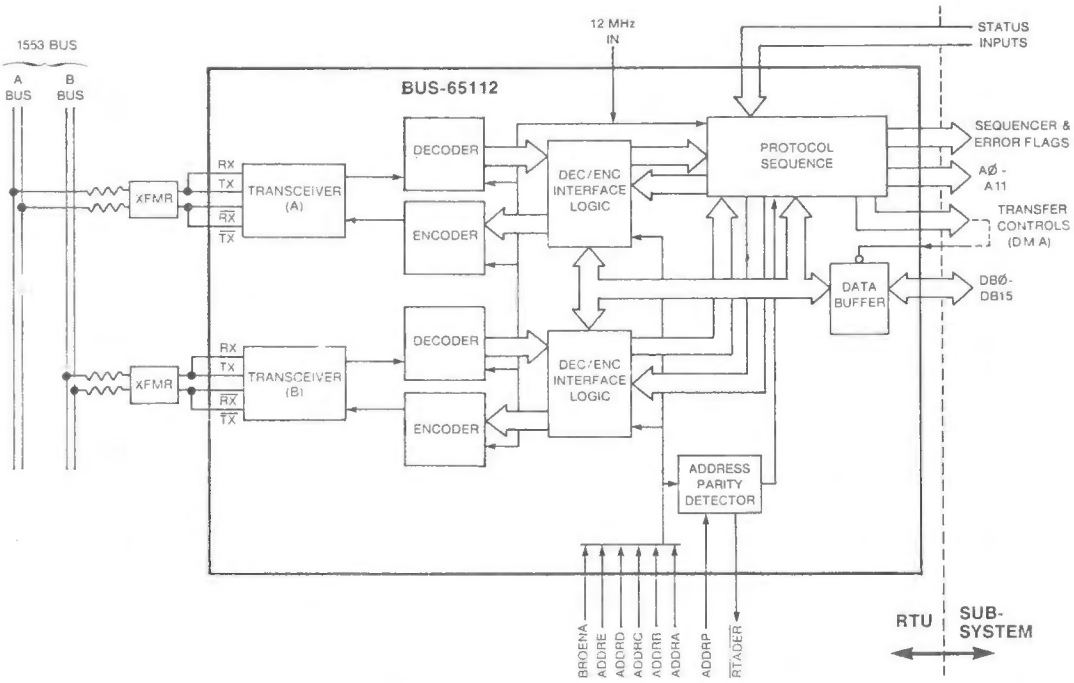

FIGURE 2. BUS-65112 BLOCK DIAGRAM

The AB' Interface Logic checks each command for a preceeding 2us minimum gap time as required by McAir specifications. It also provides the RT to RT no response time out, handshake fail (HS-FAIL) and status register time outs.

The B', LSI Monolithic MIL-STD-1553B RT Protocol CMOS Logic IC is the key element of the BUS-65112 Superhybrid. It performs all of the Dual Redundant 1553B RTU functions. the B' Protocol supports the following:

COMMAND WORD REGISTER
STATUS WORD REGISTER
LAST COMMAND WORD REGISTER
BIT WORD REGISTER
ALL 13 DUAL REDUNDANT 1553B MODE CODES
RT to RT, TRANSMITTING RT ADDRESS REGISTER
ALL 1553 MESSAGE TRANSFER FORMATS
OPTIONAL EXTERNAL PROM FOR ILLEGALIZATION OF MODE CODES AND SUBADDRESS

The B' interfaces with the Dual Redundant MUX BUS and handles all 1553 transfer formats. The protocol logic is designed to transfer data in or out of the subsystem interface unit (SSIU) using Direct Memory Access handshake signals (DMA). In conjunction with the DMA type transfers, B' latches the Command Word and generates a Current Word Counter (CWC) which is used to address the proper external RAM locations. All data transfers are 16 bit parallel with a drive capability of 7 TTL loads.

The SSIU has control over the: Terminal Flag, Busy, Subsystem Flag, Message Error, and the Dynamic Bus Acceptance Input Status Register bits. The command word is latched and available throughout a message transfer cycle. There are special output and input signals which will be covered in the discussion of operation.

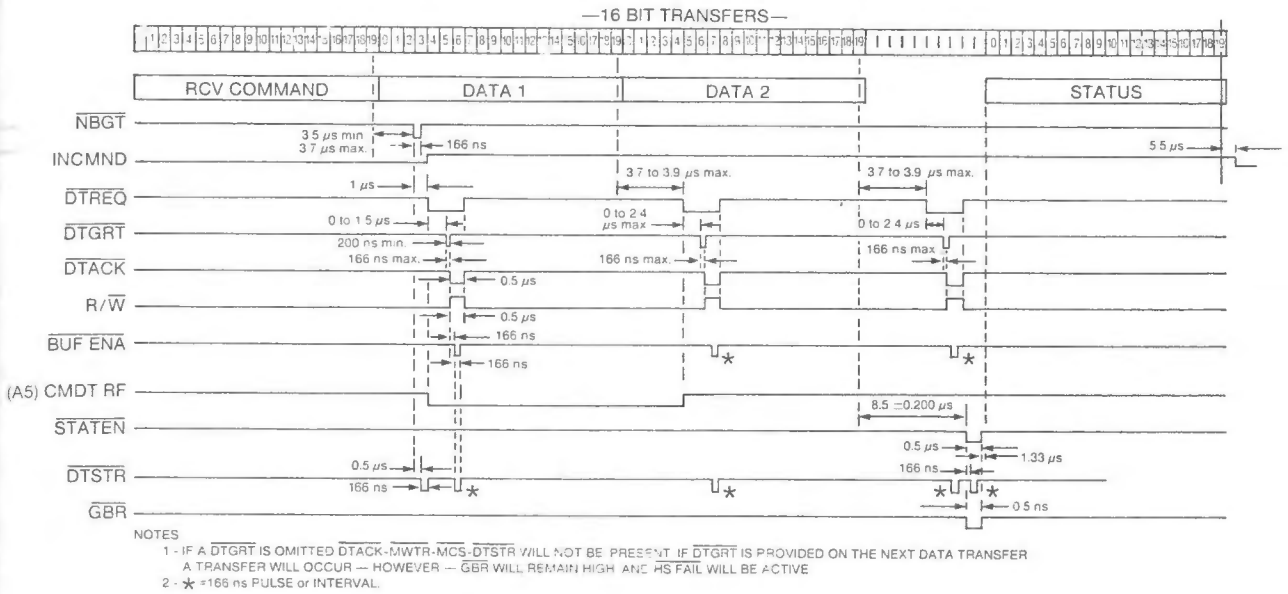

FIGURE 3. BUS-66108 RECEIVE COMMAND TIMING

DESCRIPTION

The BUS-65112, is a Dual Redundant MIL-STD-1553B Remote Terminal Unit. It contains two transceivers, two Harris HD-15530 Encoder/Decoders, two Terminal Bit Processors, two Interface Logic Blocks, one Protocol Logic Sequencer, CMOS Data Buffers and some miscellaneous logic, such as the address parity detector circuit. It requires two external BUS-25679 MUX BUS Transformers, one 12 megahertz TTL clock input, plus 5 volts, plus or minus 15 volts DC to operate. The BUS-65112 Hybrid measures 2.100" X 1.870" X .250" ht. maximum. This 3.93 square inch package makes use of 78 pins in a Dual-In-Line plug-in package configuration. The Bi-Polar and majority of CMOS devices makes this a very low power Dual Redundant RTU. At idle, the Superhybrid will require approximately 4.2 watts, while at 25 percent duty cycle it will draw 5.2 watts total. All this additional power is not dissipated within the hybrid, but transferred to the 1553 MUX BUS during message transfers.

The BUS-65112 has a dedicated internal 16 bit parallel highway which is isolated from the external 16 bit SSIU highway by a set of Bi-Directional CMOS Buffers. The Buffer Enable (PIN 67) signal is brought out to allow the SSIU to monitor the highway at all times or simply when data transfers to the SSIU are being performed. The type of transfer is of a DMA nature in that the RTU requests a transfer, waits for a SSIU Grant and then does the transfer. Figure 3, Receive Command Timing and Figure 4, Transmit Command Timimg, give typical 16 bit transfer details. Note that Data Strobes (DT STR) occur for each DMA transfer cycle and during BUS-65112 internal Command Word and Status Word transfers between the AB' and B' Monolithics. The STATEN signal designates which DT STR is transferring the Status Word Register contents to the A' for transmission.

The B' Protocol converts the external 12MHz clock to 6MHz. The 6MHz is used internally in order to generate and clock all SSIU interface control signals.

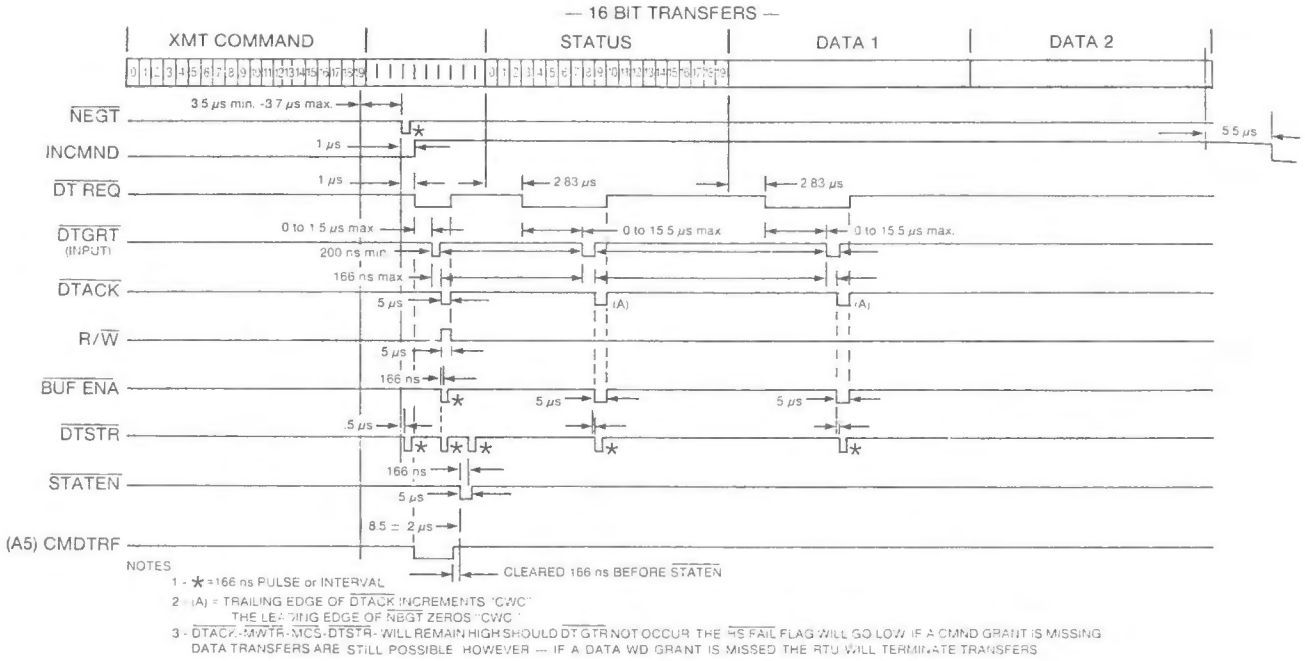

FIGURE 4. BUS-66108 TRANSMIT COMMAND TIMING

The Superhybrid generates a 12 bit address field which is used by the SSIU to read or write into memory. Bits A0 - A4 are equal to the Word Count Field (WC) between the NBGT and INCMD period of a normal transmit/receive command. It is always the WC during the process of a Valid Mode Command when INCMD is valid A0 - A4 then becomes the Current Word Counter (CWC) field starting at zero. The trailing edge of DTACK increments the CWC by one. The A5 bit is the Command Transfer Signal (CMDTRF) that tells the SSIU that the DTREQ represents the Valid Command Transfer. The A6 - A10 bits represent the Valid Command Words T/R bit. The A0 bit is the least significant bit (LSB), while A11 is the MSB bit. The Address Field is latched for the entire transfer cycle with the exception of the CWC being incremented for each Data Word Transfer.

ERROR FLAGS

There are four Error Flags which can be used by the SSIU to detect if anything is wrong with the BUS-65112 terminal. The first is the Message Error (ME) Flag, which goes low as soon as the RT detects a message error condition, Format Error, Word Count Error, Invalid Words, Sync Error, RT to RT Command Address Error or T/R Bit Error. The second is the RT-FAIL Flag indicating an internal RT failure. The RT FAIL signal indicates when the A' or B' Monolithic devices fail during an RT transmission via the BIT. The Wrap Around Bit Test checks the last word transmitted for incorrect sync type Manchester II Error. The Watch Dog Time-Out also sets this RT FAIL Flag. The RT FAIL Flag is cleared the next time the RT initiates a new status word transmission. The third error flag condition is the Handshake Failure (HS FAIL) which indicates when an SSIU fails to give the required data transfer grant in (DTGRT) in time. If a command word grant is missing, data transfers are still possible, however, if a data word grant is missed, the RT will terminate transfers. The fourth type of output flag is the RT Address Error (RTADERR) which indicates a parity failure on the unique RT address inputs ADDRA thru ADDRP. If one of the hardwired RT address lines should open, the RT ADDERR would flag the problem to the SSIU.

OUTPUT SIGNALS

The BUS-65112 has a number of useful output signals to interrupt the SSIU such as:

(1) NBGT - New Bus Grant - Low level output pulse used to indicate the start of a new protocol sequence in response to the Command Word just received.

(2) INCMND - High Level Output used to inform the SSIU that the RT is presently servicing a command.

(3) STATEN - Status Word Enable - Low level active output present when the Status Word is enabled onto the 16 Bit Parallel Highway.

(4) BITEN - Built-In-Test Word Enable - Low level used output present when the BIT Register contents is enabled onto the 16 Bit Parallel Highway.

(5) GBR - Good Block Received Word - Low level pulse used to flag the SSIU that a Valid, Legal, Non-Mode Receive Command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.

SPECIAL OPERATING FEATURES - Inputs

There are two inputs which provide the SSIU with special operating features. The first is the RESET signal. This active low input causes the BUS-65112 to reset all logic, for power-up and initialization sequences. The second special signal is the Broadcast Enable (BROENA), when high allows RT recognition of all ones in the Command Word as a Broadcast Message per MIL-STD-1553B. When low, the RT will not respond to the RT Address 31, unless it was the assigned terminal address.

In addition to the two input signals just described, the BUS-65112 features 6 inputs which provide control of the bits in the Status Word. One of the most unique and useful inputs is the Illegal Command (ILLCMD) which allows the subsystem to illegalize any command or mode code. That means any subaddress or any of the 1553B Dual Redundant Mode Codes not implemented by the SSIU can be illegalized. This can be accomplished by placing a properly programmed PROM across the latched command word outputs. When an illegal pattern presents itself, the PROM will output the illegal flag, which is read by the B' at the proper time. The ME BIT will be set and the RT will transmit the Status Word, but won't transfer any data to or from the SSIU.

The second is the Subsystem Request (SRQ), which is an input from the SSIU used to control the service request bit in the status register. If low when the status word is updated, the bit will be set, if high, it will be cleared. The third is the Accept Dynamic Bus Control (ADBC). An active low input from the SSIU used to set the Dynamic Bus Control Acceptance Bit in the Status Register if the Command Word was a valid, legal mode command for dynamic bus control.The fourth is the Remote Terminal Flag (RT FLAG) used to control the terminal flag bit in the Status Register. If low when the Status Word is updated, the Terminal Flag Bit would be set, if high, it would be cleared.

The fifth signal is the Subsystem Busy (BUSY) used to control the busy bit in the status register. If low when the status word is updated, the busy bit will be set, if high, it will be cleared. If the Busy Bit is set in the status register, no data will be requested from the subsystem in response to a transmit command, on receive commands data will still be transferred to the SSIU. The sixth and last signal is the Subsystem Flag (SS FLAG) used to control the subsystem flag bit in the status register. If low when the status word is updated, the SS FLAG will be set, if high, it will be cleared.

TYPICAL MODES

The BUS-65112 Superhybrid Protocol Logic, when preparing its response to a command, entertains basically four typical modes. The B' protocol, in determining its proper course of action, looks at the type of command and the associated T/R Bit. The first case is when a Mode Code is received with a T/R = 1, the B' checks the WC4 Bit to see if its zero for no data. This is also performed for reserved Mode Codes. If the WC4 Bit is not zero, the RT transmits the Status Word only. The second case is when a command is received with a T/R = 0, the WC4 Bit = 0, and no data is received, the B' automatically sets the ME bit of the status register and doesn't transmit the status word. The third case is when the WC4 = 1, the T/R Bit = 0, and one and only one data word is received, the RT will respond with a status word only. If no data or too many data words are received, the RT will set the ME Bit and not respond with a status word. The fourth or last consideration is when WC4 = 1 and T/R = 1, but its not a Transmit Bit Word Mode Command or Transmit Last Command Word Mode Command the RT will transmit the Status Word and request one word from the SSIU, unless illegalized by the optional external PROM.

The Bit Word Register is set up using 14 bits to provide the Bus Controller with a full report of the RT's condition. When the RT receives the Transmit Bit Word Mode Command a Status Word followed by the Bit Word is transmitted. The Bit Word is as follows:

```
     SYNC FIELD
LSB  BIT 15 - NA
     BIT 14 - NA
     BIT 13 - CHANNEL B TIME OUT
     BIT 12 - CHANNEL A TIME OUT
     BIT 11 - CHANNEL B BIT
     BIT 10 - CHANNEL A BIT
     BIT  9 - XMTR B SHUTDOWN
     BIT  8 - XMTR A SHUTDOWN
     BIT  7 - BROADCAST RECEIVED
     BIT  6 - WORD COUNT HIGH
     BIT  5 - WORD COUNT LOW
     BIT  4 - ILLEGAL MODE COMMAND
     BIT  3 - T/R BIT OR MODE CODE ERROR
     BIT  2 - BIT TEST FAILURE
     BIT  1 - HANDSHAKE FAILURE
MSB  BIT  0 - CHANNEL A OR B TIME OUT
     PARITY
```

The BIT 12 & 13 Channel A or B Time Out Flags indicate when either of the Watch Dog Timers have exceeded 800 microseconds. The Built-In-Test (BIT), which is continuously being performed with each and every message transfer dynamically, is next. The BIT checks for correct sync, and that there is no Manchester coding or parity errors as well checking the last word wrap-around for each transmission. The transmitter (XMTR) Shutdown for Channel A or B represents when the Mode Command has been exercised. If a Broadcast Command was received, BIT 7 will be set. If a Command with more words or less words than specified in the WC field is encountered, BITS 6 & 5, respectively will be set in the BIT Word Register. If the optional illegal mode command PROM is used, BIT 4 will be set when one is received. The BIT 3, indicates when a Mode Command is received with an incorrect T/R setting. Bit 2, flags when a BIT fault has occurred on either channel. Bit 1, Handshake Fail Flag, is set once a grant is not received on time. The last Bit 0 indicates when the 1553 Watch Dog Time Out Circuit timed out on either Channel A or B.

SUMMARY

All of the above features, along with the 14 Bit Built-In-Test Register makes this BUS-65112 a very powerful
remote terminal unit. The Superhybrids small size, low power, low price and flexibility make it an ideal choice in space limited military applications where full 883B level screened parts that can operate from -55 degrees C to +125 degrees C case temperatures are needed.

VLSI CHIP SET FOR HIGH-PERFORMANCE AVIONIC COMPUTERS

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ABSTRACT

Advanced CMOS processing with line widths of two micrometers makes possible a VLSI implementation of avionics computers. Using a chip set designed with 6000-gate gate arrays has allowed the design of a very high-performance, yet small, low-power, cost-effective, and highly flexible avionics computer.

The chip set comprises four chips: the microsequencer (USEQ), the arithmetic and logic unit (ALU), the operand generator unit (OGU), and the memory controller unit (MCU). The four chips can be configured to implement the Air Force standard instruction set architecture (MIL-STD-1750A, Notice 1) and emulate the Navy standard computers (AN/UYK-20, AN/AYK-14, and AN/UYK-44). An overview of the chip architectures is presented in this paper.

INTRODUCTION

Today's avionics computers must combine high processing throughput with low power consumption and small size, and yet remain cost-effective and flexible. Meeting such requirements is no easy task, as evidenced by many systems in the field today. Some systems, using emitter-coupled logic, have gained performance at the expense of power; some are too large for airborne requirements; while others have been so optimized for a specific task that they cannot be used for any other purpose. Even those systems which meet the power, size, and flexibility criteria never seem to have the performance needed for many real-time applications.

Many avionic computers have evolved from architectures which were designed to make the best of low-performance core memories [1]. Replacing the core memories with faster semiconductor memories has allowed for some increase in the performance of such machines. However, these machines are limited by the underlying architectures, unable to take full advantage of the performance increases possible with newer technologies. The problem becomes apparent: how to combine technology with suitable architectures to produce a machine which meets the desired performance, power, size, cost, and flexibility objectives. The solution should be obvious: new technologies require new architectures. The remainder of this paper discusses a VLSI chip set which implements this solution.

THE CHIP SET

The chip set comprises four chips: the microsequencer (USEQ), the arithmetic and logic unit (ALU), the operand generator unit (OGU), and the memory controller unit (MCU). The four chips can be configured (with appropriate support chips) to implement the Air Force standard instruction set architecture (ISA), MIL-STD-1750A (Notice 1). These same chips can also be used to emulate the Navy standard 16-bit computers: AN/UYK-20, AN/AYK-14, and AN/UYK-44.

Figure 1 shows a typical configuration for these chips, including memory and support functions. The USEQ, ALU, and OGU chips compose the heart of the central processing subsystem (CPU). The memory subsystem requires at least two independent memory banks, each with its own MCU.

The chip set has been implemented with 2-micrometer CMOS processing. Each chip has the equivalent complexity of a 6000-gate device. The chip set was designed for execution of the DAIS floating-point instruction mix at two million instructions per second (MIPS) and execution of fixed point instructions at 4 MIPS. This performance has been achieved by employing a six-level pipelined CPU, and a memory subsystem with multiple independent banks which allows simultaneous instruction and operand accesses. Power dissipation is 1.1 watts per chip (typical).

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* Member IEEE

This work was supported in part by the Naval Research Laboratory under contract N00014-84-C-2250.

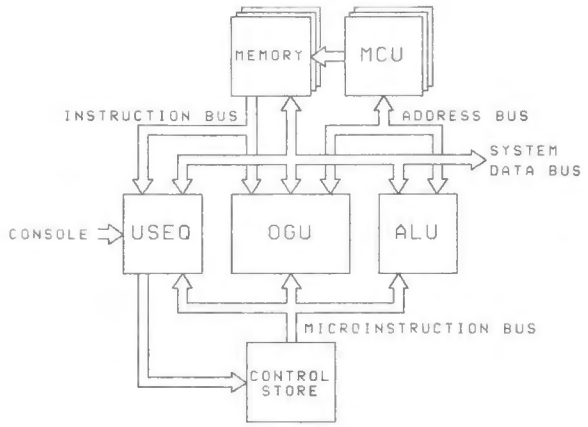

Figure 1. SYSTEM USING VLSI CHIP SET

The Microsequencer Chip

The USEQ chip (Figure 2) decodes instructions from the instruction pipeline and controls microinstruction sequencing. The chip contains five functional units: the instruction queue, the microaddress generator unit (MGU), interrupt processing logic (IPL), the control unit, and the microbranch detect unit (MDU).

The instruction queue buffers machine instructions for decoding and subsequent execution. The queue holds four single-word instructions or two double-word instructions.

The MGU forms the microaddress of the next microinstruction to be executed. The microaddress is derived from the microprogram counter, the microaddress stack, the microliteral (from the current microinstruction), or from the decoded machine instruction. The microaddress is used to access the off-chip control store.

The IPL maintains surveillance of various internal and external fault flags, forcing interrupt processing to occur as necessary. The IPL receives data (e.g. interrupt masks) via the system data bus. Also included in this unit are timers which can be used as watchdog timers or real-time clocks. These timers are also loaded via the system data bus.

The control unit receives microinstructions from the control store and uses these primarily for controlling the formation of the next microaddress. This unit also receives the microliteral field of the microinstruction, which is used in forming the next microaddress.

The MDU maintains surveillance of internal status flags and detects conditions which require microbranching. Control signals are provided from the ALU chip for branching. These controls insure that the instruction queue contains the proper sequence of machine instructions.

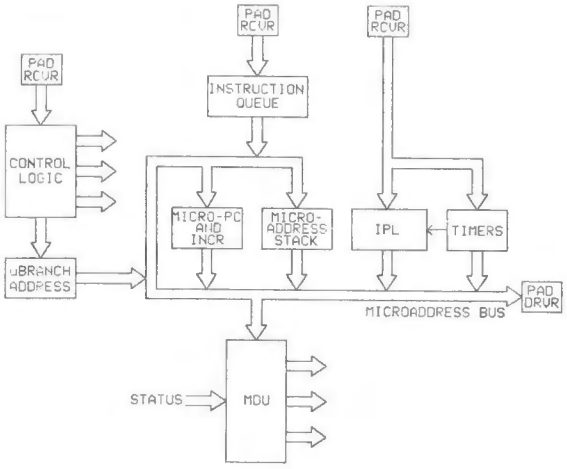

Figure 2. MICROSEQUENCER BLOCK DIAGRAM

The Arithmetic and Logic Unit Chip

The ALU chip (Figure 3) uses a 32-bit internal architecture to perform both fixed-point and floating-point operations. The chip has four functional units: the ALU, the program status unit, the control unit, and an external interface.

The ALU portion of the chip comprises a set of pipeline registers and an accumulator. They are configured as pairs of 16-bit registers, each 16-bit register is provided with individual controls so that both single- and double-precision operands can be handled efficiently. The ALU, shifter, and floating-point unit (FPU) are each 32-bits wide. These units are connected to an internal 32-bit bus. Results of operations are placed on this bus, where they may either be sent out on the system bus or used as operands during subsequent operations.

The chip interfaces with other system elements via three 16-bit buses. All three are tri-state; two are bidirectional. Two buses supply data operands to the ALU. The results of ALU operations are sent over the system data bus (16 bits at a time, controlled by the external interface), or additionally, over the bidirectional data operand bus. This capability is particularly useful for double-precision operations which require one of the words of the result to be reused (e.g. double-precision multiply).

The program status unit maintains the machine state, using status flags (e.g. carry, overflow,etc.) from the ALU, shifter, and FPU, as well as data on the internal data bus.

The chip receives encoded instructions from the control store. These instructions are decoded by the control unit and routed to the appropriate circuits on the chip.

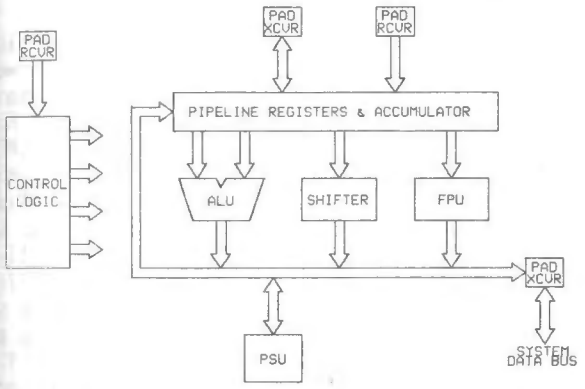

Figure 3. ALU BLOCK DIAGRAM

The Operand Generator Unit Chip

The OGU chip (Figure 4) is tasked with providing the data operands to the ALU chip. These operands come from the register file or from memory. In the latter case, the OGU provides the data memory address to the memory controller chip.

The chip is divided into five functional units: the instruction queue, the instruction prefetch unit (IPU), the register file, the address generator unit (AGU), and the control unit.

The instruction queue is an exact copy of the instruction queue on the microsequencer chip. The instructions are buffered on the OGU to provide the register addresses for machine instructions.

The controls for the instruction pipeline (on both the OGU and the USEQ chips) originate from the IPU. The IPU uses information in each microinstruction, as well as signals from the microbranch detect unit and program status unit on the USEQ and ALU chips, to keep the pipeline filled.

The register file on the OGU consists of sixteen 16-bit registers, addressed by a read address and a write address. It allows two read operations and one write operation per machine cycle. Data read from the register file can be used as data by the ALU and/or used to compute a logical memory address by the address generator.

The address generator unit's primary function is to calculate logical addresses. This unit allows memory-indexed operations to execute in a single machine cycle, saving time and control store space. The AGU is also used to adjust operands before being piped to the ALU.

The control unit on the OGU, in addition to decoding microinstructions, controls pipeline data bypass logic. Bypass operations allow the CPU to proceed, without waiting, when one instruction execution requires the result value of the immediately preceding instruction. Without the bypass logic execution would be delayed while the needed operand flows through the pipeline.

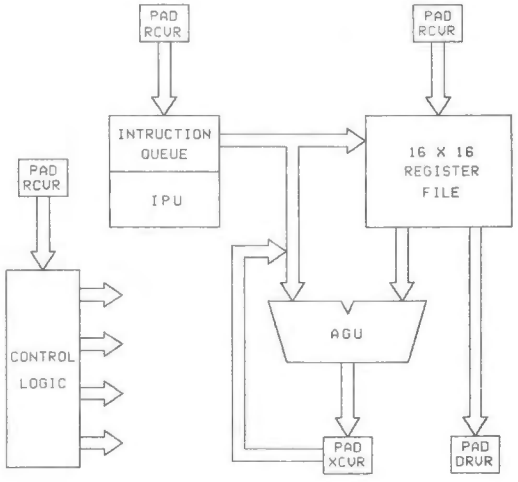

Figure 4. OGU BLOCK DIAGRAM

The Memory Controller Unit Chip

The MCU gate array (Figure 5) controls a single bank of up to 128K words of memory. It provides the following capabilities: dual-port control with contention resolution; multi-mode logical-to-physical address translation; read/write/execute protection; and a program counter for instruction port accesses.

The Memory Controller transfers information to and from the rest of the computer via the address bus. This information includes logical addresses, physical addresses, protection flags, and fault codes.

Memory data does not pass through the Memory Controller gate array, but instead is gated to/from the instruction or data bus by signals generated in the memory controller; this reduces the number of pins required on the gate array.

The Memory Controller is able to accept two simultaneous memory requests, one for instructions and one for operand data. Instruction addresses come from the on-chip program counter (except in the case of program branches) in order to reduce the number of wires connecting the memory with the CPU. Operand addresses come from the OGU chip via the address bus. In most cases, the two requests are handled simultaneously by memory controllers in separate banks. Occasionally, both requests must be serviced in the same bank; the memory controller contention resolution logic then sequences the operations on the memory array.

A content-addressable memory (CAM) allows logical-to-physical address translation and protection operations to occur simultaneously with address decoding, increasing throughput when translation is required. When an address is not found in any memory controller's CAM, the CAM is updated by the CPU.

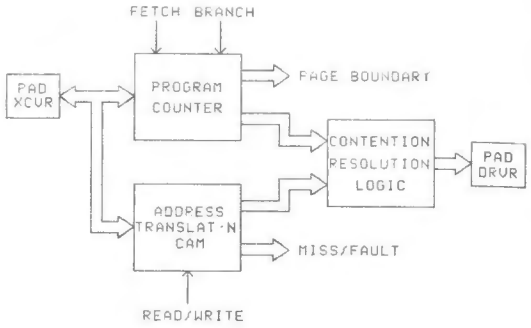

Figure 5. MEMORY CONTROLLER CHIP BLOCK DIAGRAM

SUMMARY

Today's avionic computers must combine high processing throughput with low power consumption and small size, and yet remain cost-effective and flexible. New architectures implemented with advanced CMOS gate arrays have resulted in a highly flexible VLSI chip set, capable of executing the DAIS floating-point instruction mix at VHSIC speeds. The floating-point execution rate of 2 MIPS and fixed-point instruction rate of 4 MIPS, surpasses the performance of other machines of equal size and power by as much as 50-100%. These chips implement the MIL-STD-1750A (Notice 1) 16-bit ISA and emulate the AN/AYK-14, AN/UYK-20, and AN/UYK-44 standard computers.

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SESSION 22 AIRBORNE SEPARATION ASSURANCE

Chairman:

Frank Chandler
Sperry Dalmo Victor, Inc.

Joseph J. Fee
Federal Aviation Administration

This session provides an understanding of the plans, designs, experiences and problems concerning current and future collision avoidance systems and select mode transponders.

EVOLUTION OF THE COLLISION AVOIDANCE SYSTEM IN THE COCKPIT

William L. Hyland

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Washington, D.C.

Abstract

Collision Avoidance Systems have been in various stages of development for a number of years. The aviation community is now on the verge of adopting the Traffic Alert and Collision Avoidance System (TCAS) for operational implementation. The majority of efforts over these development years have been devoted to the engineering aspects of the systems. As the system's concepts matured, the emphasis on the pilot use of the system has increased, with the attendant impact on system design of these evolutions. This paper treats the cockpit side of the systems evaluation, and the evolution of operational concepts over these years.

Introduction

The development of methodologies and systems for reducing the potential of aircraft midair collisions has been underway since the second airplane took off. Much effort has been expended by engineers and pilots to improve the capabilities of pilots to visually acquire and avoid potentially threatening aircraft. Many years of experience have produced the present "rules of the road", and pilot procedures for "seeing-and-avoiding" other aircraft. Special aircraft paint and visual alerting devices, such as navigation lights, beacons and strobe lights have improved those capabilities. The air traffic control radar has improved the system for IFR and controlled aircraft.

In recent years, more active collision avoidance systems have been proposed and evaluated to further improve these capabilities. In 1966, the airline community proposed an airborne system for air carrier use based on dedicated equipments for all users, operating at 1600 -1615 MHz. (1). This system became known as the Airborne Collision Avoidance System (ACAS). The FAA began development testing of a ground based collision avoidance system in 1974, designed to operate in the existing air traffic control radar beacon band at 1030-1090 MHz. This system, known as Intermittant Positive Control (IPC) (2) was intended for the general aviation community.

In 1975, the FAA began development of an airborne beacon-based system, known as BCAS. As the benefits of the beacon-based solution became more evident, the FAA in 1976 (3) proposed a combination of airborne and ground systems to improve "Airborne Separation Assurance" (ASA). In 1981, the FAA eliminated the ground-based portion of ASA and the Traffic Alert and Collision Avoidance System (TCAS) became the final system of choice.

Through the above progression of systems, evaluation of use of the devices in the cockpit has progressed from none to comprehensive. As pilots began to be more involved in the systems, changes in performance of the systems were introduced. Although little change in the basic concepts of the radio frequency (r.f.) portions of the system occured, the requirements for warning times needed by the pilot and the impact of rates at which alerts were experienced had considerable influence on the overall system design.

Earlier Systems

The ACAS envisioned by the airlines was basically an alerting system developed to deliver collision avoidance "commands" to the pilot. For display of this information, the system integrated the collision avoidance commands with an existing Instantaneous Vertical Speed Indicator (IVSI) instrument. The threat algorithm developed provided alerts with a 40-second and 25-second "time-to-collision" (TAU) and altitude separation of up to 3400 feet. The threat criteria produced the following commands:

Limit descend to 2000'	Limit climb to 2000'
Limit descend to 1000'	Limit climb to 1000'
Limit descend to 500'	Limit climb to 500'
Don't descend	Don't climb
Climb	Descend

The integrated display (figure 1) provided a red climb or descend arrow, with segmented amber lights around the ring for limit rates. Because of the perceived need to control the environment when "commanding" a pilot to maneuver vertically, the display further instructed the pilot to "Don't Turn"! Pilot organizations found these proposed methodologies acceptable. However, there remained some concerns for the impact on the ATC system, and for possible false alarms.

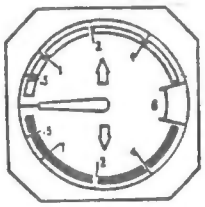

Figure 1

While no actual pilot evaluations in operational environments were conducted, an ATC simulation was conducted to assess the CAS impact on the operating environment (4). It was found that the rate of cockpit alerts in the dense terminals would be excessively high because of the large protection volume, and that the phase of flight and location in the pattern at which the high number of alerts would occur would unnecessarily disrupt the ATC system. Commands were being generated with the "don't turn" instruction, which when delivered in the approach phase confused the overall air traffic control situation.

The ground-based system, IPC (later known as Automatic Traffic Advisory and Resolution System, ATARS), originated from a background of general

aviation proximity warning systems, and had developed into a more complex system with maneuver commands. It was intended for delivering horizontal as well as vertical maneuver commands. The display developed for panel mounting (figure 2) provided the following:

Climb/Don't Climb	Turn Right/Don't Turn Right
Descend/Don't Descend	Turn Left/Don't Turn Left

It did not use the IVSI or "limit rate" commands. The display also provided course bearing information on intruder traffic, in clock position lights, and altitude information at these clock positions displayed as "above", "coaltitude" or "below".

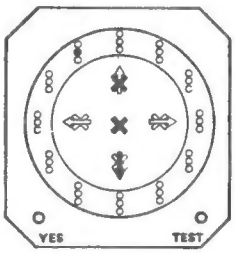

Figure 2

Some actual experience was gained in flying the IPC (5), although at this point the concept emphasized the general aviation environment and relied on VFR conditions and visual acquisition in most cases. A concept of priorities of alerts was conceived to first alert a pilot to a threat, and finally to maneuver. It used a decreasing time to collision (TAU) threat volume to generate these alerts. Many of the conclusions reached in these tests were as a result of the visual acquisition of the target aircraft. At this point the traffic advisory feature in VFR environments gained support.

BCAS and IPC

When the decision was made by the FAA to support a beacon-based collision avoidance system mainly because of the large number of operating transponder equiped aircraft, the operational concepts of ACAS and IPC were integrated. A lower cost active BCAS (i.e., actively interrogating other aircraft) would operate when out of ground radar coverage, providing vertical-only commands. A passive BCAS (i.e., listening to replies in response to ground interrogation) would operate within radar coverage and provide horizontal commands as well as range, bearing and altitude information. The IPC, which relied on use of the ground-based beacon system to derive collision avoidance data and transmit information, would individually tailor the threat volumes in terminal environments to reduce alert rates in the denser terminal areas. At this point a cockpit simulation of the BCAS and IPC operation was conducted with airline pilots to select suitable display(s) for further CAS testing (6). This cockpit evaluation determined acceptable displays, using integrated instruments (e.g., IVSI), CRTs and LED techniques. In integrating the displays, the general aviation IPC display was dropped and CRT techniques used. This allowed display of range from IPC not formerly possible with the general aviation IPC display. Pilots felt that altitude, range, relative bearing and heading of the threat aircraft was essential, in that order. Seventy-nine percent felt the traffic information was essential. The integrated IVSI display was again found acceptable because of the obvious combining of vertical rate information with vertical CAS maneuver commands, and a plan view display for traffic information was preferred, when the information was available.

In this time period, the BCAS alert rate subject was readdressed in ATC simulations. The "vertical only" active BCAS was still functionally quite similar to ACAS. The requirement to prevent turning when "commanding" a manuever was dropped to minimize unnecessary ATC impact. Also the idea that a pilot had no choice in the matter was modified and the idea that a "resolution advisory" would be provided to the pilot was adopted, assuming a pilot always retained his own decision authority. In the ATC simulations (7), the continuing high alert rate, largely because of the 40-second TAU alert, was reconsidered. The algorithm was reconfigured to provide a softer advisory; i.e., a "limit rate" advisory when appropriate, but within the same time reference as the resolution advisory; i.e., 25 seconds and not using the wider absolute altitude band. This reduced the alarm rates, but still provided the pilot only a limited number of change-of-direction instructions. Features were included to desensitize or reduce the threat volume for each aircraft similar to the technique used for the IPC; i.e., 30 seconds, 25 seconds and 20 seconds TAU, but based on altitude. It was recognized that the protection volume would be reduced as the aircraft entered the terminal areas (with decreasing altitude), but this was a trade-off with alert rates, the continuing concern of the user. This reduced threat volume was also consistant with reduced spacing criteria applied by ATC in the terminal areas. Traffic advisory information would remain an option.

Equipments were procured and a system installed on an operating Piedmont Airlines air carrier, with an integrated IVSI display located in the observer's position to gather more data in the operating environment. For the benefit of the observers and to gather information on the traffic advisory feature while in an air carrier cockpit, coarse bearing, range and encoded altitude information was provided on a CRT. These tests noted a high number of unnecessary alerts from on-the-ground aircraft, a relatively "acceptable" rate on the remaining alerts, and some, although not universal, interest in the traffic advisory feature (8). Concerns for "false" alerts; i.e., maneuver instructions on non-existent aircraft did not appear to be a factor. It began to be noted, however, that most of the resolution advisories that did occur were instructing maneuvers that were the same as a maneuver about to be made, was already in progress, or visual acquisition was made and could be ignored. The unnecessary alerts on the ground could be eliminated by technical

solutions, but what was the altitude of the pilot toward the alerts that he didn't need to follow? Most did not find them objectionable as long as the rate was low, and the rate was low. This experience in live air carrier environments began a much closer observation of the pilot reactions to the BCAS information.

In June 1981, a decision was made to pursue only the airborne solution to CAS, the TCAS. The ATARS was deleted, and all efforts focused on the active system. With this commitment, a sequence of air carrier cockpit simulations and limited flight tests was conceived to more closely assess pilot reactions to the maneuver and traffic advisory information.

When preparations for these tests were made, two opposing positions emerged on the traffic advisory feature, which had become one of the principal issues of cockpit implementation of TCAS. Against the traffic advisory was the obvious competition for scarce panel space for another display, possible distraction of the pilot in denser areas with information perhaps not necessary when on IFR flight plans, and possible overuse and contention with ATC for approach management. It was felt to be an expensive "option". This faction generally also felt that the IFR oriented air carrier pilots would follow the resolution advisories automatically when in IFR conditions, and that following the resolution advisories must be mandatory at all times making a traffic advisory display superfluous.

The other faction felt that pilots needed to have advance information on threatening traffic before maneuvering, that traffic advisories were essential to permit pilots to correlate resolution advisories with aircraft in sight, and that pilots could make their own decision on whether to follow the resolution advisories if better information was available.

In response to the above concerns, a methodology was adopted to 1) share the panel space by using the already developed Integrated IVSI for resolution advisories and the Weather Radar display for traffic advisory information (figure 3), 2) test for pilot response in cockpit simulations of IMC conditions, and in operational airspace under VMC conditions, and 3) select display methodologies to limit the distraction to the pilots but still provide him the intended information.

The first cockpit simulation (9) established audio and visual alerting criteria, and added voice reinforcement to the advisories. Color variations in CRT display methodologies for traffic advisories were included (although color was not necessarily required) to depict the priority of alerts; i.e., white for information, amber for caution, and red for warning. These and the integrated IVSI were accepted for further evaluation.

In conducting the operational flights in a twin engined C-421 at Lincoln Laboratory (10), a concept for the use of traffic advisory information was defined. To determine the pilots ability to use the information for only TCAS related potential threats, and not to manage flight paths, the weather radar display was

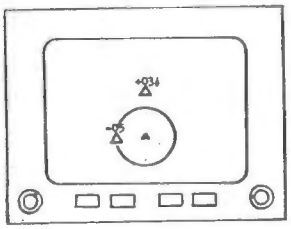

Figure 3

activated with the traffic situation only when TCAS identified a potential threat. Also, a pilot option to check the information on a request basis for a 15 second time-out period was provided. An additional factor developed during the tests was the need to consider traffic advisiories on all beacon traffic, including aircraft without Mode C and this feature was added for evaluation. Several optional ranges, and different numbers of displayed targets within those ranges were evaluated. It was decided to display all aircraft within 4 miles and $\pm$ 1200 feet of own aircraft wherever any potential threat aircraft activated the traffic display to enable the pilot to be aware of this "situation" at the time of alert. Also, because of pilot concern for the inability to ascertain the vertical direction of the threat, a vertical direction arrow was added to the threat traffic information if its rate exceeded 500 fpm. The workload of the traffic advisory did not seem excessive.

Some questions arose about the use of the red climb and descend arrows; i.e., possible interpretation as "don't fly in this direction." Also, since the cockpit alerting criteria established a color scheme for priorities, when used, the amber limit rate light segments of the IVSI in some cases would be tied to a warning-level red on a traffic display. In other cases a red arrow is provided with a red traffic advisory warning. Since both of the resolution advisories require the same response time, a possible inconsistancy existed between the intended alerting priorities of the two displays. In a finally adopted display configuration, this feature will need to be refined, but tests continued with this configuration.

In the second cockpit simulation evaluation, it was noted that in simulated IMC environments some pilots tended to maneuver their aircraft based on traffic advisory information, before the resolution advisories were produced. The level of experience (or training) with the use of the system was deemed inadequate, at this time, to conclude the negative or positive impact of longer term use of the information.

Tests of subject pilots in controlled and operational environment flights in FAA's B-727 continued to find acceptance for the methodology (although not necessarily universal support for the concept) of the traffic advisories. The tendencies were to use the display information to acquire traffic, and to continue to track the target until it was no longer a threat.

As these simulation and operational tests progressed it became clear that comprehensive crew training in TCAS procedures will be essential. By virtue of the extensive involvement of the aviation community in the development and evaluation of procedures and displays, the system has matured from a simplistic maneuver command delivered to the pilot to a comprehensive alerting and resolution system. It is believed that the system more successfully integrates the pilot into the decision making process, doing so in a manner that minimizes the possibility of misinterpretation or misuse of the information, but proper training will be essential.

After more than a decade of development, test and refinement, airborne collision avoidance in the form of TCAS is now ready for evaluation by line pilots in U.S. airspace. While there is undoubtedly some distance to go to achieve the optimum pilot interface, the installation of today's TCAS in air carrier aircraft marks the long awaited beginning of practical airborne collision avoidance system useage.

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Abstract

Bendix, under contract to the Federal Aviation Administration, has developed an airborne collision avoidance system that demonstrates the feasibility of horizontal resolution advisories. This ATCRBS/Mode S interrogator, referred to as Enhanced TCAS II, makes use of top and bottom mounted, eight-element, electronically-scanned circular arrays, which continually search the space surrounding the protected aircraft. A sum and difference beam, monopulse angle-measuring system is described which provides target bearing estimates with an accuracy approaching one degree in the forward direction. Bearing estimates are combined with slant range and altitude to generate precision 3-D target position and velocity. A series of flight tests conducted at the FAA test airport in Atlantic City, NJ have been completed. These tests included airborne angle calibration, as well as actual midair encounters. The Enhanced TCAS II was installed in a Boeing 727, while a Convair 580 served as the target aircraft. A pair of X-band, NIKE beacon trackers were used to acquire precision position reference data on both aircraft. Graphs are presented comparing the NIKE tracker data with that of Enhanced TCAS II. The angle measurements are shown to be of sufficient accuracy that collision can be avoided when a reasonable horizontal maneuver is executed within 25 seconds of a projected collision.

Hardware Configuration

The Enhanced TCAS II interrogator employs a pair of eight-element, 10.5-inch diameter, electronically-steerable circular arrays, which continuously scan the airspace surrounding the protected aircraft. One array is mounted on top of the Boeing 727 test aircraft and the other on the bottom. This provides nearly complete spherical coverage. Transmissions at 1030 MHz are radiated in each of 64 electronically selected beam positions, resulting in 360-degree azimuth coverage for both antennas. Both ATCRBS Mode C and the new Mode S formats are used. On transmit, a difference beam radiates a control signal that effectively "sharpens" the interrogated sector to 22.5 degrees, which represents nearly a 3-to-1 reduction in the 64-degree, half-power sum beam width. The same sum and difference beams are used to receive the 1090 MHz replies from surrounding aircraft. An accurate monopulse receiver provides target azimuth angle with a standard deviation approaching one degree in the forward 180-degree sector and two degrees in the aft 180-degree sector. The target azimuth angle is combined with measured range and reporting altimeter data to establish a three-dimensional track on proximate aircraft. Roll, pitch, and heading of the TCAS-equipped aircraft are used to transform target data coordinates into an earth-referenced, TCAS aircraft centered coordinate system. This permits stabilized target tracks independent of the TCAS aircraft's attitude changes. Update rates on all proximate aircraft are based on threat assessment, the highest rate being about 1 Hz.

Radiating Aperture

The antenna array, pictured in Figures 1 and 2, consists of eight top loaded monopoles on a 10.5-inch diameter circle. Each monopole consists of a circular disc placed 3/4 inch above the ground plane. A microstrip matching network is located at the base of each monopole. A larger diameter radiating element is located in the center of the circular array. This element is for possible future use as the own-aircraft transponder antenna. The nine-microstrip matching networks are printed on a single 0.03-inch thick, Teflon-fiberglass disc. A high temperature resistant, low dielectric constant foam material is epoxy bonded to the microstrip foil to form a rigid core. A rain-erosion coated fiberglass radome encloses the entire assembly. Two rings of mounting holes, shown in Figure 1, secure the antenna to the top and bottom of the Boeing 727. A sealant between the antenna and the aircraft surface prevents air leakage. Nine SMA connectors, within a 5-inch diameter ring, interface each antenna with the electronics inside the aircraft. Figure 2 illustrates the preformed curvature of the antenna ground plane. This curvature matches the 6-foot radius fuselage of the Boeing 727.

Fig. 1 Engineering Model Directional Antenna

Fig. 2 Antenna Array Profile

Electronic Beam-Forming/Beam-Steering Unit

There are two electronic beam-forming/beam-steering units, one for each antenna. Figure 3 shows the 10.5-inch by 8-inch by 15-inch long unit. This unit interfaces the eight-array elements with the interrogator, shown in Figure 4. The unit serves to combine the signals from each of the eight-array elements and simultaneously form sum and difference receive beams. A digital control signal commands a set of seven PIN diode phase shifters, which results in beam steering to any one of 64 equally-spaced angles. The beam-forming/beam-steering unit is reciprocal such that sum and difference beams can also be transmitted. The interrogator transmitter switches between the sum and difference ports in order to radiate the Interrogation Side Lobe Inhibit (ISLI) sequence.

Interrogator RF Unit

Sum and difference beam signals and beam-steering commands are passed from the Interrogator RF Unit, shown in Figure 4, to each of the two Electronic Beam-Forming/Beam-Steering Units. The 7.5-inch by 7.5-inch by 14-inch long interrogator is a modified TRA-65A ATC transponder. It contains all of the transmitter and receiver equipment, including the analog portion of the signal processor.

Digital Signal Processor/Computer/Display/Recording Equipment

The TCAS IIE engineering model includes separately packaged digital signal processing for ATCRBS and Mode S and a microprocessor-controlled computer system, which provides real-time target detection, tracking, and threat assessment. Display and tape recording equipment are also provided for quick-look and off-line data analysis, respectively. No attempt was made to compact this engineering unit. It is anticipated that all RF and digital equipment associated with the interrogator will be packaged in about the same volume as the TRA-65, shown in Figure 4. This does not include the antenna and beam-steering equipment, which will be combined into a small, lightweight integral package.

Antenna Calibration Package

Figure 5 shows the TCAS IIE antenna mounted on a 4-foot diameter, curved ground plane. The curvature matches the fuselage of the Boeing 727. Also shown is the beam-forming/beam-steering unit directly below the aperture.

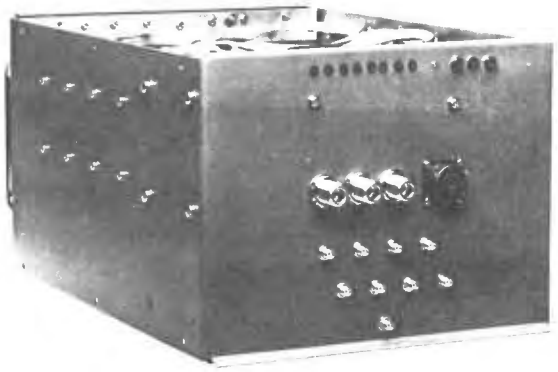


Fig. 3 TCAS Antenna Electronics Package

Fig. 4 Interrogator RF Unit

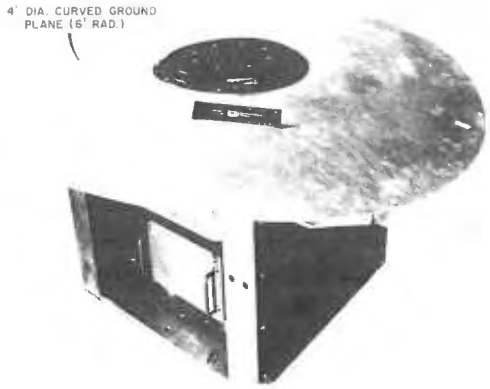


Fig. 5 Eight-Element Circular Array Antenna/ Steering Electronics

Antenna Installation on Aircraft

Figure 6 shows the mounting location of the TCAS IIE antenna on top of the Boeing 727. The bottom antenna is mounted in a similar fashion on the underside of the aircraft.

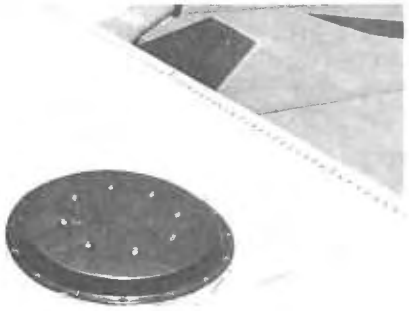


Fig. 6 Directional Antenna Mounted on Top of FAATC's Boeing 727

Interrogate/Reply Modes

Interrogate

Figure 7 illustrates the beam-sharpening technique used to reduce the reply zone of target transponders. The ATCRBS P1 and P3 pulses are transmitted on the attenuated sum beam and the P2 pulse on the difference beam. The effective interrogated zone is about 22.5 degrees when the sum beam is attenuated by 4.5 dB, corresponding to a 3-to-1 beam sharpening. Sum and difference beam pattern shapes prevent punch-through in the back-lobe region.

Use of transmitter beam sharpening reduces the amount of synchronous interference and therefore permits operation in high density airspace.

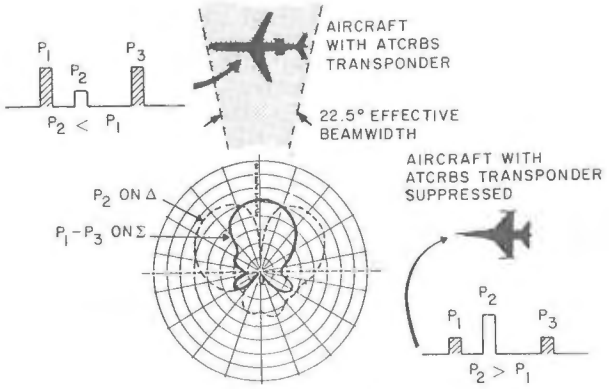


Fig. 7 Interrogate Mode of Operation

Reply

Figure 8 illustrates the receiver side-lobe suppression technique. Sum and difference beam outputs are compared for each target reply. Targets having larger signal strength in the difference beam are not processed. This reduces the signal and data processor work load by eliminating out-of-beam FRUIT replies.

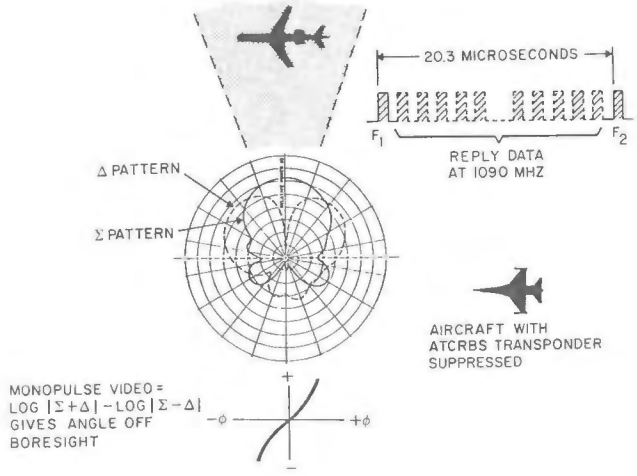


Fig. 8 Reply Mode of Operation

Beam-Forming/Beam-Steering Technique

The beam-forming technique used to produce the nearly orthogonal sum and difference beam patterns is shown in Figure 9, along with the error-free patterns. Details of this Butler matrix feed method were first published by Sheleg [1]. A similar implementation was described by Acoraci [2]. The six-bit phase shifters permit beam steering in 5.625-degree steps.

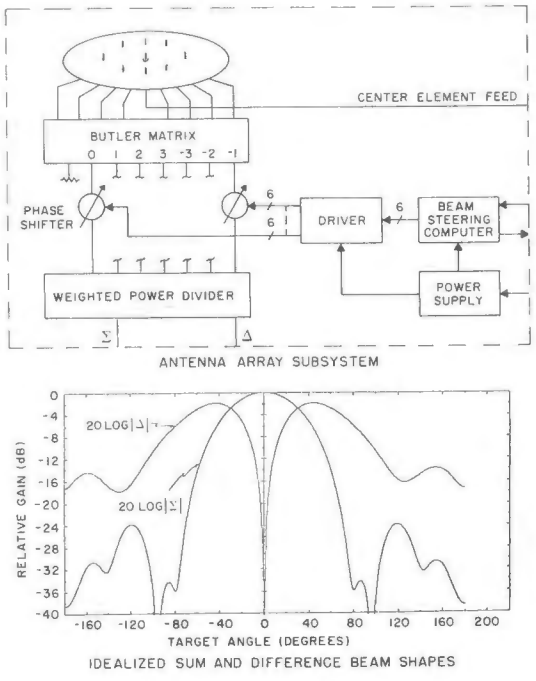


Fig. 9 Beam-Forming/Beam-Steering Techniques

Squinted Beam Monopulse Processor

Target Bearing

Target bearing angle, in antenna coordinates, is estimated using the matched log channels at the top of Figure 10. The sum and difference beams are first converted to a pair of squinted beams at the

four-port hybrid outputs. These squinted beams, graphed in Figure 11a, are then amplified in a matched pair of log amplifiers. The difference between the log channels produces an S-shaped monopulse characteristic in the vicinity of antenna boresight, as noted in Figure 11b. The angle processor is optimum in the sense that the standard deviation in target angle is minimized for a given transponder reply signal-to-noise ratio [3].

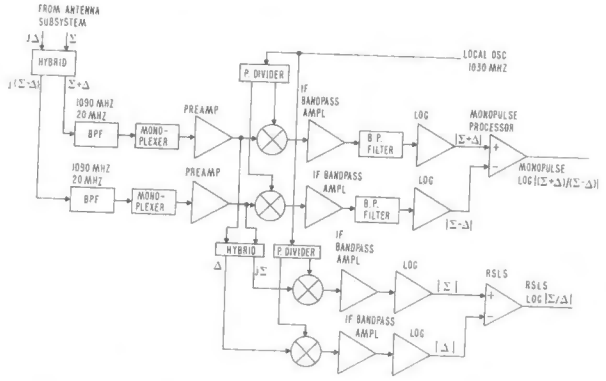
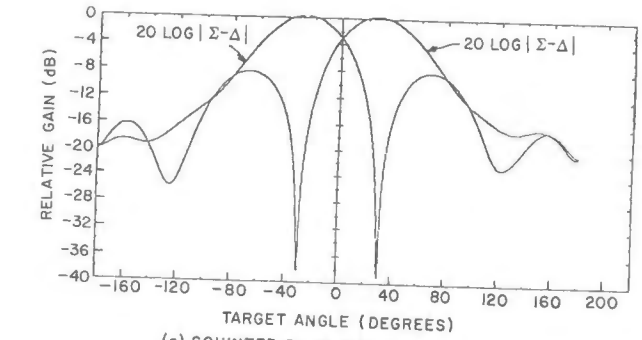
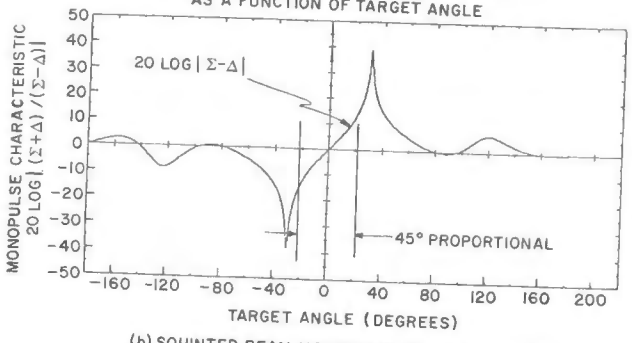


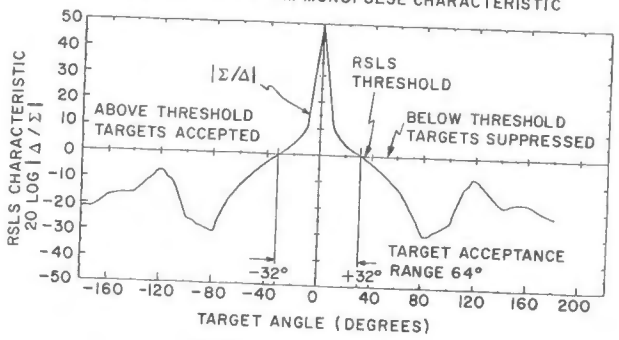
Fig. 10 Squinted Beam Monopulse Processor and RSLS Circuitry



(a) SQUINTED BEAM SIGNAL AMPLITUDE AS A FUNCTION OF TARGET ANGLE



(b) SQUINTED BEAM MONOPULSE CHARACTERISTIC



(C) RSLS CHARACTERISTIC

Fig. 11 Angle Processor Characteristics

RSLS

The lower portion of Figure 10 illustrates the receive side-lobe suppression circuitry. The squinted beams are converted back to sum and difference beams with another four-port hybrid after low noise amplification. The difference of a pair of matched log channels produces the response shown in Figure 11c. Only target replies producing an output voltage above the RSLS threshold are processed. Antenna pattern design is such that only main beam target replies exceed this threshold.

Quantization

Figure 12 illustrates the quantization intervals into which target bearing is estimated. Each of the 64-beam positions has 256 possible angle outputs, separated by 0.176 degree.

Uncompensated Monopulse Characteristics

The relationship between the A/D converted, squinted beam monopulse processor output and target angle is graphed in Figure 13 for each of the 64 beam-steering angles. These monopulse characteristics were measured using the antenna system test configuration of Figure 5.

Angle Calibration

A lookup table was created in the TCAS IIE processor to compensate for the differences between the 64 monopulse curves. Corrrected target angle is obtained by entering the lookup table with beam number (1 to 64) and off-boresight A/D output. The lookup table outputs the corrected angle as one of the 2048 possible values noted in Figure 12.

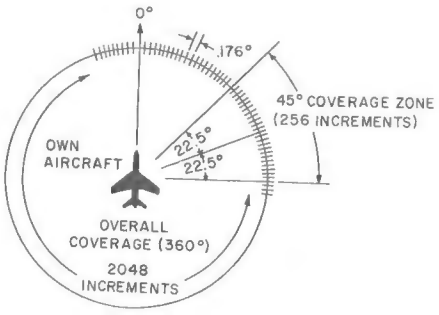


Fig. 12 Segmented Target Angle Coverage

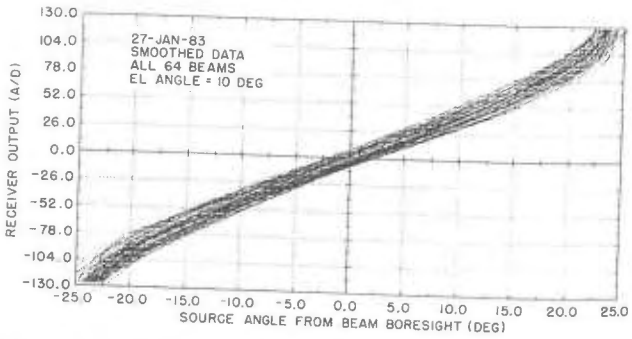


Fig. 13 Uncompensated Monopulse Characteristics

Measured Antenna Patterns

Four-Foot Ground Plane

Figure 14 depicts sum and difference antenna pattern gains for several different elevation angles. Gain characteristics include 4.4 dB of insertion loss in the beam-forming/beam-steering electronics assembly. Maximum gain occurs at about 30 degrees elevation and is nearly 5.5 dB above isotropic for the sum beam. Subtracting the insertion loss of 4.4 dB results in sum beam directivity of 9.9 dB. These antenna patterns were measured using the 4-foot curved ground plane, shown in Figure 5, on a roof-top antenna range at the Bendix facility. The beams were electronically steered to fixed angles and the patterns obtained by mechanically rotating the mount. Patterns were measured and reported for both the sum and difference beams for several different pointing angles [4].

Airport Runway

Figure 15 is a plan view of the Atlantic City airport runways used during the test. A series of antenna patterns were obtained by electronically scanning the sum and difference beams through a probe located at each of the six different locations noted in Figure 15. The probe height was adjusted for maximum signal strength at each of the six locations. Measurements were made using a 1060 MHz, CW signal source at each probe position and graphing the received signal level at the sum and difference ports of the antenna electronics unit. Figure 16 graphs the top antenna's sum and difference patterns measured at probe location 1. Patterns at other probe locations are reported in Reference 5.

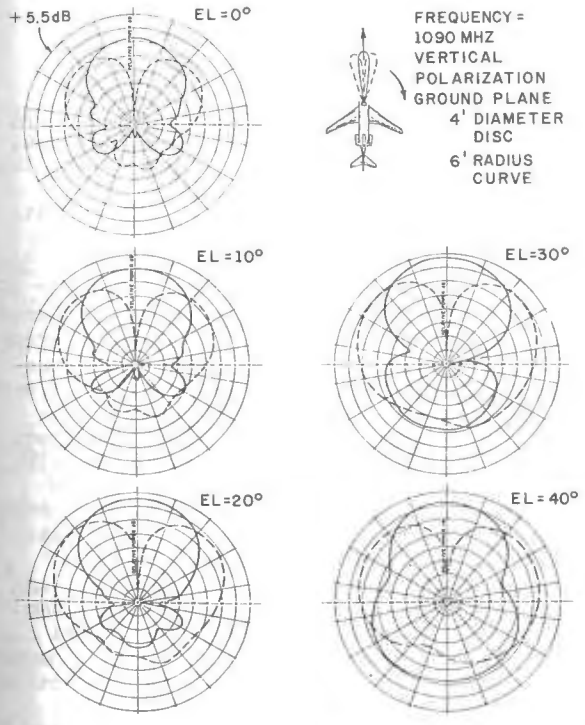


Fig. 14 Antenna Array Subsystem Gain Characteristic, Boresight = 0° AZ

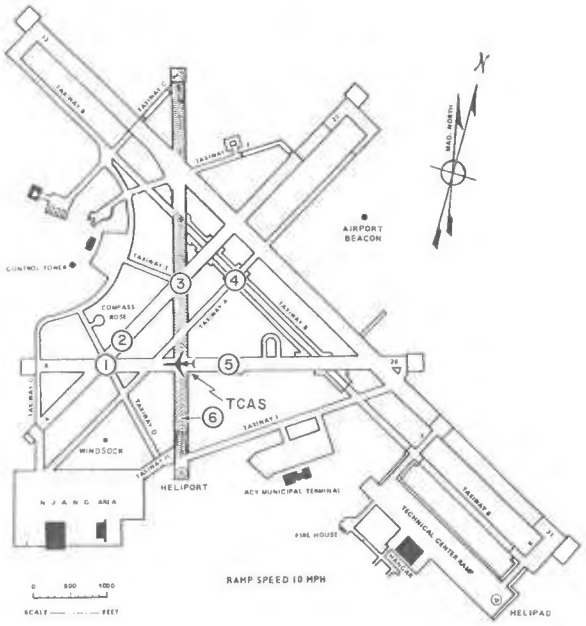


Fig. 15 Technical Center/Atlantic City Airport, New Jersey

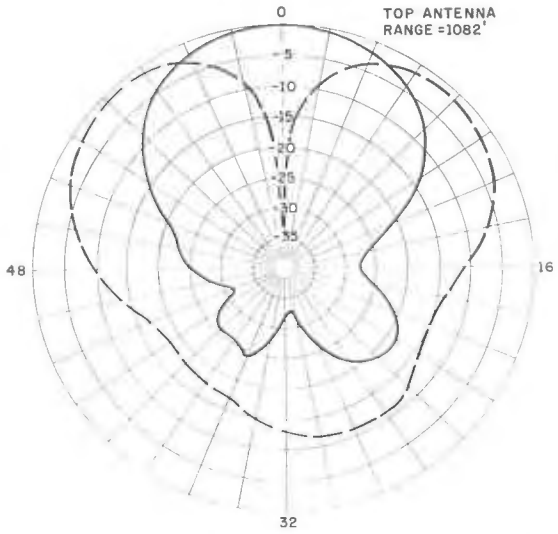


Fig. 16 Airport Surface Pattern Measurements (β = 0°)

Coordinate Transformation

TCAS IIE converts all target reports into an earth-stabilized (locally leveled) aircraft centered coordinate system. This is done so that target tracks are not affected by changes in own aircraft's attitude. The earth-stabilized coordinate system has its X-Y plane normal to the local gravity vector, its positive X axis pointed to true north and its positive Z axis down and parallel to the local gravity vector, as shown in Figure 17. The TCAS IIE measures target bearing, β, in the aircraft's x,y,z coordinate system, along with target slant range and Mode C altitude. The coordinate transformation algorithm makes use of own aircraft's roll (ρ), pitch (θ), and heading (ψ) to perform the necessary coordinate transformations, as reported in Reference 6.

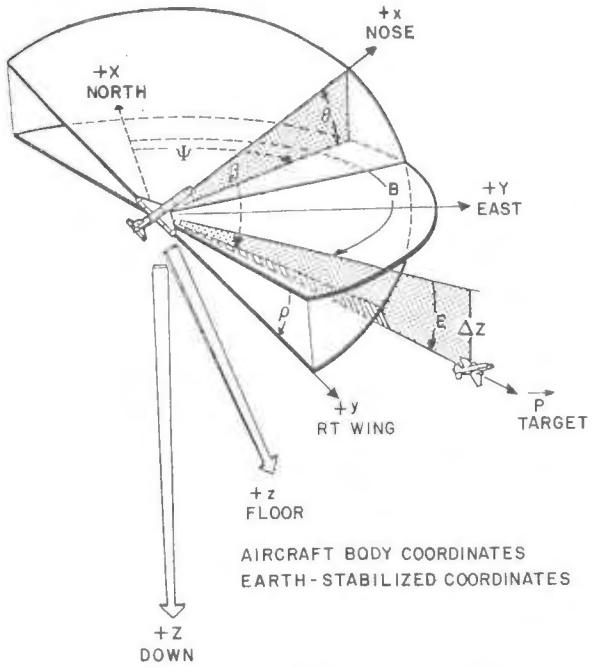


Fig. 17 TCAS IIE Coordinate Transformation

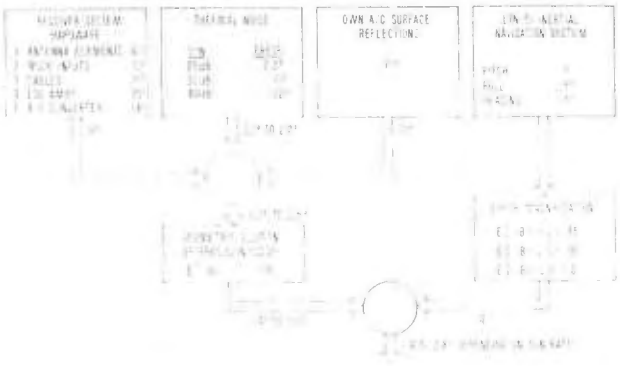


Fig. 18 Absolute Angle Error Summary

Error Analysis

During the design phase, a detailed error analysis was completed to assess the feasibility of horizontal collision avoidance maneuvers. Of primary concern was the bearing rate error, which translates directly into miss distance estimation error.

Angle Error

Figure 18 tabulates the error sources which contribute to the coordinate transformed bearing angle (B) error. The estimated RMS error is seen to be between 1.4 degrees and 2.8 degrees, depending on transponder reply signal-to-noise ratio. The estimated errors, noted in Figure 18, are on a per-reply basis and do not include the effects of the alpha-beta filters which are applied to the transformed X-Y coordinates.

Angle Rate Error

Figure 19 tabulates the error sources that contribute to the coordinate transformed target bearing angle rate (dB/dt) error. Only the standard deviation of bearing error about the mean is important because it is directly related to the error in estimating target miss distance relative to the protected aircraft [7]. Bearing rate errors are appreciably reduced by the alpha-beta filter, as noted in Figure 19. Both random errors and cyclic errors due to surface reflections were considered in the error estimation process. Choice of optimum filter constants is reported in Reference 8. Bearing rate error was estimated between 0.081 and 0.26 degree/second, depending on input signal-to-noise ratio.

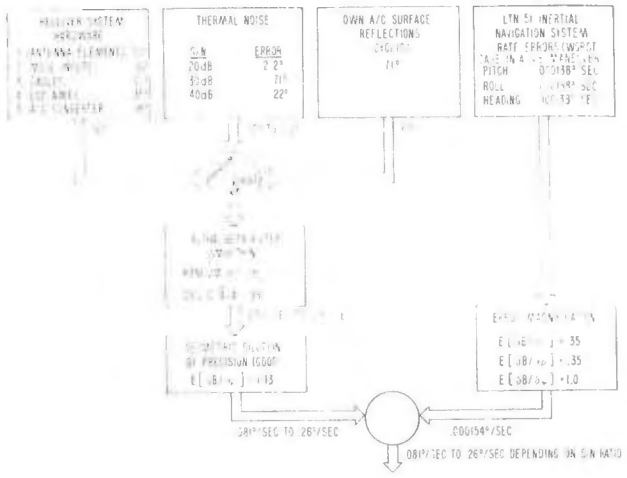


Fig. 19 Angle Rate Error Summary

Performance Testing

A series of flight tests was conducted at the FAA's Atlantic City Test Airport. A pair of precision, NIKE, X-band beacon trackers was used to track the Boeing 727 TCAS IIE-equipped aircraft and the Convair 580 target aircraft. Radar tracking data and coordinate converted TCAS IIE data were acquired simultaneously and recorded on magnetic tape, as noted in Figure 20. Time tagged radar and TCAS IIE data were then post-processed to evaluate TCAS IIE performance. The tracking radar accuracy, coupled with the selected geometry of the encounters, was such that the instrumentation errors were generally less than one-tenth of the expected TCAS IIE angle errors. Two types of flight tests were conducted. The first type involved orbiting the target aircraft at a constant altitude and range about the TCAS IIE aircraft while both were airborne. This test assessed angle coverage and accuracy at various target elevation angles completely around the TCAS IIE aircraft. Top and bottom antennas were both exercised. The second type of test involved straight line encounters between TCAS IIE and the target aircraft. A number of different encounter angles and relative closing velocities were tested. The purpose of these encounters was to determine whether TCAS IIE could accurately predict miss distance 25 seconds prior to closest point of approach.

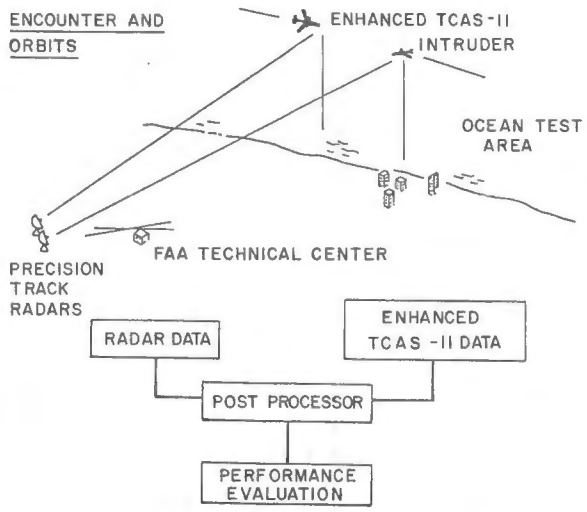


Fig. 20 Performance Testing

Analytical Model

Figure 21 summarizes the evaluation procedure used to determine angular accuracy of the TCAS IIE. Measurements of target altitude, bearing angle, and slant range are taken in the airframe coordinate system and then, using roll, pitch, and north heading, converted to an earth-stabilized system. The raw, coordinate converted, TCAS IIE target data are then stored on magnetic tape with real-time tags. The tracking radar data are simultaneously stored on magnetic tape in the form of latitude and longitude. The TCAS IIE data are taken at a 1 Hz rate, while the radar data are taken at 10 Hz.

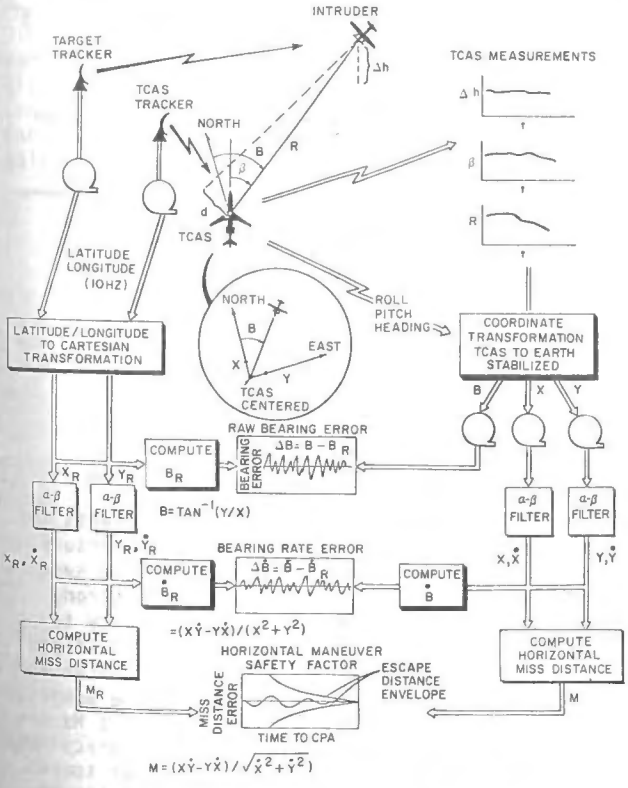


Fig. 21 Evaluation of Enhanced TCAS II Angle Accuracy

Raw Bearing Error. Unfiltered radar and TCAS IIE earth-stabilized angle data are compared. Both are graphed, along with their difference. Because the radar data are assumed to be 10 times more accurate than TCAS IIE, the difference graph is defined as the absolute TCAS IIE angle error.

Bearing Rate Error. The alpha-beta filtered TCAS IIE and radar data are compared. Graphs of measured bearing rates and bearing rate difference are generated. The alpha-beta filters used on the radar data have considerably more bandwidth than the implemented TCAS IIE filters. Any lag problems associated with the TCAS IIE filters would therefore be apparent from the comparison.

Horizontal Maneuver Safety Factor. The projected miss distance between the TCAS IIE and target aircraft is computed as a function of the smoothed X-Y coordinates and their first derivatives, using the equation noted in Figure 21. This computation assumes both aircraft are in straight line, non-accelerating motion. The miss distance prediction is computed by the tracking radar instrumentation system, as well as the TCAS IIE. The difference between the two predictions is graphed as the miss distance error. An escape distance envelope is also superimposed on the miss distance error graphs. This envelope represents the horizontal separation that can be achieved if the pilot makes a 45-degree banking maneuver at the time noted before closest point of approach (CPA). If the escape maneuver results in a separation considerably larger than the TCAS IIE miss distance estimation error, then collision avoidance is assured.

Test Results

Angular Coverage. Figure 22 summarizes the mean angular error (bias) of TCAS IIE and the standard deviation about the mean. The data were acquired by flying the Convair 580 in nearly constant radius orbits around the airborne TCAS IIE.

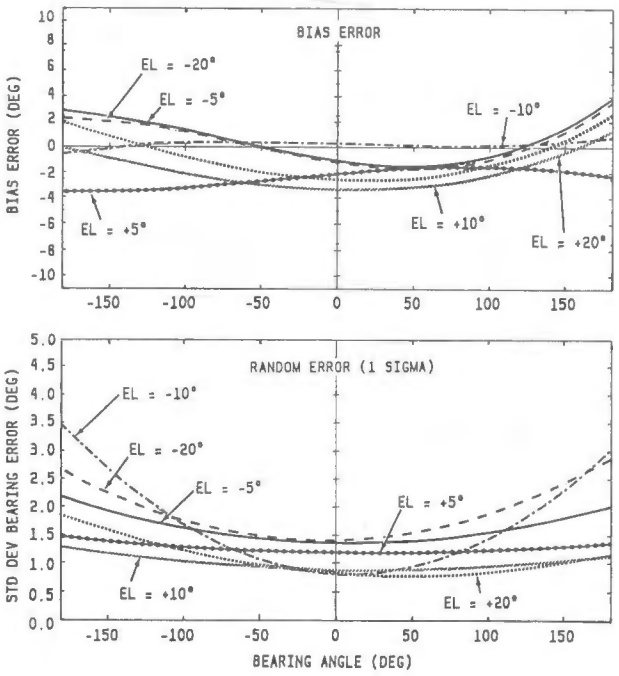


Fig. 22 Angular Coverage Performance

Target elevation angles from -20 to +20 degrees elevation were flown. The data reduction method illustrated in Figure 21 was used. Bias errors vary from +4 to -4 degrees as the target flys around TCAS IIE. Bias errors do not affect miss distance estimation, provided that they do not vary rapidly with time or angle. Standard deviation of the angle estimate translates into miss distance estimation errors. Values range from 1.0 degree in the nose direction of the TCAS IIE aircraft to 3.5 degrees in the tail direction.

Encounter Performance. Figure 23 illustrates bearing and bearing rate accuracy of TCAS IIE for a 340-knot closing speed encounter where the target aircraft was at a 90-degree bearing angle relative to the TCAS IIE aircraft's nose direction [9]. Radar data are presented as a solid curve, while TCAS IIE data are illustrated by discrete points with approximately one-second spacing. For the particular encounter graphed, absolute RMS angle error is 0.69 degree averaged over the 40-second period preceding CPA. The corresponding bearing rate error is 0.166 degree/second.

Figure 24 illustrates a head-on encounter model used to show the relationship between horizontal acceleration and miss distance error. As long as the error in estimating miss distance is smaller than the aircraft's ability to outmaneuver that error, a safe horizontal maneuver is possible. Typically, peak miss distance error should be 1/2 to 1/3 of the achievable horizontal displacement of the aircraft in the available escape time. The approximate relationship between bearing rate error and miss distance error is presented.

Figure 25 illustrates one of several encounters performed during the test series [9].

Achievable horizontal separation of the TCAS IIE and target aircrafts is seen to be considerably greater than the TCAS IIE predicted miss distance errors. The radar predicted miss distance indicates a nearly perfect horizontal collision course (a 300-foot vertical separation was inserted). The TCAS IIE predicted miss distance oscillates slightly and becomes quite small at 25 seconds to CPA. The difference between radar and TCAS IIE predictions is defined as the miss distance prediction error.

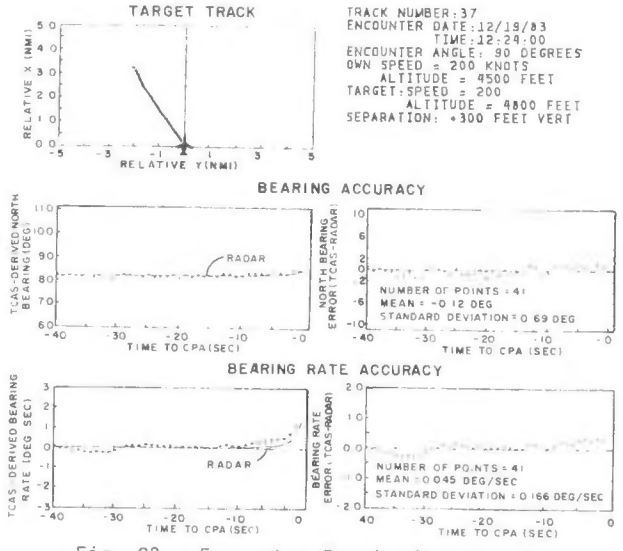


Fig. 23 Encounter Bearing/Bearing Rate

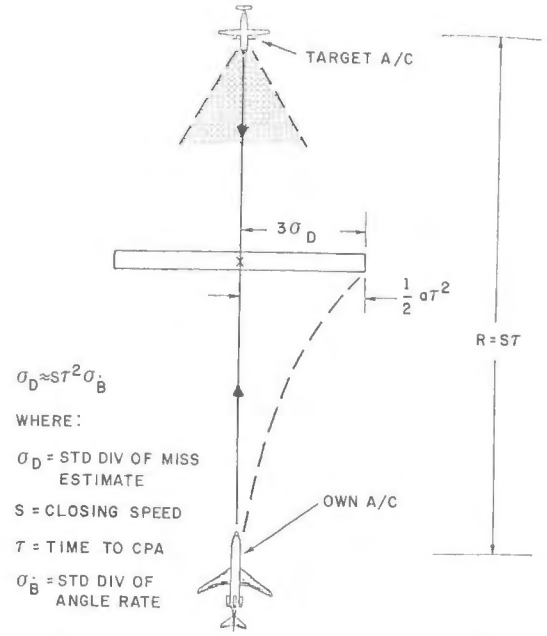


Fig. 24 Horizontal Maneuver to Miss

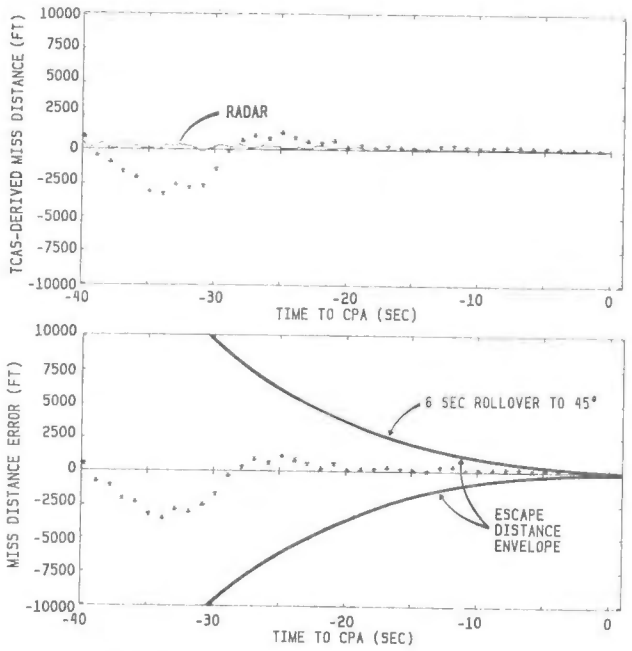


Fig. 25 Encounter Miss Estimation

TCAS IIE Angle Measuring Specification

Figure 26 summarizes the accuracy requirements for an airborne collision avoidance system to ensure that horizontal maneuvers will provide safe separation. The requirements are seen to be a strong function of the protected aircraft's ability to maneuver. One-degree accuracy is required if protection against a head-on, 1200-knot encounter is required and a 45-degree bank angle can be achieved in 6 seconds. Data rates on the order of 1 Hz are required. Corresponding bearing rate accuracy must be about 0.1 degree/second. For encounter speeds of 600 knots, the accuracy requirements relax to 2 degrees and 0.2 degree/second, respectively, for the head-on encounter.

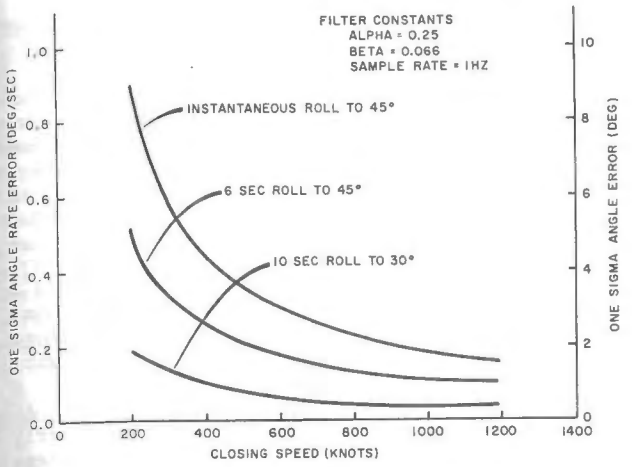


Fig. 26 Enhanced TCAS II Angle Specification

Conclusions

Test results confirm the predicted angle and angle rate accuracies of TCAS IIE. Based on measured results, feasibility of a horizontal maneuver to avoid midair collisions is substantiated. An angle-measuring system with one- to two-degree precision is required where high speed encounters must be accommodated.

Acknowledgment

Enhanced TCAS-II development was performed for the FAA under Contracts DTFA01-81-C-10041 and DTFA01-82-C-10019. The project is under the management of Dr. Clyde Miller. Particular thanks is given to Mr. Carl Jezierski of the FAA Technical Center, who was project manager for testing the Enhanced TCAS II, and who has had the patience to help reduce much of the radar and TCAS IIE data.

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NEW CONCEPTS IN COLLISION AVOIDANCE LOGIC

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Abstract

Airborne collision avoidance logic is being developed to take advantage of the accurate bearing measurements provided by the Enhanced TCAS II system. This system issues horizontal and vertical resolution advisories, and should give fewer unnecessary alarms than earlier systems. Design tradeoffs and new techniques are described for threat detection, modeling of potential escape maneuvers, and the selection of resolution advisories. Plans for further development and evaluation are described.

Introduction

An airborne collision avoidance system now under development is the Enhanced Traffic Alert and Collision Avoidance System II, or Enhanced TCAS II. Sponsored by the Federal Aviation Administration, this system is intended to provide civil aviation with an independent on-board system that serves as a backup to ground-based Air Traffic Control (ATC) in providing protection from midair collisions. Enhanced TCAS II has much in common with the Minimum TCAS II system (1, 2), but the Enhanced system is intended to provide improved performance and extended capabilities by utilizing highly accurate bearing measurements and adaptive sectorized interrogations (3). The extended capabilities include the ability to provide horizontal Resolution Advisories. (By contrast, the Minimum TCAS system can only recommend resolution maneuvers in the vertical plane.)

The design and development of the collision avoidance algorithms for Enhanced TCAS II, a responsibility of the MITRE Corporation, builds upon the expertise gained from the extensive development program for Minimum TCAS II (4) and from similar efforts for ground-based collision avoidance systems. The increased bearing accuracy and other new features of Enhanced TCAS have led to the development and use of a number of new concepts in airborne collision avoidance logic. This paper discusses the specific design features that are unique to the Enhanced TCAS collision avoidance logic, the potential benefits expected, and some of the areas for which testing and evaluation will support decisions concerning design tradeoffs.

Expected Benefits

Enhanced TCAS II is being developed to take advantage of highly accurate bearing data. With this important advance over Minimum TCAS II, the collision avoidance algorithms are designed to produce two principal benefits:

1. The use of the accurate horizontal information enables the algorithms to be more selective in distinguishing threatening intruders from safe traffic. Minimum TCAS II uses a warning time ("tau") criterion based on slant range. Its warning threshold is set from 20 to 30 seconds before closest approach (the value varying according to flight regime and airspace). A characteristic of a high-speed encounter is that the computed tau values are nearly identical for a collision and a safe passage until the last few seconds; however, TCAS cannot wait that long, if it is to give the pilot enough time to escape. Therefore, the use of a horizontal filter provides the Enhanced system with another criterion to reduce this kind of unnecessary alarm.

2. Resolution Advisories are given in both the horizontal and the vertical plane. Since the Minimum system gives ample warning to escape virtually any reasonable collision threat, this flexibility is needed not so much for the basic function of protection, as for operational considerations. Depending on encounter geometries and other factors, it may be preferable to resolve some encounters vertically and others horizontally. An obvious example is a conflict between two aircraft close in altitude which can be resolved by Enhanced TCAS II with a preventive advisory (e.g., "don't turn left"), but for which the vertical-only Minimum TCAS would require a maneuver (e.g., "climb").

Functional Design Tradeoffs

The design of a collision avoidance logic is necessarily a compromise between conflicting factors. Several of the principal design tradeoffs are discussed below.

Protection Vs. Alarm Rate

Ideally, the logic should always detect genuine impending collisions, for all possible geometries. Also, the pilot should be given a generous warning time so that he may assess the situation and perform the escape maneuver. The logic should never issue an alarm when it is not needed for safe separation.

These ideal requirements conflict because the logic is unable to consider pilot and controller intentions. Thus, most seeming collision courses are either resolved by maneuvers as the aircraft approach, or turn out to already have safe separation. The latter case is difficult for TCAS to identify far in advance because of the limitations of its measurements.

The solution to this tradeoff is reached by making the alarm time as short as possible, and yet allowing enough time for the escape maneuver. This method greatly reduces unnecessary alarms. A flexible approach to setting the alarm time is discussed later.

Protection Vs. ATC Consequences

In addition to the disruptive potential of unnecessary alerts, other ATC consequences could result from a design that causes excessively long maneuvers. Deviation from a clearance, loss of separation from a third aircraft, and possibly inducement of an alarm in that third aircraft's own TCAS (a "domino" effect) are concerns. Therefore, a tradeoff is desired that can offer protection from collisions without generating frequent or large deviations in flight path. The use of "preventive" advisories is desirable, to ensure that adequately separated aircraft (in terms of avoiding a collision) do not rapidly become endangered by a wrong maneuver.

Protection Vs. Operational Preference

Collision avoidance logic could be designed to always select the maneuver that would generate the largest separation; however, such a choice could be inconvenient compared to another maneuver that also would avoid the collision. To achieve operational acceptance of the system, it is believed necessary to account for operational considerations and give these factors significant weight. For many encounters, several maneuver choices can provide adequate separation. In such cases, operational considerations should take priority over the choice that would simply maximize separation. Naturally, for a safe encounter, the most desirable choice would be to give no Resolution Advisory at all, since this allows normal operations to proceed without interference.

New Approaches

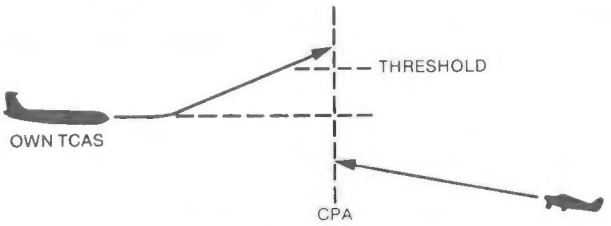
In the Enhanced TCAS system, several new approaches are being employed in the areas of conflict detection and Resolution Advisory selection. These include the "variable threshold" concept for detection and the use of a multi-criteria test sequence for evaluating candidate Resolution Advisories. These functions are supported by new algorithms for modeling potential escape maneuvers in three dimensions.

"Variable Threshold" Conflict Detection

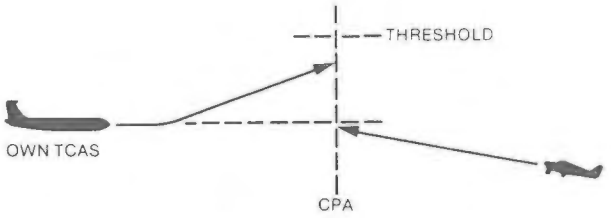
As with Minimum TCAS II, the detection of conflicts in Enhanced TCAS II is based upon the predicted time to closest approach, derived by dividing measured range by the range rate estimate. The time test is augmented with an altitude test to avoid generating alarms when safe vertical passage is predicted. The system also uses a horizontal plane projection, unique to Enhanced TCAS, to avoid alarms in a similar manner for safe horizontal passage.

"Variable threshold" logic is a new concept used in the Enhanced TCAS system for the detection of conflicts. Under this concept, fixed time thresholds are replaced with a variable alarm time, one which is appropriate to the geometry of the encounter. An alarm is deferred as long as possible, since studies show that most apparent conflicts are safely resolved either by Air Traffic Control or pilot visual procedures. Also, the effects of measurement errors from bearing and altitude rate decrease at smaller range. An alarm is finally given when further delay might cause a standard escape maneuver to produce insufficient separation at the point of closest approach. Traffic Advisories help prevent blunders before a Resolution Advisory is issued, and also prime the pilot for quick reaction by removing the element of surprise.

Figure 1 illustrates the "variable threshold" concept for a vertical escape. In Figure 1a, a certain amount of vertical separation already exists at the projected point of closest approach. As a result, the projected separation which can be achieved with a "climb" advisory (the best choice of vertical maneuvers) exceeds a specified threshold (a system parameter). The collision avoidance logic therefore decides that resolution can be deferred. The rationale is that for many encounters of this type, separation will increase and the TCAS advisory will not be needed. In Figure 1b, the two aircraft are more nearly on a collision course. This causes the projected separation for a "climb" advisory to fall below the threshold value. In this case, resolution cannot be deferred. The "variable threshold" design thus takes advantage of any existing miss distance (projected separation at the point of closest approach) in order to delay the issuance of Resolution Advisories. Note that Figure 1 illustrates this concept only for vertical maneuvers; in actuality, the logic evaluates both vertical and horizontal maneuvers for their potential separation.



(a) Resolution Can Be Deferred.



(b) Resolution Cannot Be Deferred.

FIG. 1 "Variable Threshold" Detection Concept

Resolution Advisory Selection

The selection of a Resolution Advisory (RA) for a conflict is made by considering a list of test criteria. As the criteria are evaluated, the list of potential advisories is reduced until only one choice remains, as illustrated in Figure 2. The test criteria combine both predicted separation and operational considerations according to appropriate

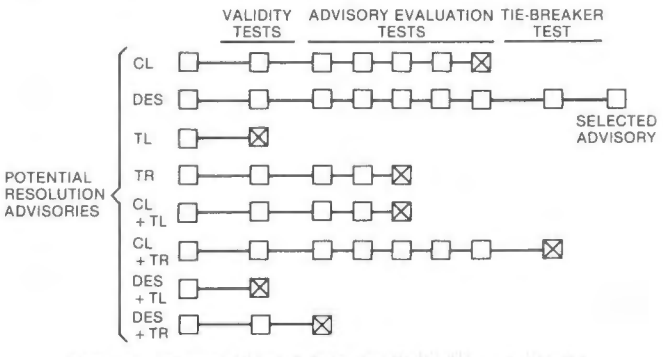


FIG. 2 Resolution Advisory Selection Process

priorities. This method is used because often more than one advisory will provide satisfactory separation, so that consideration can safely be given to operational factors. This modular approach also has the advantage of being easy to understand, analyze, test, and modify.

Table 1 lists many of the advisory evaluation criteria. These criteria consider a number of factors, including projected separation, relative confidence in the projection for each plane, the desirability of various maneuvers from an operational standpoint, deviation from the intended flight path, and efficient use of resolution dimensions.

Evaluation Test	Function
Good 3-D Separation	Favor RAs which provide 3-D separation greater than a threshold value.
Compatibility with Threat RAs	If the threat is TCAS-equipped, favor RAs which are compatible with the threat's displayed RAs, if any.
Negative Suffices	Favor any single-dimension RAs for which negative strength suffices.
Same Plane as Threat	If the threat is equipped with Minimum TCAS, favor RAs with a vertical component. If the threat is equipped with Enhanced TCAS and has indicated a single-dimension RA, favor RAs with a component in the same dimension selected by the threat.
Unequipped Threat with Large Vertical Rate	If the threat is not TCAS-equipped and has a high vertical rate, favor RAs with a horizontal component.
Double Dimension RA Needed	Favor double-dimension RAs if the situation is critical. Otherwise, favor single-dimension RAs.
Superior 3-D Separation	Favor RAs which provide 3-D separation greater than a fixed fraction of the best 3-D separation available.
Reinforcement of Existing RA	If a single-dimension RA is already being displayed to the pilot, favor any single-dimension RA which reinforces the existing RA.
Good Separation in Plane of Resolution	Favor RAs which provide separation greater than a threshold in the plane of resolution (either plane for double-dimension RAs).
No Reversal of Existing Maneuver	If own aircraft is currently executing a maneuver (a significant turn, climb, or descent), favor RAs which do not reverse the existing maneuver.

TABLE 1 Advisory Evaluation Criteria

Modeling of Aircraft Flight Paths

The separation achievable with various escape maneuvers is estimated by modeling the potential maneuvers in three dimensions. The intruder is projected ahead on an unaccelerated path using the current 3-D velocity estimate. A number of different flight paths are modeled for own aircraft. Each path simulates a standard response in compliance with a different one of the available Resolution Advisories. For each of these paths, the point of closest approach may be reached at a different time. When this point is found, the 3-D separation and its vertical and horizontal components are stored in a matrix. This is depicted in Figure 3.

Once the predicted miss distances have been computed by the modeling algorithms, the values in the matrix are reduced to allow for the possibility of an adverse error in surveillance measurements and in the resulting projected paths. The horizontal error budget is based upon the accuracy with which bearing rate can be estimated, and the error allowance is a function of range and range rate. The vertical error budget is based upon the accuracy with which vertical rate can be estimated, and is a function of the time to closest approach and confidence in the tracked vertical rate. The predicted miss distances derived from modeling each maneuver option are used in both the detection and resolution algorithms.

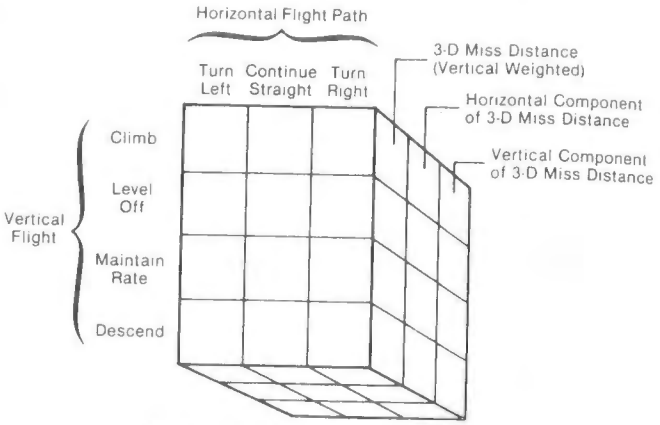


FIG. 3 Predicted Separation Matrix

Detailed Design Tradeoffs

The design of a three-dimensional collision avoidance logic presents a number of unique tradeoffs to the designer. Some of the more interesting ones are:

1. In choosing between horizontal and vertical Resolution Advisories, how much separation in the horizontal dimension should be considered equivalent to a specified amount in the vertical dimension?
2. Since late alarms require stronger maneuvers to achieve a given amount of separation, how long can Resolution Advisories be delayed?
3. How accurately must aircraft flight paths be modeled, since greater accuracy will produce a greater computational burden for TCAS?
4. In selecting Resolution Advisories, how are the various selection criteria balanced in importance against each other and against projected separation?

These design tradeoffs are described in more detail below.

Horizontal Vs. Vertical Separation

In a single plane of resolution, it is easy to compare the separation distances predicted for two different escape maneuvers — the larger separation distance indicates the more effective maneuver. In a system with two resolution planes, however, some basis must be established for comparing distances in the vertical plane to distances in the horizontal plane. For instance, almost anyone would agree that a miss distance of 500 feet vertically is much better than a miss distance of 500 feet horizontally. However, which is better: a miss distance of 300 feet vertically or 1800 feet horizontally? The picture becomes even more cloudy when comparing 3-D miss

distances containing both horizontal and vertical components.

The comparison of horizontal and vertical distances comes down to the selection of a single number — a weighting factor to multiply vertical distance for comparison with horizontal distance. The selection of such a vertical weight is a somewhat subjective task which must take a number of factors into account, including the following:

1. the accuracy with which miss distances can be estimated in each plane,

2. the general feeling of pilots as to what constitutes "safe" passage in each dimension (note that the separation to be attained in avoiding a collision is much less than the standard ATC separation),

3. the ability to maneuver in each dimension, and

4. typical aircraft dimensions.

In the Enhanced TCAS collision avoidance logic, vertical distances are weighted 5:1 for comparison with horizontal distances. This vertical weighting factor has been developed during years of design work in collision avoidance systems. 3-D (slant range) distances are compared by multiplying the vertical component by 5 before combining it with the horizontal component. Experience with this value has not shown it to cause any significant bias toward either horizontal or vertical advisories.

Timing of Alarms Vs. Maneuver Strength

As was indicated earlier, delaying alarms as long as possible means fewer unwanted alarms and allows more accurate estimates of separation. Because of the delay, however, the Resolution Advisories which are issued will call for stronger maneuvers, on the average, than would otherwise be the case. Thus, a larger percentage of the advisories could be expected to be positive advisories (e.g., "turn left") as opposed to negative advisories (e.g., "don't climb") and vertical speed limits (e.g., "limit climb to 500 ft/min"). It should also be noted that in the horizontal plane, a positive Resolution Advisory issued later will often result in a greater deviation from the intended course than if resolution had not been deferred.

In the Enhanced TCAS logic, the timing of Resolution Advisories is controlled by the setting of several "miss distance" thresholds. Two thresholds, a "large" threshold and a "small" threshold, are chosen for each resolution plane. The values of the thresholds are set according to the current sensitivity level, which depends upon the phase of flight. If the projected separation for any single escape maneuver exceeds the appropriate "large" threshold, then resolution is deferred. Also, if the projected separation for any two of the available maneuvers exceeds the "small" threshold, resolution is also deferred. Otherwise, a Resolution Advisory can no longer be deferred and is issued immediately.

The actual values of the thresholds are system parameters. They must be small enough to avoid unwanted alarms without the risk of delaying a valid alarm unnecessarily. They must also be large enough to provide some flexibility in the actual selection of a Resolution Advisory (i.e., it is not intended that the alarm be delayed so long that the system is left with only a single choice of escape maneuvers).

Modeling Accuracy Vs. Computational Burden

In the Enhanced TCAS system, the modeling of aircraft flight paths has proven to be one of the principal computational burdens. As many as twelve different 3-D flight paths must be modeled for own aircraft in order to represent all single and double-dimension advisories. Each path must be combined with the projected track of each potential threat to determine the point of closest approach. These paths must be projected up to 55 seconds into the future.

For purely vertical maneuvers, the equations predicting separation as a function of time are essentially linear and can be solved directly. However, when horizontal maneuvers are added, the computation of miss distances becomes a more difficult problem. The separation equations for maneuvers which include a constant-radius turn are transcendental and have no simple solution. In fact, more than one relative minimum may occur within the time period of interest.

Several methods have been considered for estimating the point of closest approach for the various escape maneuvers. These include stepwise modeling, where the aircraft are projected ahead in fixed increments of time, iterative solution of the actual equations for separation, and direct solution of simpler equations which approximate the actual equations.

Regardless of the method chosen, a general tradeoff must be made: the greater the computational accuracy achieved, the longer the solution takes and the greater the computational burden. In making this tradeoff, it must be remembered that computational inaccuracy is only one source of error. There are other random variables which introduce uncertainty into the flight path projections. These include surveillance and tracking errors, variations in pilot response time, and variations in the strength of the executed maneuver. Computational error need not be a great deal less than the errors introduced by these other factors, most of which are beyond the control of the system designer.

Weighing the Advisory Selection Criteria

In the process of selecting a Resolution Advisory, many tradeoffs must be addressed. Each criterion that is used to evaluate potential maneuvers must be weighed in importance against each other criterion and against projected separation. In the Enhanced TCAS logic, these tradeoffs are made in two ways:

1. by the selection and ordering of tests in the advisory evaluation test sequence, and

2. by the selection of thresholds used to determine whether a specific advisory passes a given test.

The advisory evaluation test sequence selects the best resolution advisory by the process of elimination. The tests in the sequence are ordered by decreasing priority; each test takes precedence over those that follow it. Thus, if at least one advisory passes the first test, then those advisories which do not pass the test are eliminated from further consideration; succeeding tests gradually narrow the choices to a single advisory. Various tests based upon predicted separation are

distributed throughout the test sequence; in this way, the value of predicted separation is balanced against the importance of other factors.

Figure 4 illustrates a typical tradeoff in the selection of Resolution Advisories. The figure shows a conflict caused by own aircraft turning in front of another aircraft. In this scenario, we face the conflicting objectives of not reversing a pre-existing maneuver while still providing good separation. In the Enhanced TCAS logic, this situation would be resolved by two advisory evaluation tests: a test which favors not reversing the maneuver, preceded by a test which does not allow more than 1/3 of the available separation to be given up for other considerations. Thus, in this particular geometry, a "turn right" advisory for own aircraft (reversing the existing turn) provides a great deal more separation than a "turn left" advisory (reinforcing the existing turn) and effectively eliminates "turn left" from further consideration. However, if a vertical Resolution Advisory is available which provides good separation, then the vertical advisory would be selected, as it satisfies both objectives.

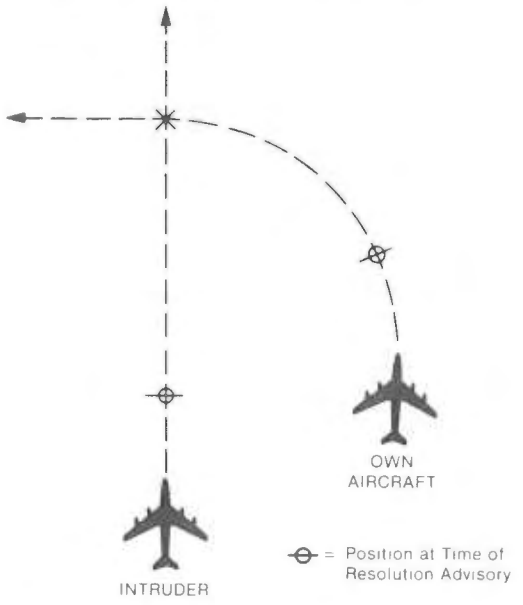


FIG. 4 Conflict Caused by Own Aircraft Turning

Taking Advantage Of Two Resolution Planes

A three-dimensional collision avoidance system inherently provides a great deal of flexibility in resolving aircraft conflicts. The second resolution plane can be exploited to handle situations which are very difficult to resolve with only one resolution plane. Examples of such situations are maneuvering intruders, multiaircraft encounters, and slow pilot response to a Resolution Advisory. The Enhanced TCAS logic includes specific features to recognize and deal with each of these situations.

Maneuvering Intruders

Figure 5 illustrates how a last-minute maneuver by an intruder can foil a collision avoidance system with only one resolution plane. In this conflict, an intruder with a high vertical rate appears as if it will pass below own aircraft (Figure 5a). If own aircraft is equipped with a vertical-only TCAS, then a "climb" sense advisory is likely to be selected against the intruder. However, if the intruder unexpectedly levels off at about the time TCAS selects its Resolution Advisory, as shown in Figure 5b, then the directional sense chosen by TCAS may be completely invalidated.

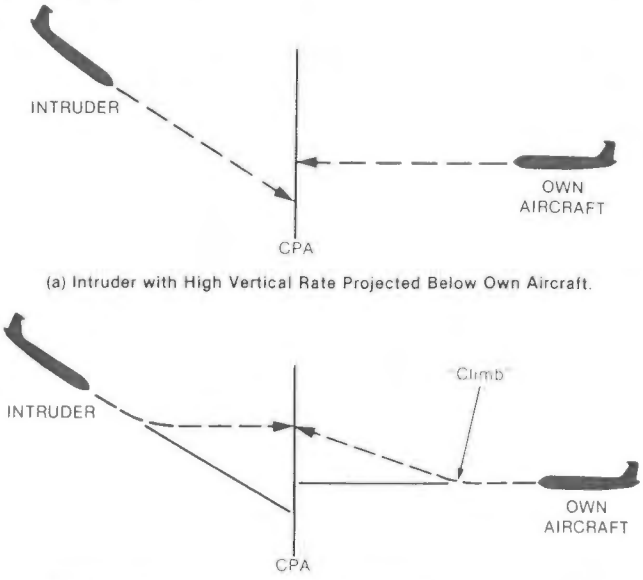


FIG. 5 Conflict Involving Vertical Maneuver by Intruder

The resolution logic of Enhanced TCAS contains specific features for dealing with maneuvering intruders. These features are designed to handle an intruder maneuvering in either dimension by making use of the alternate resolution plane. In the example given above, the Enhanced TCAS logic would recognize that the vertical rate of the intruder and the details of the encounter geometry make vertical resolution highly susceptible to a vertical maneuver by the intruder. In this case, therefore, Enhanced TCAS would initially favor a horizontal escape maneuver.

In addition, the ability to change the plane of resolution during a conflict provides a general method to cope with unexpected adverse maneuvers of any kind. It is always true that an intruder with sufficient performance can foil the TCAS escape, for any geometry. The change of resolution plane gives TCAS a "second chance".

Multiaircraft Encounters

Analysis of recorded air traffic surveillance data has shown that multiaircraft encounters would be very rare for a collision avoidance system, such as TCAS, that uses small alarm thresholds. When such encounters do occur, however, a three-dimensional system can deal with them much more effectively than can a vertical-only system.

Figure 6 illustrates a multiaircraft encounter which a vertical-only TCAS system handles in less than an ideal manner. In this figure, TCAS selects a "descend" sense advisory against the first threat, which is above own aircraft. The second intruder, flying at a lower altitude, is declared a threat a few seconds later. Because of the geometry, TCAS may be forced to select a "climb" sense advisory against the second threat. TCAS must therefore display a

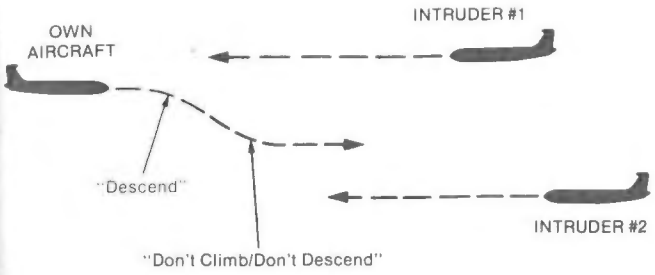


FIG. 6 Multi-Aircraft Conflict

"double negative" advisory ("don't climb/don't descend") against the two threats when a positive-strength advisory is preferred against at least one of them. TCAS would thus be "threading a needle" in the vertical dimension and would be highly susceptible to adverse maneuvers by either intruder.

In a multiaircraft situation, Enhanced TCAS may choose either the same resolution plane or a different resolution plane for the second threat. If the projected separation against the second threat is sufficient, Enhanced TCAS will use the same resolution plane in order to minimize deviation from the intended flight path and to conserve resolution dimensions. If flight path projections show that the same resolution plane is not sufficiently effective against the second threat, then Enhanced TCAS will favor the alternate resolution plane.

Slow Pilot Response

Under normal conditions, a single-dimension TCAS Resolution Advisory is perfectly adequate for safely resolving a conflict. The TCAS alarm times allow for a certain amount of variation in pilot response, as well as a certain amount of error in surveillance and tracking data. However, if pilot response is unusually slow, or if a maneuver by the intruder causes a decrease in projected separation, then a single-dimension advisory may not produce as much separation as desired. Thus, with a vertical-only system, the amount of separation that can be generated against a threat is limited to whatever can be achieved with a single-dimension positive advisory ("climb" or "descend").

The Enhanced TCAS resolution logic is designed to select a single-dimension Resolution Advisory initially against each threat. Once a Resolution Advisory has been displayed, the projected separation is continuously monitored as the conflict progresses. During this time, the strength of the selected advisory (positive, negative, vertical speed limit) is adjusted as necessary. If the pilot is unusually slow to respond to the advisory, or if the projected separation greatly decreases for any reason, then the full set of advisory evaluation tests is repeated so that a double-dimension advisory (such as "climb and turn left") can be selected. By adding the second resolution plane when required, the system can add an extra margin of safety to a deteriorating situation.

Evaluation Plan

The evaluation of the Enhanced TCAS algorithms has made good progress, although much work remains to be done. Initially, computer simulation runs validated the design and coding of the logic. Subsequently, encounters were tested using both fast-time simulation and flight testing of the Enhanced TCAS II Engineering Model.

Fast-time simulation allows many more encounter geometries to be tested, under closely controlled conditions, than does flight testing. Also, the "true" positions of the aircraft are known, as they are generated by the computer. Specific encounters of interest may be saved and replayed exactly, to study variations using different logic, repeated samples of random measurement error, or different pilot response. The measurement errors can be simulated using various distributions; however, the amount of effort to be expended will depend on the observed sensitivity of the logic to this error.

The initial fast-time simulations explored the ability of the logic to provide separation for a variety of encounter geometries, in the absence of bearing measurement error. These results provide a baseline for comparison with later tests. The geometries include linear flight, both level and with vertical rates; and maneuvers, both vertical and horizontal. Of particular interest are adverse maneuvers by the intruder, in the direction contrary to the initial TCAS advisory. If Enhanced TCAS determines that its initial choice will not provide adequate separation, it selects the other plane of resolution.

Simulation testing will be structured to study changes in the logic's performance in terms of sensitivities to real-world effects. Both the magnitude and distribution of bearing errors are of special interest, as the theoretical estimates have been supported by only a limited amount of in-flight measurement data. Logic testing will play a major role in determining the specification of accuracy requirements for this system.

Another form of simulation testing is called microscopic analysis. Working with a detailed knowledge of the algorithms, scenarios are specially designed to exercise each internal path of interest. This ensures that rare cases are tested which might seldom be seen using "normal" encounters.

Flight test data also forms a vital part of the evaluation. Engineering flights are made to gather data both from planned encounters and in normal traffic of various densities. Recorded data may be replayed using the same or improved logic. This data provides the real test of performance in the presence of measurement error. Any deficiencies in the simulation model will appear as differences when flight test encounters are studied.

The evaluation activities will address technical performance issues, such as the separation provided for various geometries; design issues, such as the basic tradeoffs discussed earlier; and operational issues. The variable alarm time feature will be examined to determine whether a reduction in unnecessary alerts is achieved by the logic. Specific Resolution Advisory sequences will be examined to determine whether the simulated escape maneuvers can reasonably be performed in flight. The resolution evaluation criteria will be studied to determine if they are sufficient, properly prioritized, and all utilized.

Conclusions

The Enhanced TCAS II system has been endowed with features intended to provide collision protection with more flexibility than the Minimum TCAS system. The use of horizontal and vertical Resolution Advisories should facilitate operational acceptance of the system and provide greater protection against maneuvering intruders. The collision avoidance logic includes features designed to reduce the rate of unnecessary alarms.

A comprehensive test program has been initiated to evaluate and refine the logic design. Data taken from Engineering Model flight tests will be used to characterize measurements errors and to exercise the logic through further simulation.

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IMPROVED TCAS I FOR PILOT WARNING INDICATION

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Abstract

TCAS is a system of computerized airborne equipment for preventing mid-air collisions. It operates by detecting the radar beacon transponders carried on board most aircraft for support of ground-based air traffic control surveillance. Two categories of TCAS equipment have been defined. TCAS I equipment generally detects aircraft at relatively short range and provides the pilot with a traffic alert. TCAS II equipment detects aircraft at longer ranges and can provide the pilot with comprehensive traffic advisories as well as advice on how to maneuver to avoid a collision. There is growing interest in TCAS I equipment with the capability to provide reliable surveillance of transponder-equipped aircraft out to ranges of 3 to 4 miles and to present the surveillance information to the pilot in the form of a plan position display. The TCAS I equipment would not transmit Mode S interrogations. It would perform surveillance of Mode S transponders by means of conventional Mode C interrogations. Existing interference standards for TCAS I hold the interrogation rate-power product constant, regardless of where the aircraft is flying. These standards were derived from worst-case interference assumptions. As a result, in a region of less than worst-case interference, TCAS I would be constrained to a power level well below what could be tolerated. This paper discusses recent improvements to the TCAS I interference standards that will allow such equipment to increase surveillance range and increase the aircraft density into which TCAS I can reliably be operated.

Introduction

Within the family of beacon-based collision avoidance systems under development, TCAS I is a lower cost, lower performance type intended principally for general aviation use (1,2,3). TCAS I may accomplish its surveillance of nearby transponder-equipped aircraft either by passively detecting transponder replies elicited by other interrogators or by transmitting its own low-power interrogations.

This work was performed under the sponsorship of the Federal Aviation Administration.

Any airborne device that operates by transmitting active interrogations must be constrained to assure that it does not generate unacceptable levels of radio frequency interference. Specific rules for assuring this in TCAS II devices have been published by the FAA in the U.S. National Standard for TCAS II (4) and by the Radio Technical Commission for Aeronautics (RTCA) in its TCAS II Minimum Operating Performance Standards (5). Guidelines for assuring this for TCAS I devices have been published by RTCA (6). This paper reviews interference limiting considerations for active TCAS I devices and describes changes to the existing guidelines that would allow performance to be improved.

The current standards for operation of TCAS I require the product of the interrogation rate and the peak power to be constant, regardless of where the aircraft is flying. Because of this the standards were derived from worst-case interference conditions; that is, a density of aircraft of 0.3 aircraft per square nmi and many TCAS II-equipped aircraft in the vicinity also interrogating in the 1030 MHz band. As a result, when flying in less dense airspace, a TCAS I is constrained to operate well below the average power level that would actually be tolerable.

In principle, TCAS I could be made more capable by more fully using the information available to it about the actual operating environment. Changes to the existing TCAS I interference standards are introduced herein which would allow TCAS I to benefit from its knowledge of the environment.

Background

TCAS I interference limits are based on the more general limits for TCAS II devices. These latter will be reviewed first.

Interference Limiting Standard for TCAS II

The interference limiting rules for TCAS II consist of a set of three inequalities intended to control respectively the effect of TCAS transmissions a) on the reply probability of nearby transponders, b) on own transponder's reply probability, and c) on the generation of Mode C transponder replies from nearby transponders (4). The inequalities that control the first and third of these effects are both based on a knowledge of the total number of TCAS units in the vicinity. That is, each TCAS II unit is required to monitor the number of other TCAS II units and to limit its average power so that the effects of all of the TCAS units together do not exceed predetermined bounds. The number of

other TCAS II units is monitored by receiving the broadcasts periodically transmitted by each TCAS II at 1030 MHz.

Existing Interference Limiting Standards for TCAS I

In the existing concept TCAS I is either passive or it employs Mode C interrogations. Unlike TCAS II it does not periodically transmit self-identifying broadcasts at 1030 MHz.

The existing interference limiting standard for TCAS I imposes a constant limit on interrogation rate and power. The limit was based on the following assumptions: a) that the TCAS I aircraft is located in a region whose traffic density may be as high as 0.3 aircraft per square nmi, b) that there may be nearby TCAS II-equipped aircraft using the entire TCAS II allocation of interference, and c) that up to 50% of the aircraft in the region are TCAS I equipped (3). The TCAS I aircraft are then restricted so that altogether they contribute no more reply interference than 10% of that allocated to all the nearby TCAS II aircraft.

Taken together, these constraints limit the rate-power product to 5 watts per second. A particular design might employ one 20 watt interrogation every 4 seconds. This low power level would be adequate for a simple traffic alerting system whose purpose is to warn the pilot when there is an aircraft at short range (for example, less than two miles.)

New Interference Limiting Standard

With the development of reliable means for estimating the bearing of nearby transponder equipped aircraft it has become possible to consider a TCAS I that not only indicates the presence of a nearby aircraft but also displays its range and bearing in the form of a plan-position indicator (PPI) display.

The availability of such a display leads naturally to a desire on the part of the user to see more than one target and to provide surveillance out to typical visual acquisition ranges of 3 or 4 miles. Studies have shown that at altitudes below 10,000 ft there are rarely encounters between aircraft that exceed closing speeds of about 400 kt. To obtain a 30-sec warning time at 400 kt. the detection range must be 3.3 nmi.

If we assume that the TCAS I is operating in an aircraft density of 0.15 aircraft per square nmi (a high density) the number of targets detected within 3.5 nmi is approximately 5. An air-to-air surveillance system that is capable of withstanding this load will need to employ some technique to overcome synchronous garble. Probably the most appropriate technique for overcoming synchronous garble in TCAS I is the use of a sequence of interrogations of varying power. This will increase the average interrogation power.

Thus there would be two benefits to an increase in TCAS I power above the 5 watts/sec. limit: (1) an increase in surveillance range, which is associated with higher closing speeds, and (2) use of a sequence of interrogations, which would increase the aircraft density into which the equipment could reliably operate.

Three means are available for allowing an increase in TCAS I power. They all take advantage of the TCAS I's ability to sense the nearby environment and to thus select its power based on the actual, rather than a worst-case, environment. The TCAS I can use its knowledge of a) the local traffic density, b) the reply rate of the transponder on board own aircraft, and c) if own transponder is Mode S, the nearby TCAS II population. The following sections examine each of these techniques.

Use of Knowledge of Local Traffic to Increase Power

A TCAS I that is capable of accurate surveillance can estimate the density of nearby traffic. If it is then assumed, as it was in deriving the 5 watt-per-second limit, that 50% of the aircraft in the area are also TCAS I equipped, it is possible to allow the radiated power to increase as the local traffic count decreases. As will be shown below, if nothing is detected within 3.5 nmi, the power limit can be increased by a more than an order of magnitude.

It is essential that the TCAS I have an accurate estimate of the number of targets within its current operating range R_o if this technique is to work properly. The TCAS I must transmit sufficient power to provide reliable surveillance out to range R_o and it must also include provisions for assuring that the aircraft count is not under-estimated because of reply loss due to synchronous garbling. This can be accomplished by monitoring the reply registers to assure that they are never overloaded following an interrogation. If a reply register associated with a particular interrogation is found to be consistently overloaded, only lower power sequences should be transmitted and the range R_o should be reduced accordingly until the overload clears.

Use of Knowledge of Own Transponder Reply Rate to Increase Power

The 5 watt/sec interference limit for TCAS I was based on a requirement that TCAS devices as an ensemble limit their interrogation rates to add no more than 40 replies per second to the nominal peak reply load of 200 replies per second from each SSR transponder. The TCAS I population is constrained to produce no more than 10% of the interference allowed for TCAS II. Thus, all of the TCAS I devices in an area must together elicit no more than 4 replies per second from each transponder in the area.

A TCAS I can learn about the reply rate of local transponders by counting the reply rate of its own on-board transponder. If it is found that own transponder is replying at a rate that is less than 240 replies per second, it should then be possible for TCAS I to ignore the interference limit associated with SSR replies, which would otherwise be the controlling effect of the three effects being considered. In this condition, average power can be increased by a factor of 3.5 (as will be seen below).

Precautions must be taken to assure that the on-board estimate of transponder reply rate is accurate. A possible source of error is the setting of the minimum triggering level (MTL) of

the transponder. If the MTL is increased by 3 dB, the average transponder reply rate will be reduced by about a factor of two. Thus, this technique should be restricted to aircraft for which the MTL of the transponder is known to be at least as good as nominal. If the transponder is less sensitive than nominal, a correction must be made to the reply count.

Use of Mode S Transponders

If the TCAS I aircraft is equipped with a Mode S transponder, it becomes possible to determine the number of TCAS II aircraft within 30 nmi by monitoring TCAS II broadcast transmissions. When there are no TCAS II aircraft in the vicinity, it would be reasonable to allow a higher TCAS I interrogation power as long as the overall limits for TCAS are not exceeded. The standards for TCAS II limit any single unit to approximately 6% of the total. Thus the remainder could be used to permit TCAS I units to decrease their average power gradually as the number of TCAS II units increases.

New Limiting Standards

The new interference limiting standards for TCAS I, including all three of the above considerations, are given in Fig. 1. The quantity that is limited is $\Sigma P(k)$ which is the generalized rate-power product for a sequence of interrogations of varying power. These inequalities are functions of:

RR = the combined Mode S and Mode C reply rate of the transponder on-board the TCAS I aircraft;

NT = the number of TCAS II aircraft whose broadcast interrogations are currently being received by own Mode S transponder; and

DL = the estimated density of PWI-equipped aircraft determined by counting, for example, the number of aircraft N(3.5) within a 3.5 nmi radius of the TCAS I aircraft.

These limits have been evaluated and are plotted in Fig. 2. The new limit is much higher than the existing 5 watt/sec. limit in most cases. For example, if N(3.5) = 2 (which represents a reasonably high density) and if NT = 0 (no TCAS II traffic), then the limit is

$$\Sigma P(k) \begin{cases} < 180 \text{ watts/sec. if RR} > 240/\text{sec.} \\ < 250 \text{ watts/sec. otherwise} \end{cases}$$

The latter is the highest value allowed under any condition.

A Specific TCAS I Design

Replies from Mode C targets whose ranges differ by less than 1.8 nmi will overlap at the TCAS receiver. This "synchronous garble" phenomenon can be largely overcome in TCAS equipment by transmitting a sequence of interrogations of different powers in each surveillance cycle. If each of these interrogations is preceded by a lower-power suppression pulse, the number of transponders that reply to the interrogation is limited. This scheme is known as "whisper-shout" and enables TCAS to separate multiple targets so that their replies are less likely to overlap and garble each other (7).

If RR $\leq$ 240/sec,

$$\sum_{k=1}^{K} \frac{P(k)}{250} \leq \text{greater of } \left(\frac{1-0.06\,NT}{10\,DL}, 0.02\right), \text{ for NT} \leq 15$$

$$\leq \text{greater of } \left(\frac{1-0.06\,NT}{100\,DL}, 0.02\right), \text{ for NT} > 15$$

or unknown

if RR > 240/sec,

$$\sum_{k=1}^{K} \frac{P(k)}{250} \leq \text{greater of } \left(\frac{1-0.06\,NT}{35\,DL}, 0.02\right), \text{ for NT} \leq 15$$

$$\leq \text{greater of } \left(\frac{1-0.06\,NT}{350}, 0.02\right), \text{ for NT} > 15$$

or unknown

under all conditions,

$$\sum_{k=1}^{K} P(k) \leq 250 \text{ W/sec}$$

$$P(k) \leq 100 \text{ W}$$

where:

RR = transponder reply rate

NT = number of TCAS II aircraft nearby

P(k) = power (Watts) of the k^{th} interrogation each second. This is the power actually transmitted, after all losses in cabling and antenna. If the set of powers is not the same in each 1 sec period, then $\Sigma P(k)$ represents the average value.

K = total number of interrogations in 1 sec.

DL = $(N_o+1)/2\pi R_o^2$, and N_o = number of transponder-equipped aircraft within R_o nmi.

Fig. 1. New limiting standards for TCAS I.

The whisper-shout transmission requires a variable attenuator whose attenuation values are stable and accurate to better than 1 dB and which can be switched in less than 2 microseconds. Attenuators used in TCAS II equipment typically employ 32 attenuation levels. Reliable TCAS I surveillance can probably be accomplished with an 8-level attenuator. A specific whisper-shout sequence of 8 interrogation levels for use in TCAS I is illustrated in Fig. 3. The peak transmitted power in this sequence is 100 watts, the sum of the transmitted powers is 250 W, and the repetition rate is 1/sec. Thus, all eight levels of this sequence can be transmitted once per second in airspace where the interference environment is such that TCAS I is permitted to operate at its full rate and power.

When operating in an area of higher interference, such that the allowable limit is less than 250 Watts, this design accommodates in two ways. First the repetition period is increased to 2 sec., and subsequently the interrogation levels are eliminated one-by-one beginning with the highest. Thus performance will degrade gracefully when flying into a dense area, and the system can continue to be used and will continue to provide a useful service under these conditions.

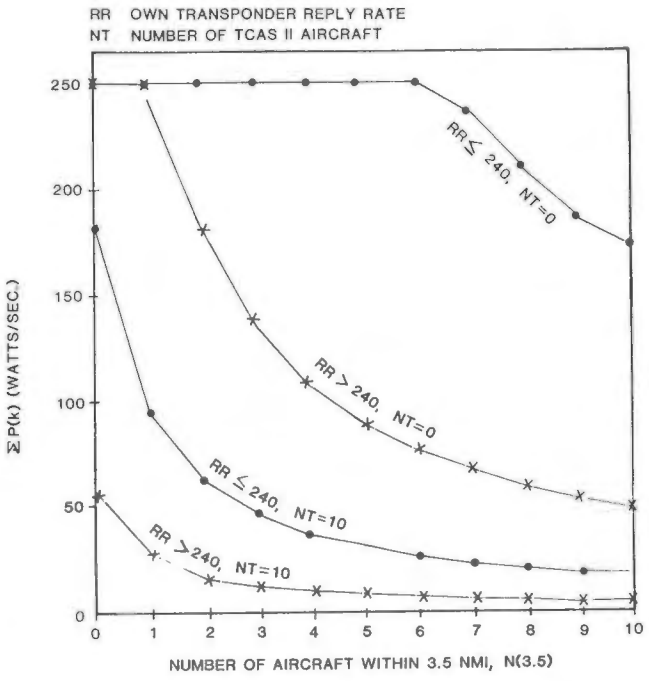
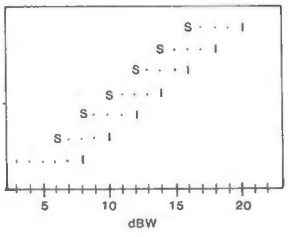


Fig. 2. New power limits for TCAS I.

STEP NUMBER	INTERROGATION POWER (dBW)	SUPPRESSION POWER (dBW)
7	20	16
6	18	14
5	16	12
4	14	10
3	12	8
2	10	6
1	8	NONE



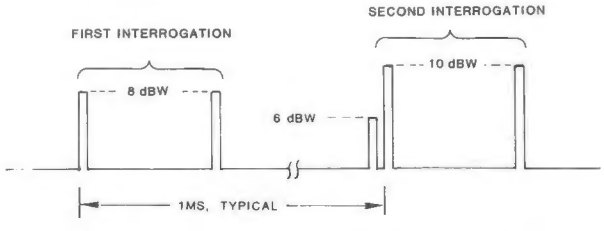


Fig. 3. TCAS 1 whisper-shout sequence of 8 levels.

Summary

This development of new interference standards for TCAS I equipment has resulted in an allowance of considerably higher values of interrogation power, while still assuring non-interference with other systems that operate at or near 1030 and 1090 MHz.

The increased power will be useful for extending surveillance range and for extending the capability to operate into dense traffic areas. To take advantage of these new higher limits, a TCAS I will make use of information characterizing the local environment in which it is currently flying: transponder reply rate, number of target aircraft, and number of TCAS II aircraft in the vicinity. The TCAS I can use all, some, or none of these pieces of information. In the latter case, the power limit becomes simply 5 watts/sec., which was the previously existing standard.

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SECONDARY SURVEILLANCE RADAR MODE S
POTENTIAL APPLICATIONS AND FUTURE REQUIREMENTS IN EUROPE

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Abstract

Although the technical performance of today's Secondary Surveillance Radar (SSR) in the European environment is adequate and will be improved by a number of enhancements now being introduced, the use of Mode A codes for identification presents severe operational problems. Aircraft identification reporting through SSR Mode S will eliminate the difficulties. The air-ground data link capability of Mode S is seen as an important component of a future Air Traffic Control (ATC) system. A programme of work, including real-time simulations, to study the role of the data link in two-way communications between ATC and the aircraft is described together with initial results. Other studies related to data link applications are presented. These include the acquisition and exploitation on the ground of data available from the aircraft system. Although there is no requirement for an Airborne Collision Avoidance System (ACAS) in European airspace, it is recognised that aircraft so equipped will enhance air traffic safety. Studies and trials are being undertaken to ensure that the use of ACAS in European airspace will not perturb the ATC system nor cause interference to SSR. The potential operational benefits of a ground-based traffic advisory system using Mode S are also being studied.

SSR in Europe Today

Operational Use

Today in Europe, Secondary Surveillance Radar (SSR), as defined in ICAO Annex 10 and referred to as the ATC Radar Beacon System (ATCRBS) in the United States, has become the principal tool for the surveillance of civil air traffic. Primary radar now serves as a backup to SSR, available to ATC in the event of SSR transponder failure, for the surveillance of VFR aircraft not equipped with transponders and for civil/military coordination. In the controlled airspace of the EUROCONTROL Member States (Belgium, the Federal Republic of Germany, France, Ireland, Luxembourg, the Netherlands and the United Kingdom) and in a large part of Western Europe, the carriage of an SSR transponder with pressure altitude reporting capability is mandatory for IFR traffic. SSR is therefore required to provide a clear, accurate and reliable display for the air traffic controller of the air traffic situation. In Europe wide use is made of synthetic labelled radar displays using processed radar data rather than analogue data and with each target labelled with the aircraft identification (e.g. flight number) or Mode A code and Mode C pressure altitude.

Deficiencies

Technical Deficiencies. The problems inherent in the SSR system are well known. They stem mainly from the fact that the system uses a single frequency channel for all interrogations and a single channel for transponder replies. This gives rise to mutual interference phenomena which degrade system performance below the theoretical maximum. In Europe the close proximity of a number of major international traffic hubs and a complex route structure lead to high transponder densities. Furthermore the concentration of military interrogators in some areas, added to those used for civil purposes, has aggravated the interference problems.

Operational Problems. The air traffic controller requires a traffic display in order to monitor the evolution of the traffic situation and to provide safe separation between aircraft. SSR provides not only a plan position display, but also allows aircraft targets to be labelled with altitude, derived directly from Mode C data, and with aircraft identification. The aircraft identification required by the controller is the aircraft call sign as entered in the flight plan, usually the flight number. If a flight plan does not exist this may alternatively be the aircraft registration, or tail number. The SSR Mode A code may be used in the ATC processing system to correlate a specific radar track with a flight plan and thus permits the displayed track to be labelled with the aircraft identification. The need to assign a Mode A code to each aircraft is giving rise to serious operational problems in the European environment.

The Mode A codes are assigned to individual aircraft by ATC from a theoretical maximum of 4096, or 64 blocks of 64 codes each. However, a number of blocks are not available in practice, having been reserved for military use or for special purposes such as to indicate emergency situations. There are also two basic, but not entirely compatible, principles for code assignment: firstly the same code should not be used by two aircraft simultaneously in the same

area and secondly the need to change code during the course of a flight should be avoided. In the ICAO European (EUR) Region the available codes are shared between 33 States. Blocks of codes are allocated to individual States for domestic use and to individual control centres assembled in 5 participating areas for assignment to international flights. Once assigned a code should not be re-assigned to another flight until after a given protection time (generally 2 hours) has elapsed. There is now a serious shortage of available codes.

In the provision of air traffic services the need to assign, enter and cross-check codes leads to an increase in R/T frequency loading and workload of both controller and pilot. In times of high activity the risk of omission or error is significant. Confusion can also arise when coordination is required between units not sharing a common data base such as may be the case for civil/military coordination.

Current Improvement Programme

In recent years much research and development has been directed towards overcoming the technical deficiencies of the SSR system and ensuring that SSR will meet the more demanding future requirements with respect to both accuracy and reliability. Modern radar plot extractors and radar data processing techniques ensure that, even in adverse environmental conditions, the air traffic controller is presented with a clear, accurate display of the air traffic situation. Monopulse azimuth measurement techniques will bring further improvements, increasing azimuth accuracy and, due to lower interrogation rates, reducing the interference effects. Monopulse developments are underway in several European States and the first operational monopulse systems are now being implemented in the United-Kingdom. Wide vertical aperture antennas, reducing propogation towards the ground and therefore reducing multipath effects, also enhance system performance.

SSR Mode S

SSR Mode S is an evolutionary development of the current SSR system in which each suitably equipped aircraft is assigned a unique address allowing it to be selectively interrogated. This selective interrogation feature, as opposed to the spatial interrogations of the current SSR, eliminates much of the mutual interference encountered in the present system and provides an air-ground digital data link capability (1) (2).

Operational Requirements and Benefits

Surveillance. It is expected that the SSR enhancements now being developed and implemented will ensure that the current SSR will continue to meet the requirements for air traffic surveillance in Europe well into the last decade of this century. Of course the operational constraint imposed by the need to continue to assign Mode A identity codes will be aggravated during this period with increasing traffic densities. It is therefore significant that the ATC requirement for unambiguous aircraft identification can be met with SSR Mode S.

Aircraft Identification Reporting. The SSR Mode S standards now being defined in the ICAO forum for worldwide application include a message format and protocol for the transmission from the aircraft to the ground of the aircraft identification, either entered by the pilot, if flight number is used, or possibly wired into the airframe if the registration marking is used. The identification would be transmitted automatically in a reply whenever requested in a surveillance interrogation. The implication of this technique is that the Mode S transponder will have to have more than the basic surveillance capability, i.e. it will also need the air-to-ground standard length message capability to transmit the identification in a Comm-B reply.

The aircraft identification reporting feature of SSR Mode S, although able to overcome one of the major operational problems encountered in Europe with current SSR, does not in itself constitute sufficient justification for the early implementation of a Mode S ground environment nor the implicit need for a transition in the airborne equipment from SSR Mode A/C to Mode S transponders. However the EUROCONTROL Member States, at least, have clearly stated that once Mode S surveillance coverage in the region is sufficient to justify the mandatory carriage of Mode S transponders, the aircraft identification reporting capability will be a required feature. Recognising the benefits to ATC worldwide of unambiguous aircraft identification and desirous to avoid a multiplicity of different regional requirements for Mode S airborne equipment capability, the ICAO SSR Improvements and Collision Avoidance Systems Panel (SICASP) is proposing, as an ICAO standard, that all Mode S transponders fitted to aircraft pertaining to international civil air traffic have standard length communications and aircraft identifications reporting capability.

In view of the fact that aircraft identification reporting implies the need for a transponder with data link capability, alternative solutions have been examined. The use of the 24-bit Mode S address, either inserted in the flight plan or used with a look-up table correlating address with aircraft registration, has been dismissed as impracticable both operationally and administratively. A proposal for General Aviation aircraft to use a hexadecimal encoding of the 24-bit address for identifica-tion, instead of the registration as at present, was also rejected as it required drastic changes to current ICAO procedures which are applied on a worldwide basis. Another proposal to provide identification in multiple short format replies, normally used only for basic surveillance, was rejected because of the significant modifications required to the Mode S formats and protocols. These are but a few of the possible means of providing aircraft identification without data link capability which have been studied in EUROCONTROL and within the ICAO SICAS Panel. These and other solutions have been examined elsewhere(3). In each case it has been concluded that the only technically sound solution is to use the Comm-B message format and the existing aircraft identification protocol.

Other Potential Benefits. Although, as has been stated earlier, enhancements to the current SSR will go a long way towards overcoming many of its shortcomings, Mode S will bring with it further improvements to surveillance performance. The ability to schedule addressed interrogations to avoid replies overlapping at the interrogator antenna eliminates the "garbling" phenomenon. Other improvements to interference levels will also be apparent from reduced interrogation rates.

Another potential benefit currently being studied within the ICAO SICAS Panel, and elsewhere, is the possibility of improving the quantisation of altitude data provided by Mode S transponders in suitably equipped aircraft. At present, Mode C data is encoded in 100-foot increments. It is argued that the performance of vertical rate trackers and vertical manoeuvre detectors, such as used in modern short term conflict alert systems, could be improved if this quantisation error were reduced to, say, 25 feet. For aircraft equipped with modern air data computers this does not present a problem. For aircraft which do not at present have a digital altimetry system it is not anticipated that they would require to provide pressure altitude data with the improved quantisation. In fact the ground system would have to continue to live with both systems but in the European environment it could be expected that over a period of time there would be a transition to a situation in which a large proportion of aircraft in controlled airspace would be able to provide 25-foot quantised altitude data. If this proposal is finally adopted for international standards then there will be implications for the vertical tracking system used by Airborne Collision Avoidance Systems (ACAS). This aspect is already being studied by the FAA.

European Studies and Trials.

Although there are at present no plans within the EUROCONTROL States to implement Mode S ground facilities in the near future, the present trend in Europe to upgrade existing surveillance sys-tems to monopulse SSR can be considered as an evolutionary step towards full Mode S capability. For this reason the EUROCONTROL States have followed closely the development and evaluation of the Mode S system both in the United-Kingdom and in the United States. Recently, some changes have been introduced into the system specifications which have not yet been thoroughly tested. EUROCONTROL is now planning a major trials programme which will evaluate features such as the multisite protocols. For this programme interrogators are being developed by the Civil Aviation Authority (CAA) in the U.K. and the Direction de la Navigation Aérienne (DNA) in France. It is expected that at least three interrogators will be available. The transponders, which are being developed under contract to EUROCONTROL, will have full communications capability, including extended length message (Comm-C and Comm-D) capability, and antenna diversity operation. Although, inevitably, some trials will use special test aircraft, it is intended that much of the programme will be carried out with Mode S transponders installed in commercial fleet aircraft normally operating in the coverage of the ground stations.

The same trials environment will provide a valuable basis for the evaluation of the Mode S data link. There are a number of potential applications of the data link which may produce benefits to the European ATC systems in both the medium and long term. These are now being studied and may bring about an earlier implementation of Mode S in Europe than would otherwise have been the case.

Data Link

Background

Fig. 1 indicates a programme of work on data link that has been running since 1974 to explore the benefits that a link could offer in an advanced system of ATC, thought capable of handling higher volumes of traffic while permitting more efficient aircraft operations, as proposed in (4) and (5). The concept described in these references, which has many similarities with FAA's AERA concept (6), is based on the exploitation of accurate aircraft trajectory prediction techniques. Prediction techniques range from the simple, that may be valid for a few minutes, e.g. extrapolated radar track, to the more complex, valid over many minutes, that require a large amount of data including high quality wind vector data.

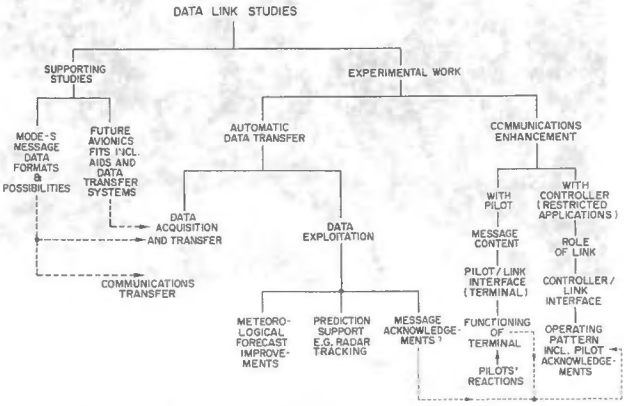

Fig. 1: Studies associated with the Mode S data link.

The data link is an ideal tool for permitting an increase in the exchange of data between ATC and an aircraft and it is in this role that it can best assist trajectory prediction. Additionally, although it is unlikely to replace R/T for non-routine communications, it appears to have the potential to overcome many of the R/T communications' difficulties currently experienced in Europe, e.g. overloaded and blocked channels, misunderstandings and delays due to language difficulties; in these control loop applications, as with the automatic transfer of aircraft data, the link can permit reliable and reasonably fast reactions and thereby enable the effects of operating errors or the malfunction of navigation equipment to be minimised. Whereas all earlier studies have been related to these future system applications, much work is currently being performed to evaluate the link's role in improving communications during the initial implementation of the Mode-S system. From the outset, link capacity requirements have been matched to the capacity expected from Mode-S.

Communications Enhancement

The Pilot/Link Interface. In order to obtain an overall assessment of the link's value in enhancing communications, and aircrew reactions to applications being considered, the pilot/link interface was first studied. For this, an experimental interface, known as the Airborne Link Terminal (ALT) was developed, together with a scenario thought representative of the future ATC environment. The interface, comprising CDU and miniature hard-copy printer (see Fig. 2), was mounted on the flight deck of an A 300B Airbus flight simulator and driven as shown in Fig. 3. Perfect ground facilities were assumed. An evaluation lasting many "flying hours" was conducted, largely by crews from Lufthansa, the German national airline, who found the most attractive feature to be the hard-copy print-out of long messages, e.g. clearances, weather and ATIS information. Full details of the evaluation are given in (7).

Fig. 2: The experimental pilot/link interface installed in the A 300B Airbus flight simulator.

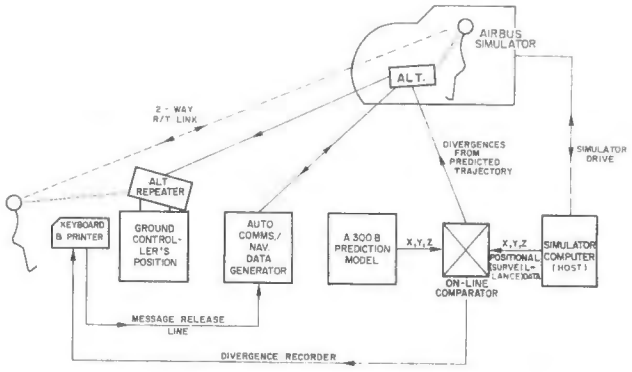

Fig. 3: Functional diagram of simplified system used for ALT experiments.

The Controller/Link Interface. To use the data link for many of the applications studied in the ALT experiments would require a very high level of automation and standardisation in ground-based systems, in particular for the generation and control of long messages. Because the initial implementation of Mode S in Europe is likely to be patchy and the overall level of automation inadequate, it has been necessary to consider and evaluate a more limited range of link applications of a somewhat tactical nature and thought likely to provide benefits in the short term. These include the duplication of the critical parts of R/T messages, in particular flight level clearances, the replacement of certain control messages, such as aircraft transfers, and assistance in conditions of full or partial R/T failure. The evaluations are being mounted by means of real time simulations for which the planning criteria call for little or no increase in controller and pilot workloads and levels of Mode S carriage ranging from 30 % to 100 % of the total traffic.

Possible Benefits. Although the work to date has not been fully representative of the Mode S system, the controllers and a small number of pilots participating in the simulations have been very positive in their support of the link's use both in duplicating R/T and in conditions of partial or full channel failure.

Limitations. Using present-day facilities, it is only when message duplication is tied to normal input actions (to the ATC computer) that controller workload can be maintained at a satisfactory level. With the variable delay in the time of delivery and receipt of Mode S messages (owing to the rotational antenna scan) it is difficult to maintain a good time relationship between R/T and data-linked messages. Much work remains to be done in order to develop suitable facilities and/or procedures to overcome these problems.

Observations. Although the work is by no means complete, experiments performed to date have highlighted a number of factors that should be borne in mind if the link is to be used in these limited applications.

(a) R/T message duplication may be better achieved using pre-notification data link messages, i.e. sent before the R/T message;

(b) whenever confirmations and/or pre-notifications are introduced for particular message types, they should accompany these messages on every occasion irrespective of controller loading;

(c) for purposes of confirmation/correlation, controllers require aircraft to be identified on their traffic display whenever data link duplications have been sent to them;

(d) because of the range of possibilites available for message acknowledgement, the actual pilot action required should be evident from any message he receives;

(e) there should be a smooth transition in communications procedures whenever aircraft move from data link to non-data link areas of control or vice versa, etc.

Automatic Data Transfer

In European controlled airspace commercial operations, by aircraft with good avionics fits, far exceed those of general aviation; it is thus attractive to consider the use of data that can be acquired automatically from aircraft to enhance the operation of the ATC system, particularly for trajectory prediction purposes. On many modern aircraft digital data can be readily acquired on some 10-15 parameters of potential interest: typical examples are shown in Table 1 below.

PARAMETER	POTENTIAL APPLICATION	RESOLUTION		DATA BITS REQUIRED FOR TRANSFER
		AVAILABLE	ACCEPTABLE	
MAGNETIC HEADING	RADAR TRACKING	0.05°	0.7°	11
ROLL ANGLE	" "	0.01°	0.7°	11
COMPUTED AIR SPEED	" "	0.25 kt	2 kt	12
WIND SPEED	METEOROLOGY	0.5 kt	2 kt	10
WIND DIRECTION	"	0.35°	1.4°	10
TOTAL AIR TEMP.*	"	0.5°	1°	12
GROSS WEIGHT	CLIMB/DESCENT PROFILES	40 lbs	640 lbs	14

* Static air temperature is preferable to avoid conversion on ground.

Table 1 - Examples of data available from many modern commercial aircraft

Apart from the aircraft's carriage of the appropriate sensor(s), satisfactory data acquisition and transfer necessitates access to the relevant data source, e.g. via the ARINC 429 data bus, plus some on board processing and a suitable data interface with the transponder, as discussed in (8). Because data availability is thus heavily dependent on aircraft type, it is necessary, when considering particular data applications, to make some forecasts of future aircraft population and their likely equipment carriage. Two applications studied relate to improvements in radar trackers and meteorological forecasts. The former would require data from the maximum number of aircraft possible, while in the latter case, data from 15-20 % of all traffic would probably suffice.

Radar Trackers. Radar trackers can provide frequent estimates of aircraft speed, position and future position for ATC displays, short-term conflict alert systems, etc. Because of imperfections in the radar data used (noise, missed plots) a considerable averaging period is required to obtain good estimates, making it difficult to detect rapidly any change in aircraft flight path, e.g. the onset of a manoeuvre. Because on-board measurements of various parameters offer scope for improvements both in this respect and in the subsequent tracking through the manoeuvre, three experimental trackers have been developed (9) and their performances assessed using data transferred via an experimental Mode S link.

The trackers were known as:

- ABF (Acceleration Bias Filter, employing roll-angle data);
- HBF (Heading Bias Filter, using heading data);
- VBF (Velocity Bias Filter, requiring both heading and true air speed data).

Their performances have been assessed both statistically and subjectively (with the aid of displayed tracks) using a reference baseline filter known as TARAD, which is a first-order Kalman filter believed to represent the best available in present-day ATC systems. Full results are given in (10) and it appears that, whereas all the modified trackers were superior to TARAD, HBF was probably the best of them when considering its performance following missing data together with its simple (heading) data requirement.

Meteorological Forecast Improvements. The quality of forecast winds available today in ATC centres is the major factor limiting the accuracy of aircraft trajectory predictions made over extended periods of time throughout all phases of flight: temperature effects are most significant in the climb phase. Following a search for improvements in the quality of these forecast data, it was thought that the most effective method would result from aircraft upper-air measurements and, accordingly, a series of feasibility studies was undertaken in conjunction with the Regional Meteorological Office, Bracknell, UK. Initially, this work aimed at establishing the accuracy of aircraft measurements of wind-vector (INS) and temperature, followed by an investigation into the feasibility of using data to obtain improvements in the quality of short-term meteorological forecasts (11). Practical experiments have since been conducted using an experimental Mode S data link as discussed below.

Experimental Facilities. In 1982, two British Airways Tristar aircraft were modified to carry prototype Mode S transponders with interfaces to the on-board AIDS systems. During approximately 200 normal scheduled flights, these two aircraft were interrogated by an experimental SSR Mode S station at Matching Green, north-east of London, whenever they flew within its cover. The aircraft data received on the ground plus the normal radar surveillance infor-mation, were transferred on-line to the EUROCONTROL Experimental Centre in France. These data were recorded for different studies; in addition, the meteorological data plus aircraft positional information and time were extracted and converted into a standard meteorological message known as a CODAR. The resulting CODARs were sent on-line by teletype link to the Paris Meteorological Office for onward transmission to Bracknell, via the World Meteorological Organisation (WMO) network. At Bracknell, the meteorological data were validated and used to continue the studies into the use of such airborne derived information for improving the quality of forecast data. For the latter stages of the meteorological experiment, wind/temperature profiles were constructed at Bracknell and remoted to London (Heathrow) Airport for use by forecasters. A functional diagram of the experimental set-up is given in Fig. 4. An example of comparisons between aircraft temperature data and appropriate radio sonde data is given in Fig. 5. The implications of this work are discussed in (12).

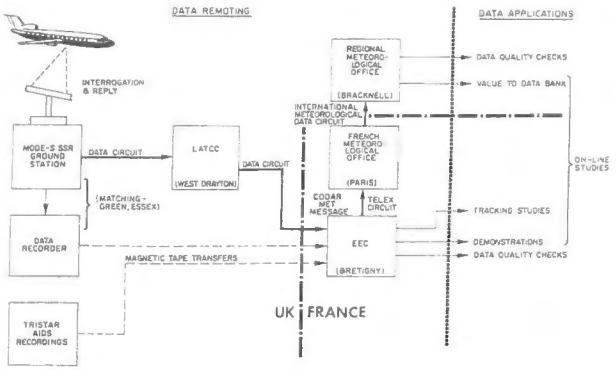

Fig. 4: Functional diagram of Mode S data acquisition facility for on-line exploitation experiments.

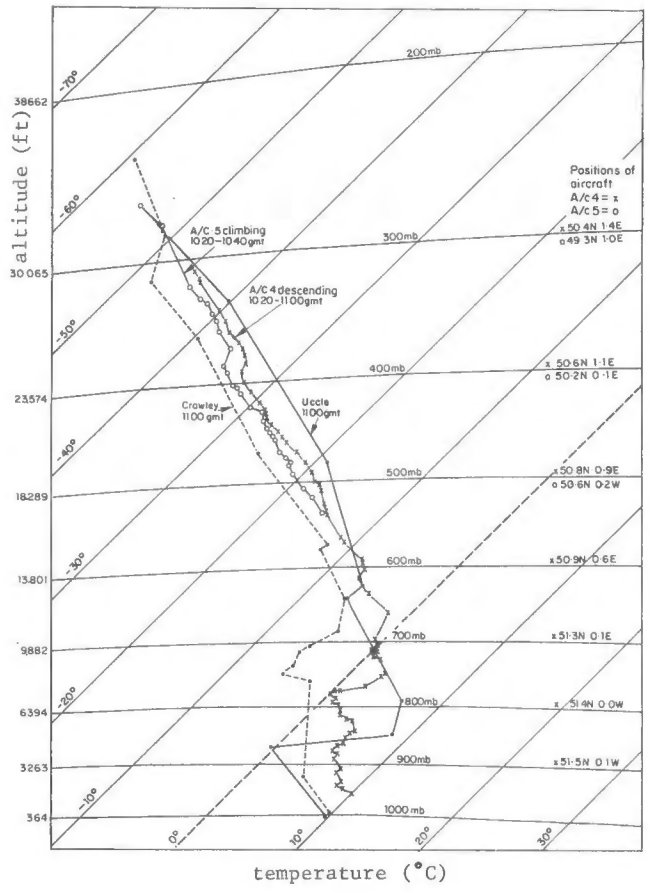

Fig. 5: Simplified tephigram comparisons of aircraft temperature data (recovered via the Mode S data link) and appropriate radio sonde data.

Mode S data from a number of flights containing a range of manoeuvres were selected from the recordings made at the Experimental Centre for use in evaluating the radar trackers, as mentioned above. From Figs 6 and 7 it is possible to compare the response to a manoeuvre and missing data of TARAD, which uses only positional data, with that of HBF, using heading data in addition.

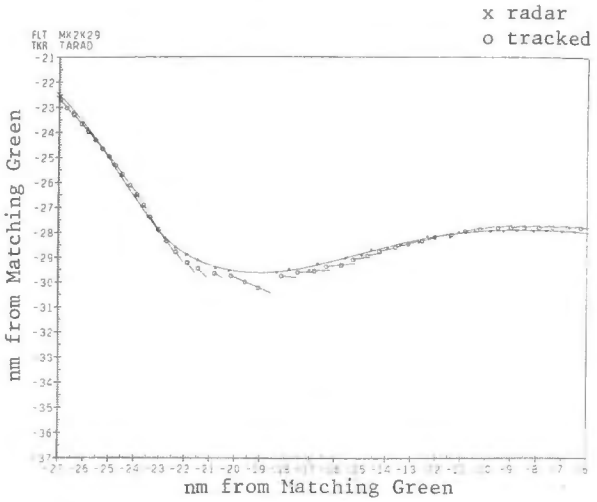

Fig. 6: Response of conventional tracker (TARAD) to typical manoeuvre with missed plots.

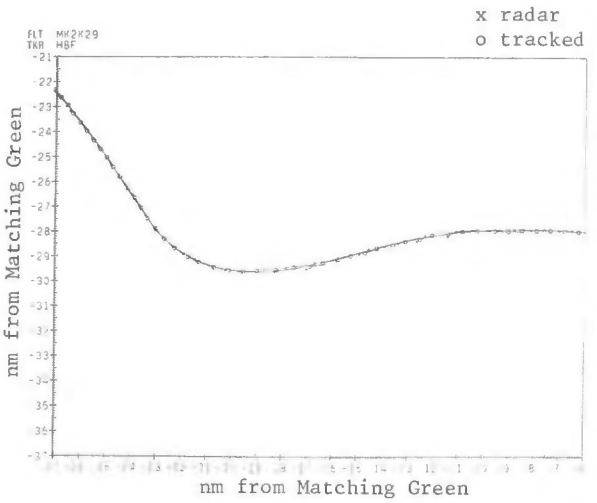

Fig. 7: Response of modified tracker (HBF) to same manoeuvre.

In another study, using the same data and the improved trackers, wind vectors are being computed from the tracker ground speed vectors and aircraft measurements of speed and heading (two parameters generally available) for comparison with the corresponding INS wind vectors.

Avionics Implications.

There is an increasing amount of work being performed on data link, both elsewhere in Europe and in the USA. Accordingly, it would be unrealistic to suggest that the picture emerging from the experimental work briefly described above gives the only possibility for the future.

Nevertheless, in an airborne installation comprising transponder, output display and hard-copy printer, input device and data processing unit, it is highly probable that the role of the latter will grow in importance as more communications are transferred via the link and the value of aircraft data in ATC systems becomes more widely recognised. Regarding the transfer of aircraft data, the processing unit may serve two main purposes, both of which would contribute to a more effective use of down link capacity. First, reformatting the data available from the aircraft systems and possibly buffering them for immediate transfer whenever required; second, processing readily available data to provide more usable information, e.g. computing true air speed, or static air temperature. It is clear that there will be a great deal of commonality in the needs of the Mode S data link and other systems under consideration, e.g. ASDAR and ACARS II. Should developments continue in this way, perhaps there is merit in considering some sharing of processing and input/output facilities to reduce weight, costs and the need for suitable space on the flight deck?

Collision Avoidance Systems

Airborne Collision Avoidance Systems

It is unlikely that there will be an operational need in the foreseeable future for an airborne collision avoidance system in European airspace. However a number of European States have followed with interest the development and trials of the Traffic Alert and Collision Avoidance System (TCAS) in the United States. Many aircraft operators will wish to equip their aircraft with ACAS, nevertheless, and it is generally accepted that the presence of such aircraft in the European airspace can only enhance air traffic safety.

European Studies. The studies relating to collision avoidance systems so far conducted or planned within EUROCONTROL and its member States are in general aimed at supporting the definition of a policy on the operation of ACAS in the EUROCONTROL airspace. No technical developments have so far been undertaken. These studies have been defined either to assist in an understanding of ACAS, both technically and operationally, or to assess the impact of ACAS in the European environment.

In the United Kingdom a study commissioned by the CAA to examine the impact of TCAS on monopulse SSR systems concludes that the probability of the loss of a target at the SSR ground system due to TCAS interference is acceptably low (13). It also demonstrates that the interference limiting mechanisms, which are part of the TCAS design, are crucial to ensure acceptably low interference levels. This study identified the mechanisms which cause TCAS to have an effect on the SSR system and examined the effects on two worst case scenarios, one assuming a uniform distribution of traffic in the airspace and the other representing one of the worst situations imaginable, viz. stacks of 14 TCAS equipped aircraft on a hexagonal lattice with 30 nm spacing. This represents some 1600 aircraft within 200 nm of the ground interrogator. It was estimated that, for these two scenarios, the probability of losing a single reply from a Mode A/C transponder was 0.051 and 0.136 respectively, the equivalent results for Mode S targets being 0.058 and 0.127. The probability, however, of losing a target, as distinct from a single reply, is of course much lower. It is estimated that with a monopulse extractor working on 6 to 8 hits in a 3 dB beamwidth the probability of loss of a target is approximately 0.01 times the probability of loss of a single reply. It should be emphasised that these are results for worst case scenarios. In practice, the interference effect will be considerably lower.

Another study, undertaken by the Centre d'Etudes de la Navigation Aérienne in France, has examined the operational impact of airborne collision avoidance systems on the ATC system (14). Applying ACAS conflict detection logic to on-line recordings of radar track data in an area embraced by the Paris terminal and en-route control centres and assuming that all altitude reporting (Mode C) aircraft were ACAS equipped (a worst case assumption), it indicated a peak alert rate of one alert per hour. The study concluded that the introduction of ACAS into French airspace would not disturb unduly the ATC system and would, in fact, increase overall safety.

A more recent study undertaken by the Technical University, Braunschweig (Federal Republic of Germany) has shown that, in the approach phase of flight, a TCAS traffic advisory would be generated once per 2.6 flight-hours in the Frankfurt terminal area in today's peak taffic conditions. A resolution advisory (Tau = 30 secs) would be generated once per 7.8 flight hours. These are not of course all real threats. Many result from the ATC procedures applied in the Frankfurt TMA, the runway configuration, etc. This rate is therefore considered to be unacceptably high and it suggests that under these circumstances, at some point on the glide-slope, resolution advisories would have to be inhibited (sensitivity level 2). The same study estimates that with horizontal threat logic (enhanced TCAS II) unwanted advisories would be eliminated. In the above case the resolution advisory rate would fall to some 10 % of its value i.e. 1 resolution advisory per 78 flight-hours.

The development of minimum TCAS II by the FAA has been based on a performance requirement for the reliable generation of resolution advisories in a traffic density of 0.3 aircraft per square nautical mile. A MITRE Corporation study has shown that such densities might occur in the Los Angeles Basin area by the year 1995 (15). Although it is not expected that such densities will be encountered in European airspace in the same timescale, a study is now underway to estimate future traffic densities in the three major terminal areas of the EUROCONTROL region (Frankfurt, London and Paris). Data recordings are now underway. Initial results from recorded radar data from the Frankfurt TMA show existing peak densities of 0.08 SSR equipped aircraft per nm^2 within a 10 nm square cell. This compares with a measured peak density of 0.15 SSR equipped aircraft in the Los Angeles Basin.

With a view to studying the impact of ACAS on the European ATC system, particularly that in France, and to assessing the operational interest of ACAS in current airline operations, the Direction de la Navigation Aérienne (DNA) in France, in cooperation with Air France and the FAA, has defined a programme of trials of ACAS very similar to the FAA's Piedmont Phase I trials. For these trials, which are currently underway, a Sperry Dalmo Victor TCAS II equipment has been installed on an Air France B 727 aircraft engaged in normal commercial operations serving the major European airports as well as the Middle East and North Africa. As in the Piedmont Phase I trials, the TCAS outputs will be available on the flight deck but only to an observer, not to the flight crew. Traffic and resolution advisories and other pertinent data will be recorded and off-line analysis carried out by the MITRE Corporation. The trials will extend over five months and it is expected that results will be available by the end of the year.

Ground-Based Collision Prevention Systems

A ground-based traffic advisory and collision prevention system was the objective of an earlier development in the United States (16). The more recent development of TCAS I and TCAS II provides an autonomous airborne system for separation assurance in which TCAS I is designed primarily to provide a limited traffic advisory service to general aviation aircraft (17). Nevertheless, the interest of providing a traffic advisory service from the ground to Mode S equipped aircraft is the subject of a new study within EUROCONTROL.

Ground-Based Traffic Advisory System. The availability in the cockpit of pertinent traffic information, without controller intervention, has a number of potential benefits. A significant improvement in visual acquisition performance has been indicated (18). This is of particular interest for VFR operations. In a future system using air-ground data link for the transmission of tactical ATC messages, a traffic advisory service may help to substitute for the loss of common channel information at present available on R/T.

The study of a ground-based traffic advisory system (GTAS) to be undertaken by EUROCONTROL will initially be concerned with the operational benefits to different categories of users and the airspace in which such services should be provided. It will also examine the compatibility of GTAS with visual flight rules and with ACAS. The constraints imposed by the radar and radar data processing system and by the performance of the Mode S data link will also be considered in the study. This initial phase does not include any equipment development or trials.

GTAS represents an application of Mode S which does not require a large proportion of the aircraft population to be equipped for benefits to accrue. If the service is available from the ground, any aircraft equipping will benefit immediately. The availability of such a service may also encourage airspace users to equip with Mode S transponders. A simple general aviation version with a small cockpit printer for presentation of traffic information can be envisaged.

Airborne Separation Monitoring

Proposals have been made in the past for an extension of ACAS capability to provide an Airborne Separation Monitoring (ASM) function in order to reduce separation minima in en-route airspace outside radar coverage, such as oceanic areas (19). This concept is the subject of a report to the ICAO SICAS Panel and may be developed further by other appropriate bodies in the ICAO forum. No particular studies are scheduled at the moment within EUROCONTROL on this application of the ACAS air-air surveillance capability.

Conclusions

The requirement for surveillance of civil air traffic in the controlled airspace in Europe is generally adequately met today by the ICAO standard secondary surveillance radar system backed up where necessary by primary radar. It is expected that the enhancements now being introduced will allow basically the same system to meet the surveillance requirements for some years and therefore no immediate operational requirement for SSR Mode S is anticipated in this region.

The aircraft identification reporting capability of SSR Mode S is recognised as one of its major surveillance features, which will provide a solution to the present difficulties encountered in Europe with the use of Mode A codes for identification purposes. Therefore the aircraft identification function will be a requirement for Mode S transponders when these become mandatory at least in the EUROCONTROL region.

The potential applications of the Mode S data link are now being studied and an extensive programme of work is underway to assess the operational benefits and define the technical requirements. Applications of particular interest include back-up to the R/T channel, to provide access in the aircraft to ground-based data banks and to provide the ATC system with air-derived data to enhance meteorological forecasts, aircraft tracking, etc.

It is generally accepted that airborne collision avoidance systems will enhance air traffic safety. A number of studies have been, or are being, carried out in Europe to assess the impact of ACAS on the ATC system, and to ensure that it will not perturb the SSR environment. The potential benefits of a ground-based traffic advisory system are being studied and any development by the ICAO community of an extended ACAS capability for airborne separation monitoring will be followed with interest.

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SESSION 23 ALL ELECTRIC AIRCRAFT

Chairmen:

Cary R. Spitzer
NASA Langley Research Center

This session addresses the emerging concept of an all-electric aircraft with reviews of current research on secondary power generation, power distribution and control, and electro-mechanical actuators.

84-2739

THE DÉ-JÀ VU OF ALL ELECTRIC/ALL DIGITAL AIRCRAFT

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Abstract

In two past studies of All Electric Aircraft, conducted by the Lockheed-California Company under NASA contracts, major pay-offs and benefits were identified, when aircraft using all electric technologies were compared with conventional aircraft, using hydraulics, pneumatics, conventional electrics, pneumatic (engine) starting and engine bleed air. One of the most rewarding benefits revealed by the studies was the elimination of compressor bleed from the engines, since aside from the major simplification to the power plant, the $\triangle$SFC and $\triangle F_n$ (thrust penalties) were found to be much less for shaft power extraction. Significantly, these penalties will increase more as the future advanced aircraft turn to the energy efficient engines (E^3) that have higher bypass and compressor ratios. Because of the ensuing small core flows, the extraction of high energy compressor bleed air tends to be prohibitive on these new engines.

In a most recent study, just completed by Lockheed-California Company and the Boeing Commercial Aircraft Company, the concept of an Integrated Digital Electric Aircraft "IDEA" was investigated and compared with a BASELINE aircraft. This recent study was directed towards an evaluation of the synergistic interaction of Advanced Digital Flight Control Systems (ADFCS), with the All Electric Airplane (AEA) technologies. This is the subject of this Paper and it discusses the improvements that have come about, since the earlier studies, largely because of the proliferation of electronic technologies.

The Dé-Jà Vu

When one talks about the dé-jà vu of All Electric Aircraft, we are reminded of science fiction writers such as Jules Verne, Isaac Asimov, Arthur Clark and others who were not scientific professionals but, rather individuals with a strong intuitive imagination and sense of things of the future. In retrospect, some of their intuitive forecasts of rockets, spaceships, underwater vehicles, jet-propelled man, and space travel showed an amazing sense of the future, since most all of the projections have come to pass, as a result of the technological progress over the past fifty or so years.

It is an amazing commentary to reflect on the fact that in World War I, airplanes were barely scraping into the air and the military offensive roles of these aircraft consisted merely of hand-dropping a small bomb over the side. About that time, the sober-minded scientist looked at the sound barrier as an inpenetrable constraint on the airplane development and upon high speed flight. As youths, we talked of splitting the atom and thought about the awesome energy that could be released, if it became possible to split the atom; enough energy to propel large ships across the Atlantic, plus other crafts. In the late 1920s and early 30s, space and space travel was still for the likes of the science fiction writer, since the professional scientist was more concerned with specific impulse and the type of propulsion system that could accelerate projectiles (and vehicles) up to escape velocity.

Yet with all the skepticism about man's role in space, all the above scientific barriers have fallen: the sound barrier has been broken and commercial/military now commonly fly at supersonic speeds. The atom has been split and, in the atom bomb, we saw its awesome destructive energy displayed in World War II. In the same war, Germany completed the development of the V2 bomb, which on a ballistic-trajectory (and an apogee of some 70 miles) was dropping on London and parts of England. These military projectiles were soon to be developed into the Intercontinental Ballistic Missiles (ICBMs), and the antimissile missiles. Then we witnessed the culmination of the prestigious U.S. program for placing a man on the moon and the success of the Mercury/Apollo Space Shuttle programs. And who will ever forget the resolution and beauty of those digitised colored photographs of Saturn (and her rings) that were transmitted through 886 million miles of space. As stated, these technological breakthroughs have all taken place in the short time frame of about 50 years and we can now marvel at them: Leonardo da Vinci certainly would be well pleased. Now, under government edict, we are looking to a star wars scenario!

When we come back to earth, and look at the more "mundane" but, nonetheless, still challenging technology of the commercial aircraft, the sense of dé-jà vu comes from the electric/electronic engineer, who wonders why it has taken so long for the aeronautical engineer (the chief designer) to recognize the potential of the Integrated Digital Electric Airplane: the "IDEAL" airplane in more senses than one.

Introduction

This Paper is an update on the progress of the application of advanced electric/electronic technologies to future commercial and military aircraft. The three Lockheed studies on this subject so far are References 1, 2, 3.

These three studies have addressed the application of advanced electric/electronic systems primarily to the next generation commercial transport aircraft, using advanced aerodynamics (supercritical wings), high percentage composites, energy efficient engines (E^3), fly-by-wire/ fly-by-light and power-by-wire flight control systems. The catalyst for the present program, and the previous studies, has been NASA's ACEE (aircraft energy efficiency) program, of which the E^3 program was a subset. Now the concern for aircraft energy efficiency has turned on the aircraft systems with the purpose of evaluating the contributions that could be made to NASA's fuel conservation objectives, by replacing the present multiple power systems, with a single type electric power system.

As described in three studies, significant benefits and payoffs were identified for the all electric/all electronic airplane. These

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benefits included reduced direct operating costs, reduced development/acquisition costs, reduced fuel costs, reduced maintenance support costs, reduced aircraft weight and increased aircraft/engine performance. Figure 1 is a reproduction of some of the financial benefits, as were reported in the second NASA/LRC study. This study evaluated three sizes of commercial advanced transport aircraft.

Aircraft Capacity (PAX)	Range (NM)	Fleet Size
150	1500	1000
350	4600	300
700	3000	250

A difference that contrasts the third NASA/Lockheed study from the previous two was NASA's requirement for trades to be conducted on the various subsystems, so that an optimum system could be selected for the IDEA. Another departure from the previous studies was that an ALTERNATE IDEA be studied in which advanced electric/electronic technologies could be used that could not be selected for the IDEA (because of the immaturity of these technologies for a 1994 certification date). The ground rules for the ALTERNATE IDEA were that this airplane would have the same payload and range as the IDEA, but it could use advanced electric/electronic technologies that might be considered too high a technical risk at this time, but which could bring major benefits and payoffs in the time frame beyond 1994.

IDEA Study

Working with the ground rules and premises of the SOW, the three aircraft evaluated in the study were:

BASELINE.

An advanced commercial and transport, with the most modern current technologies, e.g.,

- Major use of composites
- Energy efficient engines
- Advanced aerodynamics: supercritical wings and so forth
- Conventional secondary power system.

IDEA.

Same advanced technology aircraft with:

- All electric SPS
- Advanced DFCS
- Electric starting

ALTERNATE IDEA.

An advanced version of IDEA with:

- Most Advanced electronics/electronics (beyond the late 1990s)
- More advanced E^3
- Electric engine fuel/lube pumps

As a final note, the Lockheed-California/Lockheed-Georgia companies were joined, in this most recent study by the Boeing Commercial Aircraft Company, who worked to the same ground rules and premises. Boeing, however, addressed a smaller domestic commercial airplane of the 757/767 type,

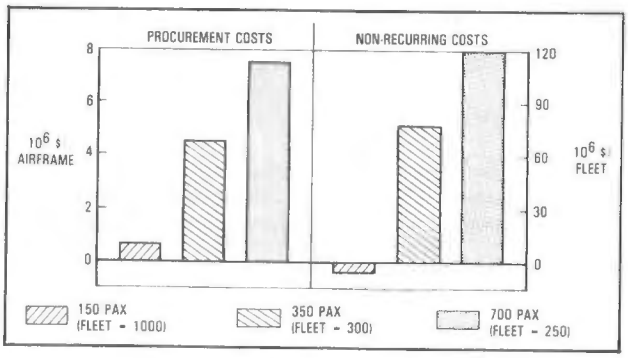

Fig. 1 AEA: Financial Benefits

while Lockheed addressed a large, longer range international aircraft. As far as possible, the two companies agreed to work with standard ground rules such as fuel price and so forth, and to use common costing/accounting procedures; the latter however proved to be difficult. There were in fact difficulties in working with a standard fuel cost, because of the differences between domestic and international fuel prices. As a result, a definitive comparison between the Boeing and Lockheed designs is not realistic, but a comparison of the benefits can be assessed in a relative sense.

Figure 2 is a two-view of the BASELINE airplane showing it as an advanced but conventional looking wide-bodied jet; it uses three advanced (E^3 type) high compression/high bypass ratio turbofans and supercritical wings. General Electric and Pratt & Whitney cooperated with Lockheed and furnished data on the E^3 technology power plants; GE data was however used for the inputs into the Lockheed Aircraft Systems Synthesis Evaluation Technique (ASSET) Program.

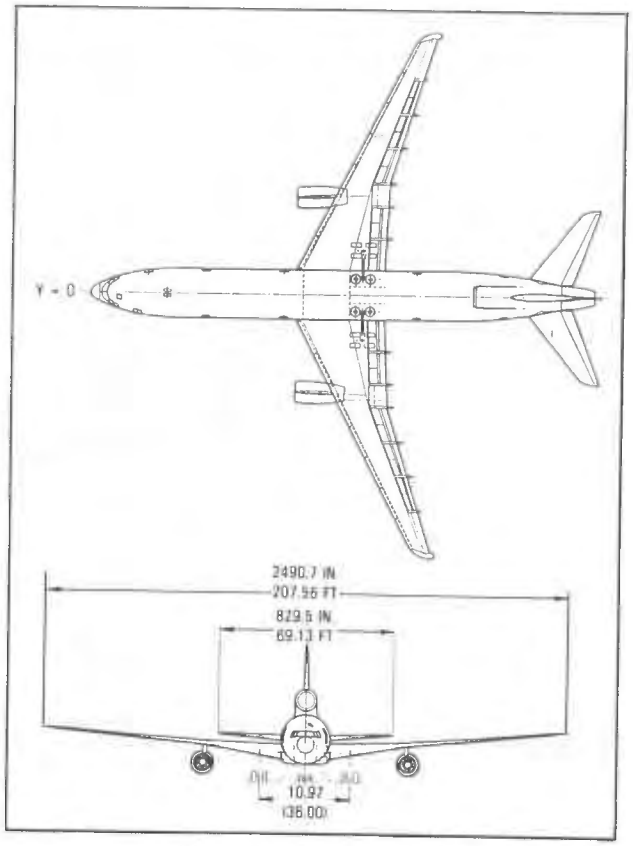

Fig. 2. BASELINE: Two-View

The new E^3 engine has an SFC of 0.55 so it is a measurable improvement over the turbofans in the current wide-bodied jets, which had an SFC of approximately 0.673 or higher.

Power Plant Configurations

One of the key aspects of the all electric/electronic aircraft is the consideration of fuel improvements that derive from using electric generators as the sole source of power in the aircraft.

BASELINE

Conventional Accessory Geabox (AGB) with:

- Engine lube pumps
- Engine fuel pumps
- Utility hydraulic pumps
- Pneumatic engine starter
- One CSBS (90/120kVA)

IDEA.

Austere AGB with:

- Engine lube pumps
- Engine fuel pumps
- Two electric starter-generator (150/200 kVA)

ALTERNATE IDEA.

Austere + AGB with:

- Two starter-generators (220/275 kVA)

It is clear from the above that the airplanes become pregressively "more electric" as they move through from the BASELINE to the ALTERNATE IDEA.

Flight Control Technology

For the previous NASA/Lockheed studies, fuel conservation was the primary objective and this was the case with the latest NASA/Lockheed AEA/IDEA study. Thus, in addition to the systems/equipment weight savings, the AEA/IDEA configured airplanes highlight the advanced flight controls and the fuel savings that derive from the improved efficiency of the engine power extraction method (mechanical versus engine bleed air).

The new study continued to show the fuel savings that derive from the digital flight control technology when the IDEA operates in conditions of relaxed and negative static stability. As stated, the additional benefit of flying the airplane with aft c.g. locations is a smaller tail. When the airplane operates at say + 14 percent static stability, a large down force is required on the tail to counteract the down pitching moment of the fuselage. When however the c.g. moves aft to a position equivalent to neutral stability, the required down force vector decreases and, if it is taken further aft of neutral, the vector actually reverses, to create a lifting force on the tail. When this occurs, the angle of attack (α) decreases and the lift induced drag on the wing decreases. These are all complementary effects, that result in a reduction in the airplane's total drag and, consequently, a decrease in engine thrust/fuel consumption.

Figure 3 is a schematic of an automatic c.g. positioning system proposed in the IDEA (and the previous AEA program) in which a slipper tank (containing fuel) was installed in the vertical stabilizer. This adds to the fueled-weight of the aircraft, but is is more than offset, by the mission fuel weight

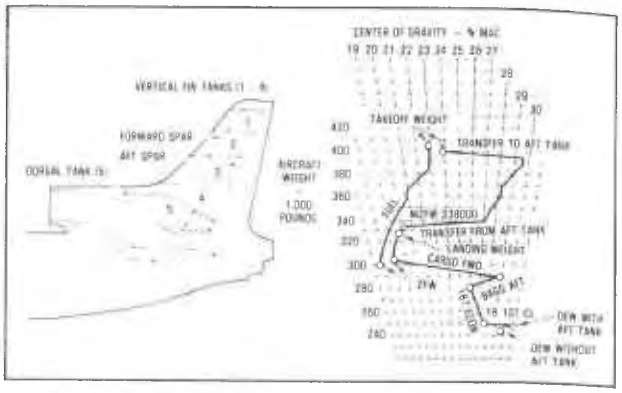

Fig. 3. Pitch Axis Control System CG Management

savings. Fore and aft fuel pumping is accomplished automatically as a function of the flight profile segment: at takeoff, fuel is pumped aft to assist in the rotation of the aircraft (after takeoff) and, in the approach (after landing) fuel is pumped forward. In between these two conditions, the fuel is discretely moved in accordance with the curve plot shown in Figure 3.

Wing Technology

A high wing aspect ratio (AR) has always been known to have a favorable impact on mission fuel load and, as shown in Figure 4 in a typical large wide bodied transport, the minimum point on the fuel cost is shown at AR of about 12. The cost also shows that if the AR increases beyond 12, the fuel benefit begins to diminish since, as the lower curve shows, a minimum weight wing favors lower ARs: therefore the 12:1 becomes a compromise. However, if a design predicate is that wing AR can be increased (to say 14 or 15) without weight increase, then we could achieve a good fuel saving, without the weight penalty. Unfortunately there being no panacea, such a lightweight wing would have a propensity for flutter so, here again, advanced ACT electronics must be used to suppress this incipient flutter condition. Clearly, the ACT flutter suppression requirements will increase the bandwidth (frequency response) of the electronic FCS and the Electromechanical Actuators (EMA) of these systems, but these are within their projected capabilities.

Figure 5 is a projection of the benefits that will derive from such an improved Integrative Active Control System (IACS). The upper curves show the improved ride and handling quality when the IACS is added to the BASELINE aircraft. The center curve shows the high oscillatory (flutter) response of the wing without the IACS, and the lower curve shows the improved aeroelastic response/reduction in the wing (dynamic) bending moments with the IACS. Figure 6 amplifies the above

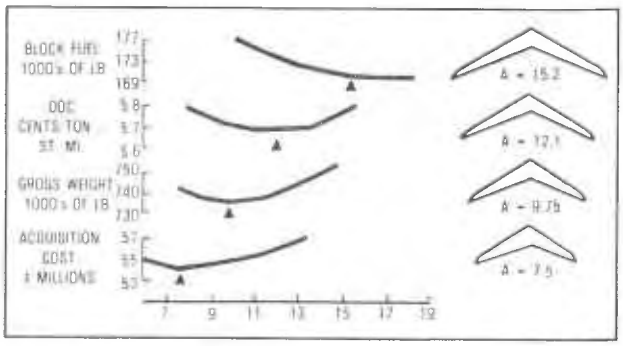

Fig. 4. Design Aspects of Wing Aspect Ratio Transport

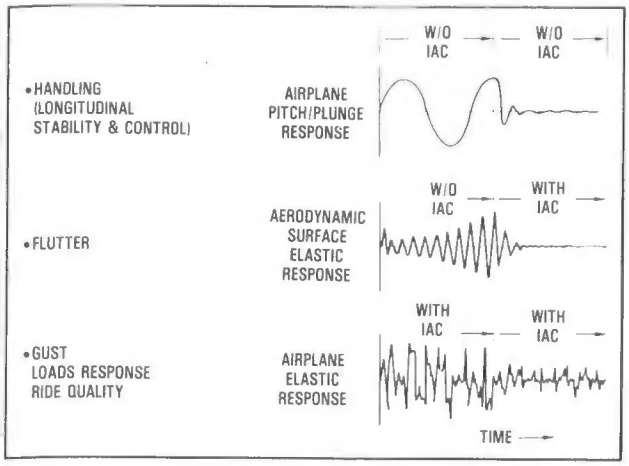

Fig. 5. Integrated Active Controls System (IAC)

performance benefits from GLA in the IDEA configured vehicle as compared to the BASELINE. As shown, the dotted curve shows the nonlimited outer wing shear and bending moments compared to the much reduced levels in the IDEA, indicated by the solid lines. These, then, are the future projected benefits of the advanced electric/electronic technologies.

Other significant fall-outs of the ADFCS are the ability to incorporate Gust Load Alleviation (GLA), Maneuver Load Suppression (MLS), Elastic Mode Suppression (EMS), and Flutter Mode Suppression (FMS). Many of these features such as GLA and MLS are already in place and, in the future aircraft, advanced lead-sensors could monitor the environmental conditions ahead of the aircraft, so that Active Control Technology (ACT) might permit a lowering of the structure design limits on the aircraft (to effect further structural weight savings). These additional benefits deriving from the advanced all electric/all electronic (digital) systems were not factored into the IDEA configured transport, but they represent another endorsement of the benefits and payoffs that are resident in the all electric/all electronic aircraft technology.

Engine Power Extraction Sensitivities

In the GE E^3 FPS-9 design, a 1.5 lb/sec IP bleed on the engine (at 0.82 Mach Number and 35,000 feet) results in an approximately 2.14 percent △SFC penalty, while a 150 hp (comparably equal to 1.5 pps) is only about 0.85 percent △SFC. This represents an approximate 2.5:1 improvement.

Figure 7 shows that at the same 0.8M/35,000 foot condition, 1.5 pps creates a 4.22 percent thrust loss while the 150 hp creates only a 1.53 percent thrust loss. Thus the horsepower thrust loss of the 1.5 pps bleed at an aircraft velocity of approximately 800 f/s is 0.0422 x 7200 x 800/550 = 442 hp/engine (7200 = engine cruise F). In contrast the 150 hp power extraction impact is only 1.53/4.22 x 442 = 160 hp/engine. Therefore, if the power difference is assumed to prevail over an 11 hour (intercontinental) flight time, the energy difference would be 11 x 3 x (442 - 168) = 9306 hp/hr. This shows impressively the energy efficiency difference between the IDEA and BASELINE, when considering the ECS cruise power demands only.

Environmental Control System (ECS)

Of all the systems in the aircraft, the ECS and the engine starting systems are the most influential in sizing the electrical capacity of the generators. In fact, for the large commercial transport carrying 350 to 500 passengers, the total electrical

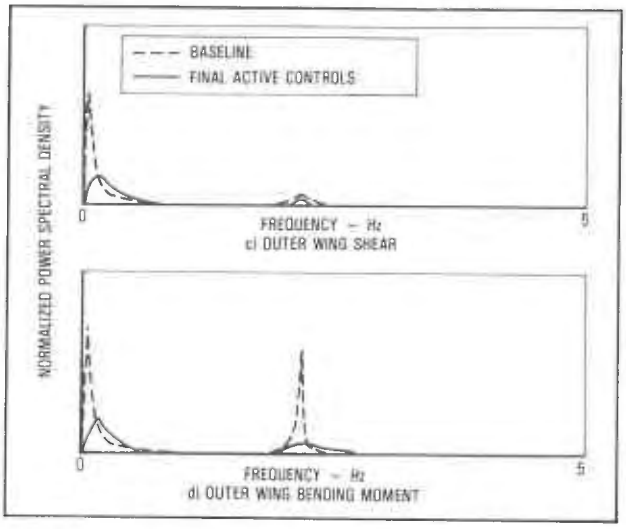

Fig. 6. Typical Wing Gust Response Loads Comparisons

power requirement to provide cooling for a fully loaded airplane (on a 104°F hot, humid day condition) presents an almost untenably high load to the aircraft's generator/APU systems. It is also a power demand that is well beyond the capacity of any airline ground power system today. There is, therefore, the important message that if AEA and IDEA are to be phased into the airlines' aircraft inventory, then the industry must initiate immediately technology-readiness plans, to ensure the availability of much larger capacity ground power systems in the early 1990's time frame.

For the IDEA and previous NASA/Lockheed studies, a minimum cabin ventilation requirement of about 20 cfm/pax (passenger) was provided: this is equivalent to an equivalent total air mass flow of approximately 600 ppm (350 x 1.76). When designing a motor driven air cycle system to provide the necessary amount of cooling (approximately 376,000 Btu/hr), the horsepower rating for each of three ECS packs (including the benefit of power recovery from the cooling turbines) was some 243 hp/pack. This is a total of 729 hp (or 543 kW), which clearly poses a major power demand on the airline's ground power systems.

To ameliorate these problems, innovative solutions must be brought to the design of new (all electric) air conditioning systems. One of the more basic considerations might be to reduce the present objective of providing 50 percent (outside) fresh air or, at least, to do this on the hot humid days. If a 100 percent recirculation could be considered on these days, the

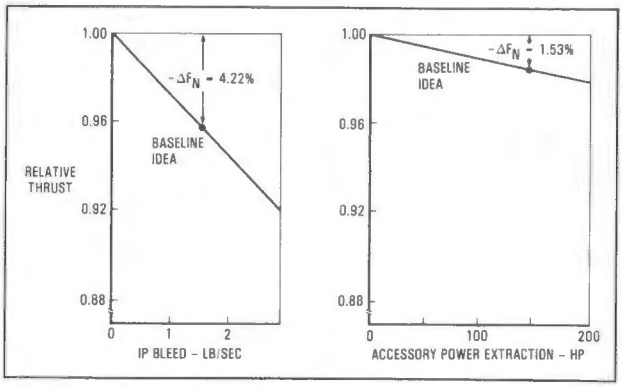

Fig. 7. E^3 (FPS-9) Engine Thrust Sensitivities

latent heat load could be reduced by some 24 tons (out of a total of 76 tons). Another approach might be to consider a 100 percent vapor cycle system, which while much more efficient, is more costly and somewhat less reliable than the air cycle system: it would however have a much lesser power demand. For example, the same cooling load could be furnished by three ECS packs of approximately 112 hp each for a total of 336 hp, or 250 kW. This is still high, but it is much less than the previous 543 kW.

Reference to Figure 8 shows the various flow pressure, temperature and humidity conditions, based on three ECS packs each providing 200 ppm at a temperature of about 40°F. For the hot 104° day with humidity ratio conditions of 130 gr/lb, the total sensible and latent heat loads/pack are 17.5 tons and 8 tons respectively.

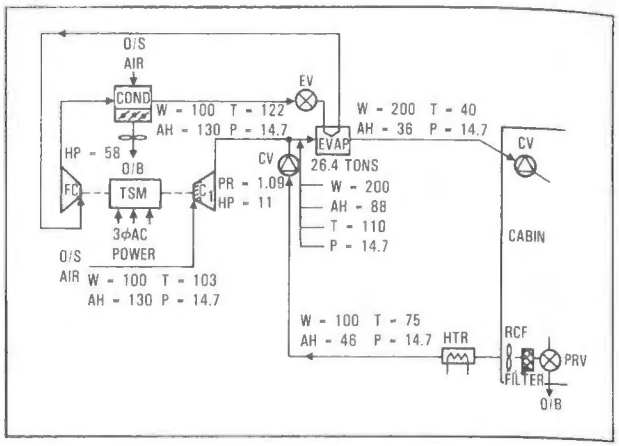

Fig. 8. IDEA: ECS Schematic

Electromechanical Actuation System (EMAS)

The NASA/Lockheed IDEA study required trade analysis to be performed on alternative electromechanical actions systems, that would replace the hydraulic mechanical action system (HMAS) in the BASELINE configured aircraft. All mechanical functions were therefore identified and specifications/ technical briefs were written to define the actuation requirements. This was done but, in accord with the NASA work statement, primary emphasis was given to the FCS actuators. Further, it was a specific directive that particular attention be given to the supporting electric power system to ensure that the 10^{-9} reliability objective of the FCS/EMAS would not be abrogated by the electric system. It is of note that the Lockheed-Georgia Company, who have a special expertise in the design and implementation of digital flight control systems, were given the responsibility for this important part of the NASA/Lockheed IDEA Study. The EMAS responsibility was however retained by the Lockheed-California Company.

Table 1 shows the specific performance requirements, that were given to the suppliers for the primary flight control actuators on the 350 PAX international range aircraft. The primary responders to these technical requests were Sundstrand Aviation and MPC Products, Inc. Each of these suppliers selected SmCo drive motors and the usual electronic power controllers. The supplier approaches were different to the extent that MPC Products responded (at Lockheed's request) with a jam-proof actuator design, while Sundstrand responded with a conventional EMA design (also at Lockheed's request). Figure 9 is an outline drawing of the MPC actuator designed for outer aileron which uses a primary and a secondary motor that operates into an eccentric. It was difficult to make a good comparison between the two suppliers' designs, but the philosophy was to obtain a comparison between a jamproof and nonjamproof design in terms of weight and other factors. The following FCS actuators were designed for the Lockheed IDEA.

Control Surfaces	Number of Actuators
Horizontal Stabilizer	Four Actuators/Flying Tail
Outboard Ailerons	Two/Surface
Inboard Ailerons	Three/Surface
Rudder	Three/Surface
Spoilers (6 Per Wing)	One/Surface

FLIGHT SURFACE	SPOILERS 1	2	3	4	AILERONS 5	6	STABILIZER/ I/B	O/B	ELEVATOR	RUDDER	NOTES
LOADS: FT LB											
• STALL	9.8	4.7K	4.2K	2.7K	3.2K	1.9K	5.9K	7.3K	80.2K	9.7K	1. EXCEPT AS NOTED OTHERWISE, VALUES SHOWN RELATE TO SINGLE ACTUATORS.
• DESIGN	6.5K	2.5K	2.2K	1.42K	1.5K	0.86K	4.0K	4.7K	20.0K	7.2K	
RATE: DEG/SEC	60	60	60	60	60	60	35	35	7.3	30	2. SPOILERS HAVE DIFFERENT AMPLITUDES DURING DIFFERENT OPERATIONAL MODES.
DISPLACEMENT (MAX)											
• DEGREES	-60	-60	-60	-60	-60	-60	±20	±20	+1 -14	±30	
• INCHES	5.59	5.59	3.05	3.05	2.65	2.65	±2.48	±1.46 RET ±1.38 EXT	38.62	S 25.3 L 30.0	3. RUDDER HINGE MOMENT LIMITED TO 5000 fp AT 260 kCAS: MAX./8° FLAPS UP.
FREQ. RESPONSE											
• BANDWIDTH (-3dB)	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	2.2	1.6	4. MECHANICAL SHEAR-SECTION REQUIRED AT 100 kfp IN STABILIZER ACTUATOR OUTPUTS.
• AMPLITUDE (DEG)	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	0.3	1.0	
MIN. SERVO STIFF (IN.LB/DEG)	6.3K	6.3K	1.75K	1.99K	1.23K	1.68K	3.49K	8.7K	2.61×10^6	60K	5. VALUES SHOWN, PER ACTUATOR, ARE MAXIMUM (UNDER ANY FAILURE MODE).
INERTIA (IN.LB.SEC^2 (SURFACE)	89.8	69.4	10.2	19.7	23.1	17.8	3.18K	1.28K	41.5K	0.629K	
NO. OF ACTUATORS	1	1	1	1	1	1	3	2	4	3	6. LINEAR TRAVEL RELATES TO HYDRAULIC ACTUATORS. SAME AS L-1011-BASIC EXCEPT FOR STABILIZER/ELEVATOR.
RESOLUTION (DEG.)	0.25	0.25	0.25	0.25	0.25	0.25	0.1	0.1	0.01	0.1	7. RUDDER DEFLECTION 3.5° AT 350 KCAS.

Table 1 EMAS Design/Performance Data

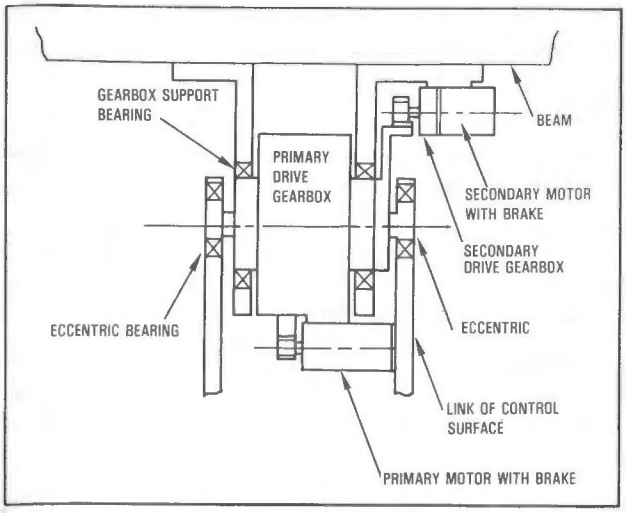

Fig. 9. EMA with AntiJam Feature (Courtesy MPC Products)

In addition to the specific actuator designs, Lockheed-California Company conducted the NASA required trade analysis on the different candidate systems. Pursuant to this, some 44 configurations of EMAs in eleven categories were evaluated. It is not possible in this Paper to discuss adequately all the designs, but of the nonconventional types, the eccentuator was identified as one that affords some novel advantages.

The most attractive feature of the eccentuator is the fact that the actuator has a variable mechanical advantage (MA), as depicted in inset diagram of Figure 10. For approximately $\pm$ 35° around neutral, the actuator has an MA of about 10, but near full deflection (where the maximum hinge-moment occurs), the MA approaches infinity. It can be seen from this that if the surface has to be held in deflections, near maximum hinge moment, the currents in the electronics and the motor stator can be significantly decreased. This, therefore, becomes a very synergistic aspect of the eccentuator when interfaced with the motor and power electronics. In contrast to these advantages, the eccentuator is limited to surface deflections of about $\pm$ 28°.

Electric Power Systems

NASA-LaRC, having placed emphasis on the reliability of the digital flight control system, was most concerned that the electric power system did not abrogate the 10^{-9} reliability objective

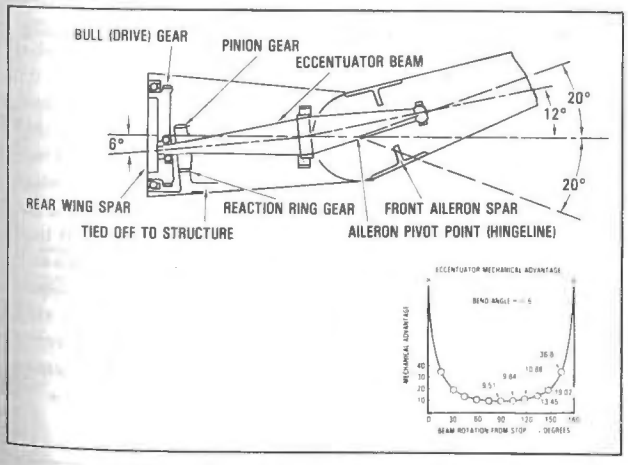

Fig. 10. Eccentuator Installation

for the complete DFCS. Pursuant to this, the RFP Statement of Work (SOW) called for a trade analysis of the candidate advanced power generation systems. These were as follows:

- Advanced Hydromechanical CSD (Constant Speed Drives) (Sundstrand)
- VSCF Cycloconverter (General Electric)
- VSCF dc Link (Westinghouse)
- 270 Vdc (NADC/AiResearch)
- VVVF (Variable Voltage/Variable Frequency)
- 20 Hz Power Transmission (NASA-Lewis)

The first three of the above systems are well known throughout the aerospace electrical industry, but the preponderance of experience is with the Sundstrand hydromechanical drive system.

CSD Systems

The CSD systems are used in practically all aircraft throughout the world and they are manufactured primarily in the United States, although Lucas Aerospace (GB) supplies the European market, under a Sundstrand license. This latter company has in fact developed an advanced lightweight/high speed, 24,000 rpm CSD configuration, in which the primary elements of the drive are accommodated within the hollow rotor shaft. The main rotor shaft therefore has high stiffness and high structural integrity. In recent years, Sundstrand's CSDS was selected for the Boeing 757/767 aircraft, so it is clear that the CSDs (which have had a somewhat difficult development history) are still highly competitive with the VSCF systems and they still dominate the aerospace power generation system market.

VSCF Cycloconverter

The VSCF power systems (cycloconverter and dc link types) have each reached an advanced maturity status that merit their consideration in new advanced aircraft. The VSCF cycloconverter system has been the beneficiary of the most laboratory and flight experience. It was also selected in a 60 kVA configuration as a starter-generator for the Air Force A-10 aircraft. Unfortunately, this program is now in a hold-phase, but the cycloconverter has been used on the A4D and it was selected as the primary power system on the F-18 aircraft. Extensive laboratory testing under AFWAL contracts culminated in the successful development of a 150 kVA starter-generator configuration, which was built and demonstrated for starting high bypass ratio engines in the 48,000 pound SLS class. The General Electric company and Rolls Royce have also examined the feasibility of integrating a large samarium-cobalt generator inside the engine by mounting the generator rotor over the high-pressure spool shaft. Figure 11 is a schematic of the Rolls Royce configuration.

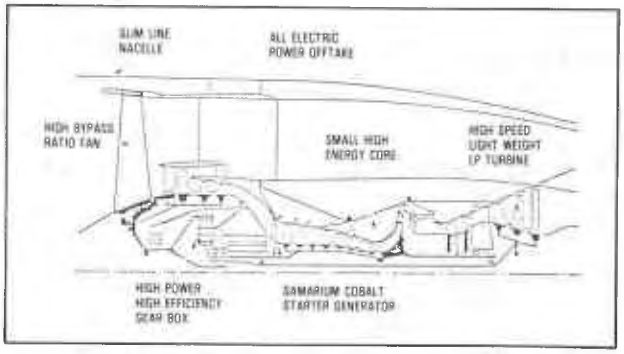

Fig. 11. Engine Integrated Starter Generator (Courtesy Rolls Royce)

VSCF (DC Link)

The VSCF dc link power system (like the cycloconverter system) is a highly mature technology, but unlike the cycloconverter VSCF, it does not require high generator speeds and frequencies (of 1.2 kHz/2.4 kHz). As proposed by Westinghouse, this system can use conventional frequencies of 400 Hz, 800 Hz or other frequencies, since the power is merely rectified to 270 Vdc and then inverted to the required constant frequency output. A claimed advantage of this system is that with the emergence of high voltage/high current transistors, power systems in the 60 to 120 kVA capacity can now be built whereas the dc link systems were originally limited to the lower capacity systems of 20 to 40 kVA capacity. Westinghouse claims that the VSCF dc link is more reliable because the inverter uses only six power switching transistors compared to 36 SCRs in the cycloconverter VSCF system. Other disadvantages leveled against the cycloconverter system is the need for shielded cables, and larger ratio of generated kVA to bus kVA.

270 Vdc System

The 270 Vdc system is a U.S. Navy/NADC development in which the variable frequency/variable voltage output of a direct engine driven generator is rectified to 270 Vdc; power for three-phase 200 V/400 Hz ac and 28 Vdc is inverted and converted on an "as required" basis.

The primary advantage of the system is that it is a very simple form of "constant power" generation from a "variable speed" power source. As such, it is not unlike the earlier 28 Vdc systems, where the dc generators maintained a constant dc voltage over a 4:1 engine need range. The writer was involved with a constant 112 Vdc voltage and a 28 Vdc power system in the Bristol Brabazon and Bristol Britannia aircraft, which were designed in the early post-World War II period, as commercial airliners. For these aircraft, power was obtained from (stepped variable voltage/variable frequency generators).

Some other advantages of 270 Vdc are the ease of paralleling and, more importantly, the ability on aircraft carriers, to derive 270 Vdc power from three-phase 200 V 60 Hz power (which is readily available). The disadvantages of 270 Vdc are that the dc power cannot be used directly to drive any brushless dc motor so every motor must utilize an inverter to synthesize three-phase ac power. The more serious problem however, of high voltage dc systems is the concern for dc power contactors and relays which must have high rupturing capacities. This latter problem has led to the development of solid state and hybrid devices of somewhat esoteric design.

VVVF System

The VVVF (V^3F) powered system is a variant of the dc link VSCF in that it uses a variable frequency/variable voltage generator, but it inverts only a small percentage of it to CVCF and 270 Vdc (on an as required basis). The major part of the power is therefore used directly for heating, lighting, galley, deicing and many motor loads, viz: flaps, slats, landing gear, cargo/passenger doors, inlet doors. It is also possible to power directly the large motors required for the Environmental Control System (ECS) as required in the NASA/Lockheed IDEA configuration. The V^3F was therefore selected for this aircraft since it has particular merit in large All Electric Aircraft, where the generator capacities in each power plant may be of the order of 350 kVA and higher. Also, since the generators double as engine starters, the large compressor drag torque additionally requires a generator of this size. The other main attributes of the V^3F system are that by the use of phase delayed rectifiers (as dedicated separate assemblies or electronic "front-ends" in inverters). It is possible to maintain a constant level of 270 Vdc (or other voltage value), over the complete speed range of the engines. Thus, the DFCS and the FCS servo actuators can be powered by a "constant-power" system, whose performance is independent of the varying speed and frequency of the primary generators.

Interpolating between Figure 12a and Figure 12b, it can be seen that a constant speed pump designed for the maximum fuel flow demand (at takeoff) delivers a very high (unusable) pressure at low fuel demands. In contrast, the VV/VF motor pump pressure/flow characteristics are more compatible with the engine's flow demand, so it operates more efficiently over the speed range, than a constant speed pump

20 kHz Power System

The NASA-Lewis Research Center is the primary sponsor of this system and it is a system that is presently without flight or substantive laboratory experience. The claimed advantages of this system find their origin in the impressive development now going on in the solid state converters and, more pertinently, the high frequency switching type inverter/converters. The principle of the system is that high frequency power is obtained from power conversion of engine driven induction generators, or more conventional solid rotor PM generators. With high-frequency power distributed through the airplane, conversion, inversion and rectification of the 20 kHz power is accomplished on a dedicated conditioning basis for specific loads, or on a subsystem basis. In the latter case, some percentage of the power would, for example, be converted to three-phase 200 V 400 Hz for motor and other CVCF loads in the airplane.

It is of note, in this system design, that NASA-LeRc used engine driven compressors for the ECS and that the APU was deleted from the airplane. On these premises, NASA-Lewis identified the various favorable aspects of the system and showed the benefits to be comparable to the other All Electric Airplane Studies. For their in-house study NASA-Lerc selected a 767 type airplane for which Boeing supplied the necessary load data.

The advantages claimed for the resonant mode power switching converter are that the inductive/capacitative circuit has low dynamic resistance and therefore high efficiency (due to low I^2R losses). It also permits the selecton of the high frequency of 20 kHz power-switching mode, so, that the size of filters

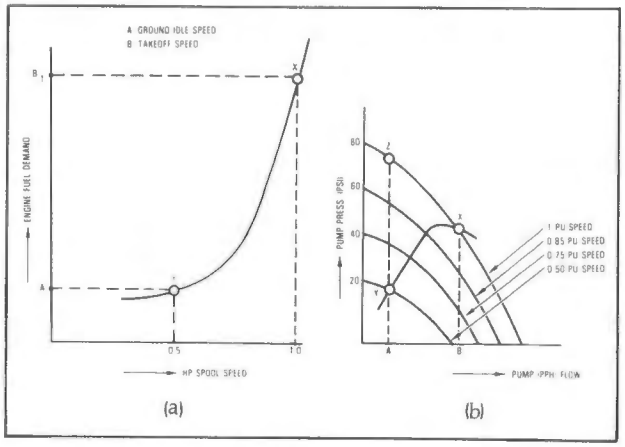

Fig. 12 Engine Fuel Pump vs. Speed Characteristics

transformers, and so forth are minimized. However, in regard to the former, the low dynamic resistance means low damping so the stability and loop dynamics of the resonant mode converter must be cicumspectly designed. Other design aspects relate to the use of the converters as common power sources for the (diverse) linear and nonlinear loads in the aircraft. When these converters are dedicated to a single load, it is possible to design and match the converter characteristics to that of the load but, in the system proposed, the converters must act a common primary power source (for many different type loads). As a result, there may be incipient problems since the acceptor, or rejector, resonant circuits could be de-tuned by the in-line harmonic currents flowing to nonlinear loads. A further aspect of high frequency is the problem of skin effect and distribution cable impedances that would necessitate the design of special cables. A conclusion of the Lockheed study, therefore, was that while the 20 kHz power system had some attractive prospects, it lacked the necessary background experience and development status to be considered for the IDEA application.

Program Summary

The NASA-IDEA Study represented another step towards a further validation of the concept of all electric aircraft using advanced electric and electronic technologies. Specifically, the Study generated a more in-depth evaluation of Advanced Digital Flight Control Systems (ADFCS), which though not described in design detail in this Paper is covered by the Lockheed-Georgia Company in the final NASA-LaRC report. However, the point was made in this Paper that the ADFCS is key to the achievement of very attractive fuel gains that derive from the ability to operate the IDEA under conditions of RSS and negative static stability. These latter systems require a highly reliable Pitch Active Control System (PACS); also, the use of Integrated Active Control System (IACS) will bring about other major improvements in the integration of the flight controls/propulsion systems.

Insufficient attention was given to the intriguing aspect of the ALTERNATE IDEA, as it is an aircraft configuraton that is worthy of more attention than was given in the Study. There is no doubt that while one does not normally view the "systems" as having impact on the external geometric configuration of the airplane, it is possible to project that such could be the case. It was shown during the Study that, the use of advanced electronic sensors (which could give lead information to the FCS) could permit the airplane to be designed with lower structural load limits. The IDEA design followed conventional practice using a 2.5 g load factor but, if the airplane could be operated as a stable platform by using the lead sensors to detect unstable air conditions (as well as collision hazards) ahead of the aircraft, the load factor might be reduced to 2.0 g (or even 1.5 g). This means that as the load factor decreases, the minimum point on the fuel vs. AR curve (Figure 4)decreases. Assessments were made of this and it was found that for a 2 g load factor, an AR of about 14 yielded an approximate 4.3 percent fuel improvement: a 1.5 g load factor permitted an even higher AR of 15, providing better than an 8 percent fuel reduction. There is also the fact, already mentioned, that a sophisticated electronic flutter mode suppression system might permit the use of a lighter than normal wing structure. This wing would have a propensity for flutter (without the active flutter suppression system) but with IACS,load factors would be held within limits by the advanced DFCS.

Benefits and Payoffs

As in the previous NASA/Lockheed studies, weight reduction was a primary goal because when the net savings are cycled to assess the impact on the airplane's operating empty weight (OEW) and fueled weight, the net savings are magnified. Some of the major net weight savings were:

• Hydraulic System Elimination	2823 lb
• Flight Control	1404 lb
• Air Conditioning	2334 lb
• Other	473 lb
Systems Weight Saving:	7034 lb

In the bookkeeping, some miscellaneous aircraft weight savings (not included in the above) included the landing gear, austere gearbox, thrust reverser and engine starting. A further 1458 pound saving was identified for these systems to yield a total net weight saving of 8492 pound: corresponding to about a 3.4 percent of the OEW.

Fuel saving is the other key parameter of assessment of the IDEA and All Electric Aircraft in general. Here, the engine bleed elimination yielded -2.4 percent, c.g. management/trim drag reduction/tail size reduction, -5.7 percent, structural weight reduction, -3.4 percent. The total fuel reduction was therefore some -11.3 percent for the IDEA.

For the ALTERNATE IDEA, the following relates to the change in maneuver load factor (MLF).

Configuration	MLF	Wing Wt	Fuel
IDEA	2.5g	49,069	Base
ALT. IDEA	2.0g	42,479	-3.0%
ALT. IDEA	1.5g	35.393	-6.1%

In summary, it can be noted that the Study resulted in another reaffirmation of the fuel/weight saving benefit and a reduction of 7 percent in maintenance support costs of all electric/electronic aircraft. There are, in addition, other benefits in terms of engineering development and acquisition costs that are not covered in the Paper.

In regard to the ALTERNATE IDEA, that was not given the challenging/innovative design consideration it deserved, it can be said that NASA's objective to identify advanced electric/electronic technologies "---to permit an aircraft design not heretofore possible" is realistically achievable. It has not been discussed, but there are possible and challenging applications in the future for the consideration of hybrid electric propulsion systems in which the 6000 to 12,000 shp turboshaft engines now being developed can be considered as drive sources for the multimegawatt size generators, already available in the marketplace.

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AN ASSESSMENT OF THE 1990 DIGITAL/ELECTRIC AIRPLANE

84-2740

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Abstract

The application of advanced systems technology has shown increasing promise for significant potential gains in airplane performance and efficiency. In late 1983, NASA initiated the Integrated Digital/Electric Aircraft (IDEA) study programs to determine the impact of extensive use of advanced electrical and digital systems on future aircraft. The first objective of the IDEA program was the broad evaluation of improvements in airplane performance and economics resulting from the integrated introduction of digital controls and advanced electrical systems. The second program objective was the definition of research and development areas required to achieve the projected improvements. A baseline configuration was compared to the new IDEA configurations in terms of economic performance, fuel efficiency, and significant system and airplane configuration characteristics. Important factors (weight, reliability, maintainability, cost, performance, survivability, and environmental constraints) were determined and compared to form the basis for recommending the research and development necessary to implement IDEA concepts. Based on these developmental needs, research programs were recommended for high-risk, high-payoff areas appropriate for implementation under NASA leadership. The 1990 Baseline configuration represents a 6% to 8% fuel burn improvement over current technology. When compared to the 1990 Baseline airplane, the IDEA airplane systems showed a 1.8% improvement in direct operating cost (DOC) and a 3% improvement in fuel burn performance. In addition, significant economic improvement was apparent when the total operating cost was included.

Introduction

This paper presents an assessment of the digital/electric airplane concept. Various measurements of acceptability, such as the impact on DOC, will be used not only to evaluate the impact of concept application, but, more basically, to examine the realistic probability of that application taking place by 1990. A brief description of the IDEA study and its results is presented here as a basis for assessment.

Generally speaking, this study was a nine-month investigation of integrated digital/electric concepts. Besides the data generated for the study itself, a large amount of data generated for other in-house IR&D studies was also incorporated. Considerable supplier support was included as well. The performance and economics of an IDEA configuration and an alternate IDEA configuration were evaluated to determine the potential benefits of such concepts and to identify the research and development required for potential application to transport aircraft in the early 1990s. To determine the benefits of the digital/electric concepts, the IDEA configurations were defined and compared to those of a reference baseline configuration. The selected Baseline configuration was an alternate version of the 767 used in a recent NASA active controls study program and modified incrementally to include the following 1990 technologies:

- Active controls
- Energy Efficient Engine (E^3)
- Advanced supercritical wing
- Composite structures
- Other certifiable new technologies

The baseline systems were those expected to be used in 1990 if IDEA-related research and development were not accomplished. Figure 1 presents an illustration of the Baseline configuration.

The next task was to apply the IDEA concepts and system features to the Baseline configuration and develop a new configuration. A series of major subsystem trade studies was conducted in the flight controls, actuation, electrical system, and data distribution technology areas. The preferred subsystem designs were selected and incorporated to establish the IDEA configuration.

Concurrent with the IDEA configuration definition, an alternate (a possible future turboprop, illustrated by Figure 2) was defined and investigated to the extent possible within the scope of the study.

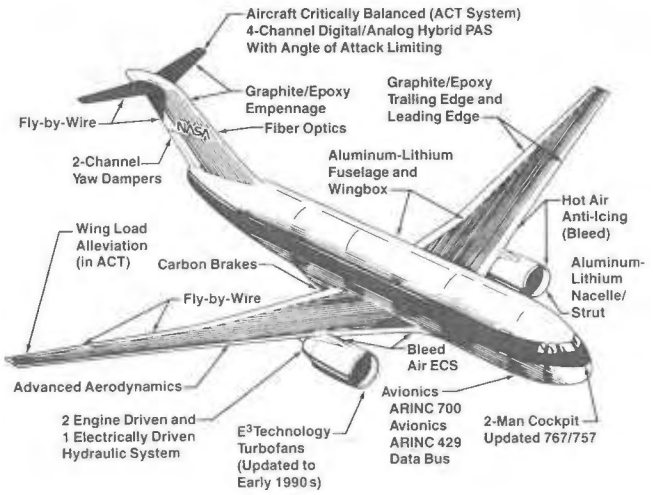

Figure 1. Baseline Configuration for IDEA Study

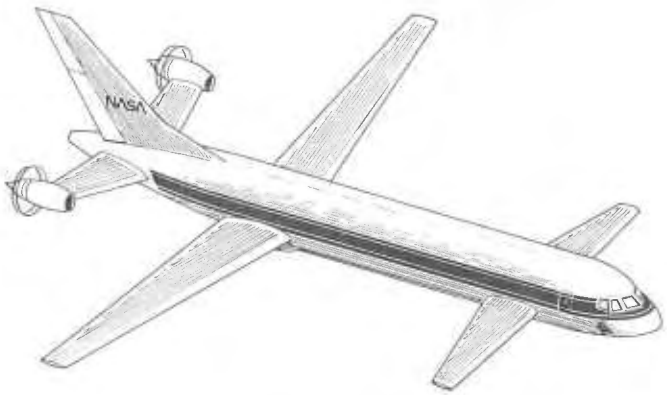

Figure 2. Alternate IDEA Airplane Configuration

The IDEA configuration included the following additional technologies:

- Digital fly-by-wire flight control system with electromechanical actuators and no mechanical backup
- Electrically driven environmental control systems
- No engine bleed for hydraulic or pneumatic power
- Electric starting
- Nonhot-air cowl and wing deicing
- Other related system concepts

During the development of the various study configurations, major decisions affecting the selection of specific options were based on trade studies and other related study results. For aspects of the study that could not receive lengthy attention, it was often necessary to base decisions on engineering judgements or standard approaches for typical applications. Once the Baseline configuration, the IDEA configuration, and the alternate IDEA configuration were established, they were compared in terms of economic performance, fuel efficiency, and significant system and airplane configuration characteristics.

In comparison to the Baseline configuration, the IDEA configuration resulted in a weight reduction of 3180 lb (see Table 1); a 3% decrease in fuel burned for a 1000-nmi segment at the same payload and range conditions; and a corresponding improvement in DOC of 1.8% (Fig. 3 and Fig. 4). It should be noted that the Baseline configuration resulted in a significant improvement of fuel burn, 6% to 8%, over current technology.

Table 1. Weight Comparison, IDEA vs Baseline

Total Systems Delta Weight (lb)			-3180
Equipment Delta Weight		-1740	
Remove Hydraulic System	-2480		
Revise Surface Control System	- 20		
Revise Landing Gear/Thrust Reverser Control	0		
Revise Electrical Power System	+ 850		
Revise Avionics System	- 70		
Remove Pneumatic System	- 820		
Revise Environmental Control System	+ 1080		
Revise Anti-Ice System	+ 40		
Revise Engine Starting System	- 90		
Revise Auxilary Power Unit	- 230		
Wire/Support/Connectors Delta Weight		-1440	
Data Bus Control System	-1250		
Double Voltage Power/Distributed Load Centers	- 40		
Remove Hydraulic/Pneumatic Wire	- 150		

When the Baseline was compared with the alternate IDEA configuration, an advanced technology turboprop, the result was an even greater potential benefit (Fig. 3 and Fig. 4). Although much of the benefit was due to propulsion technology, it should be noted that the digital/electric systems supported these potential propulsion benefits as well as increased secondary power system efficiency. Important factors (weight, reliability, maintainability, cost, performance, survivability, and environmental constraints) were analyzed to form the basis for recommending the research and development necessary to implement IDEA concepts. Recommended research programs were defined for high-risk, high-payoff areas appropriate for implementation under NASA leadership.

Together, the various IDEA research tasks constitute the research and development deemed necessary for reaching the technical capability projected to exist for the system elements of the IDEA

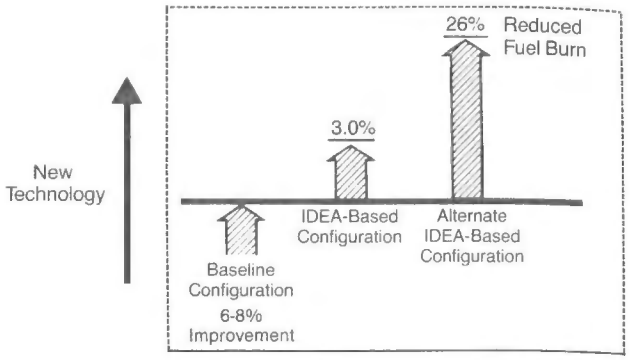

Figure 3. Fuel Burn Comparison, IDEA vs Baseline

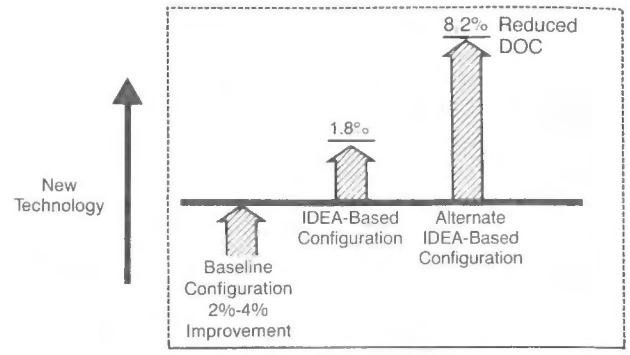

Figure 4. DOC Comparison, IDEA vs Baseline

configuration. The type of research, of course, depends on the current stage of development of each item. Some elements need a major system development sequence, from conceptual status through analysis, design, test, and demonstration, while others need only performance verification, hardware development, flight demonstration or in-service experience.

Other research areas were identified—areas of related developments not included in the IDEA configuration, but of sufficient interest to be considered for inclusion in broader research programs. Some of the categories of related research areas are:

- Features outside the basic scope of the study
- Alternative approaches which are potentially attractive
- Long-term developments
- New research for which feasibility has not yet been demonstrated

The most important aspects for each system included in the recommended NASA research activity are:

Flight Control and Avionics

- Architecture selection and development
- Development of high-reliability, remotely located avionics actuation
- Development of reliable actuator controllers and surface actuator computers

Electric Power System

- Development of flight critical electric power sources and system architecture

Data Distribution

- Design and development of distributed digital data bus

ECS

- Development of single stage compressors and motor controllers

Ice Protection

- Development of ice thickness detection equipment
- Development of design parameters for electro-impulse systems and components

Assessment Criteria

The availability of digital/electric systems for a 1990 airplane program is dependent on the successful completion of necessary research and development. Traditionally, the level of support for particular areas of research depends on the shifting military or commercial priorities of the market. As often stated in the aerospace news media, the market is currently impacted by a number of major economic factors, such as:

- Increased cost of fuel
- World and national economy
- Deregulation in the airlines
- Limitations of military budget
- Increased labor costs
- Availability of critical skills

During the past decade, emphasis has been focused primarily on technologies that could bring about a significant, measurable improvement in the fuel segment of the DOC. This came about as a direct response to the fuel crisis. Since fuel cost is a major component of the DOC, various methods of reducing fuel consumption became increasingly important in establishing priorities for research and development. Most of the emphasis was placed on the significant potential gains available through improvements in propulsion and aerodynamic technology. As a result, in the design of a new airplane the application of these technologies has, historically, led system design rather than having been integrated with it.

In this same time period, the extent of systems research activities was determined primarily by the increasing requirement for new functions and the need to provide solutions for specific problems. System capability was increased, but the lack of an integrated approach resulted in an unprecedented growth in complexity and cost. The recent IDEA study program represents a major effort to organize systems development on an overall airplane basis. Its goal was the definition of a developmental approach that provides for increased capability to meet the new system requirements, but does so with system architectures that are less complex and less costly. For the assessment, then, the effectiveness of systems research can be considered primarily in terms of potential cost benefits. This is true even though the results of systems research may provide only nominal improvements in performance or fuel burn.

Since the 1960s, for instance, the combined effect of propulsion and aerodynamic research has been much more obviously beneficial for the DOC than has systems research. To equate the progress of systems technology with that of other technologies, a more thorough assessment of digital/electric concepts is required. It must include the total economic impact of the system advances, not only in terms of performance and DOC, but also in cost of ownership or life cycle cost. This is especially significant because, for a new airplane, the propulsion and system costs together make up about 80% of the total recurring and nonrecurring costs. Of greater significance is the fact that the costs for propulsion and systems are now about equal. More and more functions are being required of airplane operating systems, and as the trend of functional requirements is increasingly flight critical or flight essential, there is also a need for increased reliability. The main challenge for systems technology development is to meet the increasing design requirements without increasing either the first cost to manufacturers or the operating and maintenance cost to users.

Conclusion

The IDEA study program defined and evaluated an IDEA configuration, and identified the research and development required for potential application to transport aircraft in the early 1990s. This study, together with the depth of other related work, produced results which indicate considerable potential in the proposed digital/electric concepts. The study results point out the necessity for the immediate organization of a comprehensive research and development program, if the goal of an early 1990 airplane program go-ahead is to be met. The study also suggests certain areas of systems research that should be examined to gain maximum benefit from parallel development, apart from the original goals of the program.

As the design of the digital/electric components, as well as their configuration, will be determined during the period of research and development, it was not reasonable to determine precise cost comparisons at this time. For a current assessment of the digital/electric airplane concept, the only available practical measure of success is neither a specific number nor an overall value. It is a direction. The key question is, "Will the suggested systems research and development plans lead us toward meeting the increasing requirements and demands without increasing cost?" or even more, "Will the plans lead toward meeting the challenge of a decrease in systems cost?" These questions can be answered by giving a responsible estimation of the anticipated effect of overall system change on each of the affected areas of DOC.

To begin with, we can examine the expected improvement in fuel burn for the 1990 digital/electric airplane. One of the most significant improvements is attributable to the addition of active controls. However, the full potential of relaxed static stability, with its 6% to 8% fuel burn reduction, is unlikely to be reached without the incorporation of an advanced, digital/electric flight-critical control system. In proceeding from the IDEA configuration to the alternate IDEA configuration, the addition of turboprop propulsion gives a significant potential improvement. Here too, the full potential can be enhanced with the application of advanced digital/electric concepts. Although the data is in the preliminary stage, industry feels that current bleed requirements would seriously impact the potential benefits of the propfan engine. Here especially, the beneficial advantage of no-bleed digital electric systems development must be exercised.

As we have stated, the fuel segment of the DOC is often exemplified in order to show fuel burn improvement effects. Figure 5 is

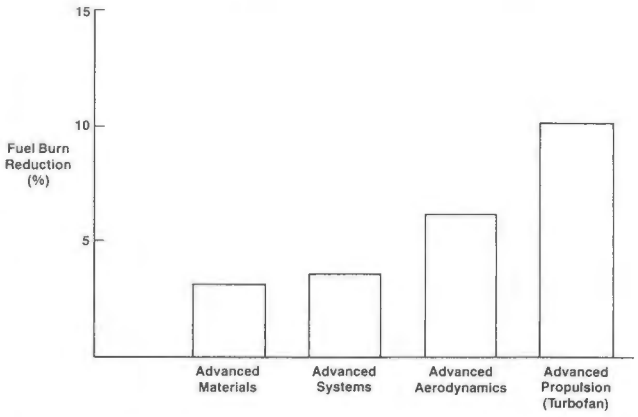

Figure 5. New Technology Potential for 1990s

a typical contemporary example of an illustration that emphasizes the fuel burn benefits of potential improvements in propulsion. Digital/electric systems improvements appear less impressive against potential propulsion gains. However, the total effect of digital/electric systems application can be seen more clearly in the overall DOC picture.

Table 2 is a listing of the major segments of the DOC breakdown and compares the IDEA-based airplane to the Baseline. The largest single impact is the result of systems weight reduction. For the IDEA configuration this amounted to 3180 lb. As a result of recycling the airplane size to a reduced OEW, a 1.8% decrease is noted in the DOC of the IDEA configuration.

Table 2. DOC Comparison — IDEA vs Baseline

1983 U.S. Domestic Rules 500-nmi Range	Baseline	IDEA
Takeoff Gross Weight (lb)	268,040	260,980
Number of Passenger Seats	197	197
Block Fuel (lb)/(lb/Seat)	9,385/47.6	9,120/46.3
Depreciation, Airframe and Engine	3.19	3.19
Insurance	0.10	0.10
Flight Crew	1.45	1.45
Fuel (at $1.50/gal)	4.42	4.28
Airframe, material and Burdened Labor	0.87	0.85
Engine material and Burdened Labor	0.68	0.65
DOC ($M per Year)	10.70	10.50
Δ DOC (%)	Base	-1.80
(Cents/ASM)	4.459	4.374

Besides fuel costs, the other areas of the DOC affected by the digital/electric systems concepts include the costs of depreciation and insurance and the cost of maintenance. Exact determination of costs for future 1990 IDEA components was not possible. Therefore, initial systems-cost figures for the IDEA study were maintained equivalent to those of the Baseline airplane. Systems-related DOC costs represent about 24% of the initial cost of the total airplane and about 70% of the total maintenance cost (Table 3). If these systems-related portions of the DOC could be reduced by 10% through application of the IDEA systems concepts, the total DOC would be decreased by an estimated $1.39M per year, or 1.32% of the DOC. For the purpose of this general assessment, then, a 10% decrease in the depreciation, insurance, and maintenance items segment of the DOC was considered reasonable and attainable; this will require innovative development.

Table 3. Effect of Selected System Improvements on DOC

1983 U.S. Domestic Rules 500-nmi Range	IDEA Airplane		Systems Portion	IDEA Systems
Depreciation, Airframe and Engine	3.19	▷	24%	0.79
Insurance	0.10			
Flight Crew	1.45		*	*
Fuel (at $1.50/gal)	4.28			
Airframe, material and Burdened Labor	0.85	▷	70%	0.60
Engine material and Burdened Labor	0.65			
DOC ($M per Year)	10.50	▷	13.2%**	1.39

* Systems Weight Effects Not Shown
** 10% Reduction in Systems Portion Reduces DOC by 1.32%

Combining the various reductions in DOC, due to the application of digital/electric systems, gives a total reduction of more than 3%. Interestingly, this decrease in DOC is equivalent to a reduction in the fuel segment (such as an engine SFC improvement) of the DOC of approximately 8%.

Based on this examination of the 1990 digital/electric airplane concept, it is concluded that the IDEA configuration is a positive step toward the many operational benefits of a fully integrated system. More obviously, the application of these new concepts will result in reducing many of the system's DOC component values, and reverse the trend of increasingly expensive airplane systems. Digital/electric systems offer a positive approach to cost reduction as well as increased functional capability. Upon successful completion of the appropriate research and development, many of the potential benefits indicated can be realized in time for application to commercial transports of the 1990s.

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A MINIMUM INTERRUPTION AC ELECTRIC POWER GENERATING SYSTEM FOR AVIONICS

84-2742

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Abstract

Momentary electrical power interruptions caused by bus transfers during startup occur on aircraft load buses supplying 115 VAC 400 Hz power. These brief interruptions can upset avionics subsystems requiring manual reset. This paper discusses the causes and effects of these phenomena in more detail, especially interruptions which occur during normal operation such as when load buses are transferred between sources. Techniques to eliminate these normal interruptions exist and can easily be applied in modern controls for electrical generating systems.

Introduction

As aircraft capabilities continue to expand and the complexity of manned aircraft systems increases, the electrical system is called upon to provide power with minimum interruptions to improve the overall utilization equipment performance. Aircraft electrical power characteristics affect the design and power dissipation of essentially all power utilization equipment. Each deviation from desired power quality may cause a design or performance penalty to the power using equipment. In addition, electronic equipment includes built-in power conditioning circuitry or power supplies to provide the internal power requirements. The weight, cost, and power dissipation of this internal circuitry is adversely affected by the possibility of input power interruptions.

The advent of microprocessors and the reliance on more and more software stored in memory to control essential functions have put some new demands on aircraft electrical power systems. Use of digital processors supported by volatile memories require that the electrical power system be free of transient power interruptions.

Techniques have been developed which eliminate power interruptions and the magnitude of transients which can occur during power source and bus-to-bus transfers.

Electrical Power Generation System Requirements

The electrical power generation system (EPGS) power interruption requirements are generally a function of the utilization equipment requirements. These are controlled by such documents as MIL-STD-704 and RTCA DO-160 which define EPGS requirements at the utilization equipment terminals.[1];[2] Detail requirements which tailor these documents to the needs of a particular aircraft, are provided in a control document written by the airframe manufacturer.

Typically on conventional aircraft, bus-to-bus transfers are allowed interruptions from 50 milliseconds (MIL-STD-704) to 200 milliseconds (RTCA DO-160). The interruption is mainly composed of logic delays and contactor operation time. Transfers from the auxiliary power unit (APU) or external power to the main generator power are normally performed by manually initiating closure of the main line contactor for a main generator channel. This will automatically open the APU or external power contactor. The main line contactor will then automatically close when interlock circuits sense that the APU or external power contactor has opened. Figure 1 shows a typical external power to main generator power transfer with a load of 20 KVA at a .75 lagging power factor. As illustrated, there is a power interruption of approximately 50 milliseconds. The voltage reaches steady-state an additional 30 milliseconds after the transfer is completed.

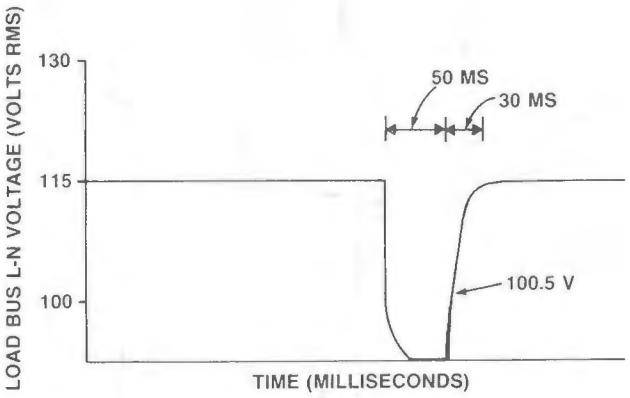

Figure 1. Load Bus Voltage for Typical External Power to Main Bus Power Transfer

Modern technology aircraft have attempted to utilize various techniques to reduce the magnitudes of power source transfer transients and interruptions. Low level voltage transients caused by the on/off operation of utilization equipment during a typical flight can never be completely eliminated. These transients should be considered as a part of normal electrical system power quality and be acceptable by aircraft avionics.

One technique is to use dual (redundant) input power sources for sensitive equipment. The two power sources must be internally isolated and buffered within the "black box" to prevent an internal fault from seriously disturbing either source of input power. This method adds complexity, weight, and cost to the equipment.

Modern technology aircraft are also making changes in the typical electrical power generating system (EPGS) bus configurations to reduce overall system complexity and minimize power interruptions. In conventional aircraft with multiple EPGS channels, standard operation has been with the channels connected in some form of a parallel configuration to reduce the impact of high magnitude load switching and provide greater fault clearing capability. Since these problems are of less concern today, the trend is to utilize a split bus or split-parallel bus, arrangement. Examples of these bus configurations are shown in Figures 2 and 3.

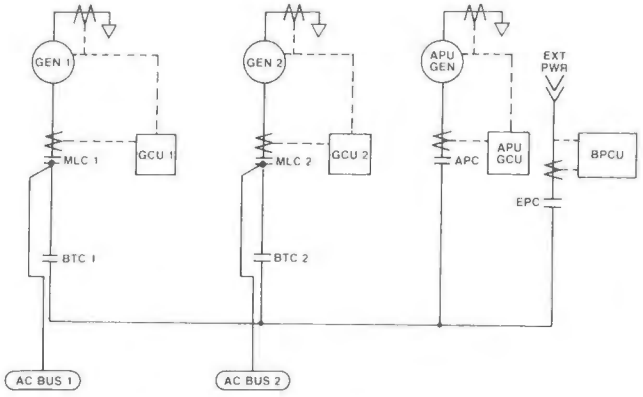

Figure 2 Typical Modern Technology Aircraft Two-Channel Bus Configuration

The split bus arrangement places the added burden on the EPGS to limit bus transfer times to a minimum and reduce the magnitude and duration of voltage transients which occur when the additional load is acquired by the operable bus(es).

Problem Solution

Philosophy and Requirements

The philosophy of no-break power transfer is to momentarily parallel the source, assuming that the load and the source are being replaced. After a brief period of parallel operation, the old source is disconnected and the new source takes over the full load. With this technique, there is no period in which the load is disconnected from all power. With proper design and operation of the control circuitry, transients will be limited to those levels associated with normal load-on or load-off events.

To execute a transfer, the power source output waveforms must be closely aligned. Differences in phase and voltage will result in reduced point of regulation voltages as well as potentially high currents flowing between sources. The combination of these effects may result in unacceptable transients and power interruptions.

The analysis of such transients is a function of the system internal reactance and load impedance, as well as the dynamic performance of voltage regulators and speed

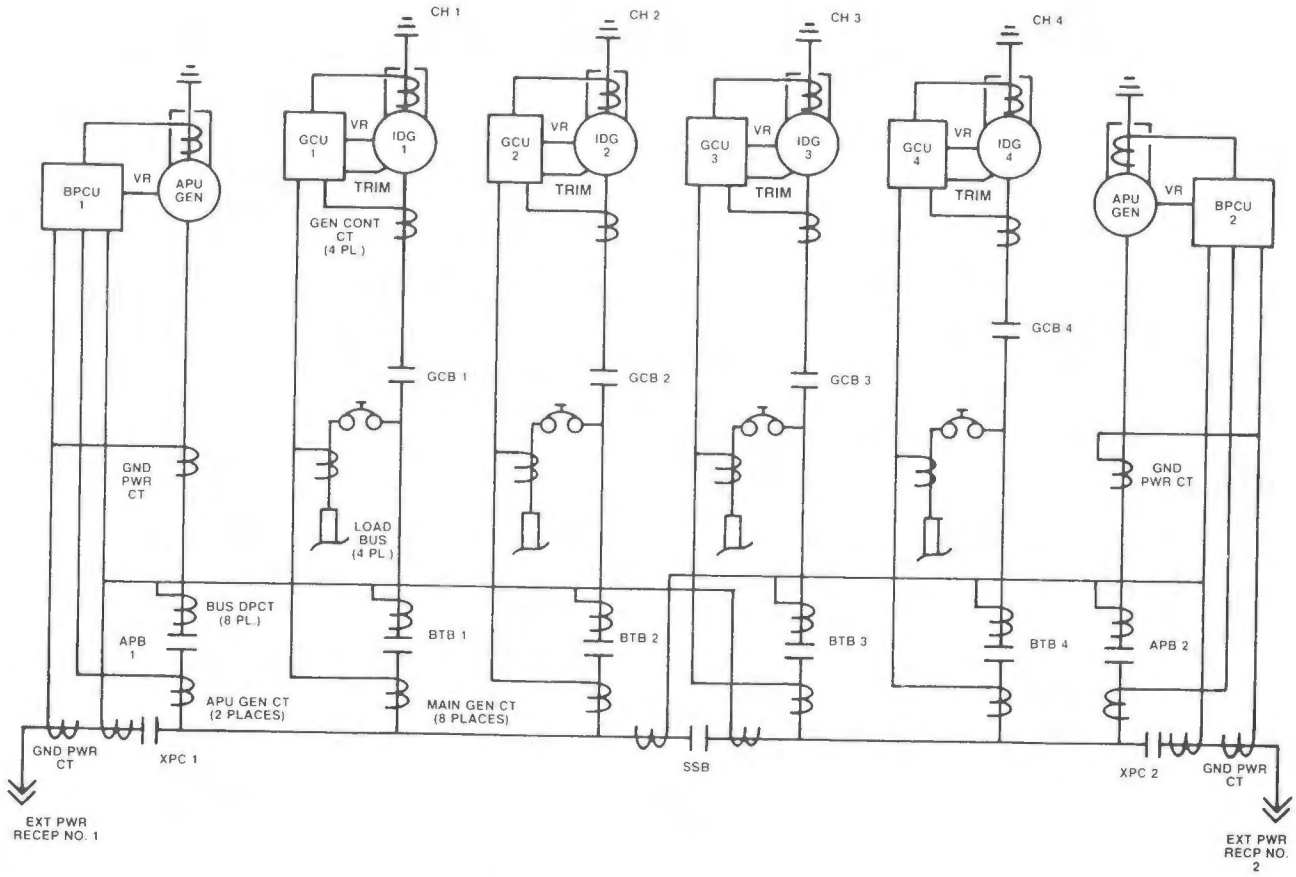

Figure 3. Typical Modern Technology Aircraft Multi-Channel Bus Configuration

control circuits. This analysis is beyond the scope of this paper, but if the initial conditions of voltage, phase, and frequency differences are kept low, then the transients will be kept within acceptable levels. The magnitudes of transients in physical systems are typically a function of the magnitudes of the perturbations which have caused the transient.

It must be assumed that external power sources will not be capable of the control required to match phase and frequency, so all aircraft engine-driven sources, integrated drive generators (IDGs) and auxiliary power unit (APU) driven sources must be capable of synchronizing with all alternate sources, when they are taking over a load or when they are giving it up. In the case of IDGs, the required speed control abilities are readily available. APUs can also have the desired speed control, but it is not customary for them to do so.

When phase, frequency, and voltage equalization have occurred, the contactor connecting the new source to the load bus will be automatically closed. At this point a transient may occur, but it will be no more than a normal load-on or load-off transient.

Figure 4 below is a flow chart of this power sequence.

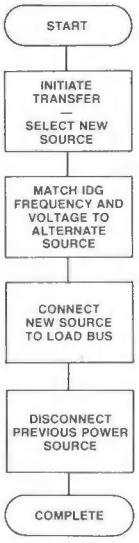

Figure 4. No-Break Power Transfer Sequence

To implement this control philosophy, the individual system elements must have several capabilities. Integrated drive generator governors must have electronic trim control or electronic servovalve governing. Control circuitry must be present in the generator control and bus control units to monitor input parameters and coordinate the transfer sequence. Finally, voltage sensors are provided for determination of bus voltage, frequency, and phase relationships between sources.

Early system designs to provide no-break power transfer between power sources were unsophisticated. They provided no direct control of the power sources and simply monitored the beat frequency between like phases of the two power sources. When the phase difference was less than 90^0 and closing, the transfer was initiated. This resulted in transients greater than those with normal load switching.

Other designs utilized direct control of the main generator frequency. The main generator frequency was adjusted to within 3Hz of the other power source. When the phase angle difference was less than 30^0, the two sources were momentarily paralleled and the transfer accomplished.

Advanced System Implementation

As noted, no-break power transfer has been implemented successfully using techniques which allow relatively wide tolerances in the power characteristics of the various sources.

An advanced system to minimize transients and provide a full range of transferring capabilities can be implemented with a minimum impact on system complexity. Features of this advanced system would include complete phase-locked synchronization of sources, voltage control during transfer to match aircraft source voltages to external voltages, and APU speed control to allow transfers between external and APU power.

The power control methods for this approach are based on well-known technologies and are a subset of those used in parallel systems. In addition to no-break power transfer, these methods also provide fine frequency control and voltage regulation. The synchronization feature eliminates the possibility of beat frequencies induced within the aircraft power distribution system.

In a typical system of either split or parallel configuration, power may be supplied to various loads from various sources through a tie bus. To allow no-break power transfer, each generator control unit (GCU) must sense its own output voltage and frequency, and have reference to the voltage and frequency of the tie bus and the external source outputs. Each GCU must be able to vary its own generator's output characteristics to match the external source.

Many implementation schemes are possible. The following system is provided as an example. Figure 5 shows a simplified aircraft system suitable for explanation. The sequencing of bus transfers is controlled by the bus control unit (BCU)in conjunction with the GCUs. The BCU has logic to process the request for a transfer, decode the source selection signals, select the sequence which is appropriate for the commands and system state, and operate some of the system contactors. The GCUs control the matching of source voltages and frequencies, eliminate phase differences, and operate the remaining contactors. Command and status information must flow freely between the GCUs and the BCU.

In a system such as the one in Figure 5, different event sequences must occur for different types of bus transfers.

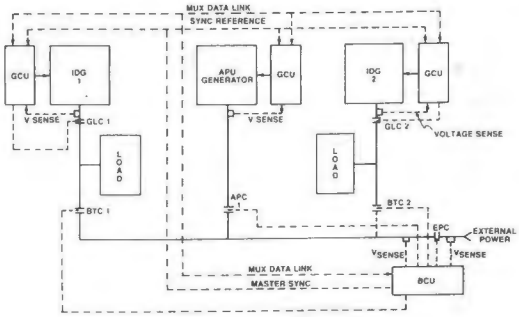

Figure 5. Simplified Power Distribution System With No-Break Power Transfer

Table I lists these sequences for the three most common types of transfers. These include transfers from external power to auxiliary or IDG power, from IDG or auxiliary power to external power, and transfers of loads between IDGs or APU. Variations within these sequences may also occur, depending on how the tie bus is used (or not used) to supply power to the loads. Sequence variations or abortions may also be required in the event of abnormal operation of any of the sources.

TABLE I NO-BREAK TRANSFER SEQUENCES

External or APU power to IDG power

1. BCU receives transfer request and identification of new source.
2. BCU issues bus transfer command to GCU of system which will acquire load. BCU sets sync reference and external voltage reference to match tie bus power.
3. GCU matches IDG frequency, phase, and voltage to tie bus power.
4. GCU closes generator line contactor, senses closure, and indicates closure to BCU.
5. BCU opens auxiliary power contactor (APC) or external power contactor (EPC) as appropriate.
6. Bus transfer command is cleared.

IDG power to external or APU power

1. BCU receives transfer request and identification of new source.
2. BCU sets system sync reference and external voltage reference to match APU or external power and issues bus transfer command to GCU of system which will acquire load.
3. GCU matches IDG frequency, phase, and voltage to reference from BCU and indicates match to BCU.
4. BCU closes EPC or APC and indicates closure to GCU.
5. GCU opens GLC.
6. Bus transfer command is cleared.

IDG 1 power to IDG 2 power

1. BCU receives transfer request and identification of new source.
2. BCU issues bus transfer command to GCU of system which will acquire load. The bus tie contactor of the original source is closed.
3. IDG phase and frequencies should already be matched.
4. GCU closes GLC or bus tie contactor (BTC), connecting itself to tie bus. Closure is indicated to BCU.
5. BCU commands old source to open its GLC or opens BTC as appropriate.
6. Bus transfer command is cleared.

These sequences are complex especially if exception cases are considered, but they can easily be implemented by modern microprocessor based control units with negligible additional parts.

Figure 6 is a block diagram of GCU functions related to no-break power transfer. The sync reference is a pulse train received from the BCU. The sync reference serves as a reference for the speed control loop. During a bus transfer it will be modulated by the BCU to adjust generator output frequency to match that of the alternate power source. An internal frequency reference is provided as a backup.

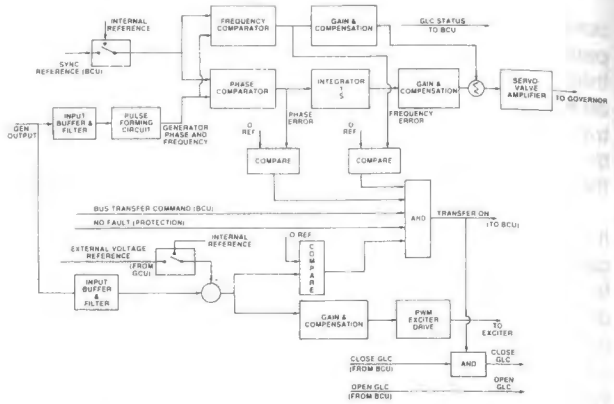

Figure 6. No-Break Power Transfer — Generator Control Logic

The frequency reference pulse train and the pulse train representing the generator output frequency are fed to both phase and frequency comparators. The frequency comparator and the subsequent gain and compensation network close the frequency control loop. The frequency error output of the comparator passes through the compensation block and is summed with the phase error to provide an input to the governor servovalve amplifier.

The frequency loop tends to match the generator output frequency to the reference frequency, but it is also necessary to match phase. The output of the phase comparator is integrated and the result is a constant value which, when compensated, is the second input to the governor servovalve amplifier. In the steady state, the frequency error is zero, the phase error is close to zero, and the phase loop controls the servovalve.

The phase and frequency error signals are tested, and if their magnitudes are low enough, status signals to that effect are asserted.

An external voltage reference may also be provided by the BCU. It allows the BCU to reduce or increase system voltages to match poor quality external power. It can be a digital signal, and it is used as the reference for the voltage control loop. A backup internal reference is also provided.

The voltage reference is compared to a signal representing the POR voltage. The voltage error is fed to a gain and compensation network and then drives the generator exciter field to control generator output voltage.

If voltage, phase, and frequency errors are near zero, and if the bus transfer command has been received from the BCU, and if the GCU protection circuitry is not declaring a fault condition, the transfer OK signal to the BCU circuit is enabled. This signal enables the closing of contactors to begin the transfer.

The GCU receives generator line contactor (GLC) control signals from the BCU over the data link and executes them. The GLC status is also transmitted to the BCU.

All GCU functions, except input buffering and filtering and output amplifiers, can be implemented in software within the unit's microprocessor. With this type of implementation, control hardware complexity is negligibly affected by the no-break power transfer option.

In the example system, the BCU has the intelligence to control the sequencing of the bus transfers. Figure 7 shows the logic associated with no-break power transfer which resides in the BCU. Two signals are passed from elsewhere in the BCU to cause a transfer. These signals are transfer request and source select. It is assumed that they are generated upon command of the aircraft crew or by some overall system control logic within the BCU.

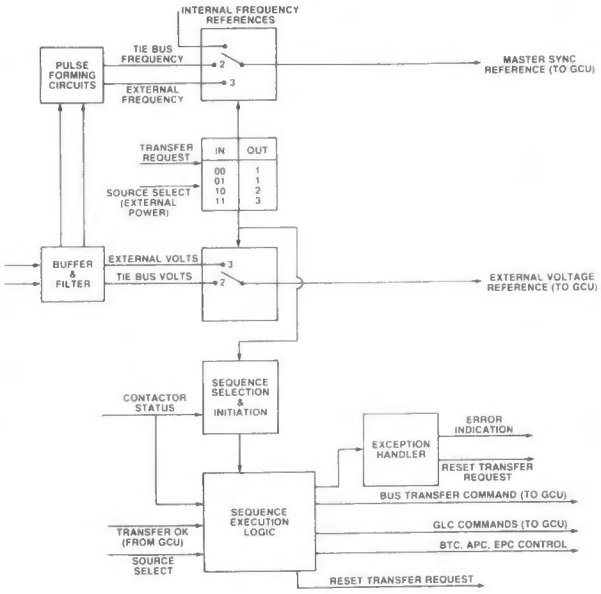

Figure 7. No-Break Power Transfer — Bus Control

These signals initiate the transfer and set the sync reference and external voltage reference source switches to the appropriate inputs. Under normal operation, sync reference is set internally in the BCU to a value as determined by the system specification. External voltage reference is only determined when needed for a bus transfer; otherwise GCU internal references are used.

During most transfers the tie bus will initially be powered by the source giving up control of the loads. In this case the tie bus voltage and frequency are used as reference inputs. In one case, when a speed controlled aircraft source is passing control to external power, the aircraft source(s) must adapt to the external bus power. In this case the external bus voltage and frequencies are used as reference inputs.

The same information used to set the references is passed to the sequence selection and initiation logic along with knowledge of contactor status. This logic resets all internal sequence status. It also selects the appropriate transfer sequence and sets internal variables for sequencing logic to access the proper status tables and command words for the sources active in the transfer. It then starts the sequence.

The sequencing logic executes the transfer in a manner similar to that described in Table I. It responds to contactor status information and transfer OK signals from the GCUs. It issues contactor control signals and eventually, at the completion of the transfer, resets the transfer request signal to return references to their normal inputs and annunciate the completion to other logic within the BCU.

In the event of abnormal operation or behavior of a system element during the transfer, exception handling logic is provided to terminate the sequence. It sets an error indicator to flag the failure of the transfer and resets the transfer request signal as noted above.

All logic blocks except input buffering and the frequency reference switch can most easily be implemented within the software of a microprocessor.

Test Results

A demonstration of no-break power transfer was conducted using a somewhat different control circuit than described above. The philosophy of phase locking was used.

Initially, the load bus was supplied with external power at 390 Hz and 118 VAC. The IDG output frequency was adjusted by its GCU to external power. When IDG power was synchronized with external power, the GCU auto parallel circuit closed the IDG contactor, paralleling the two sources. The external power source was then disconnected in less than 50 milliseconds. The IDG output was then readjusted to its specified output level. The transfer occurred with no interruption in load current.

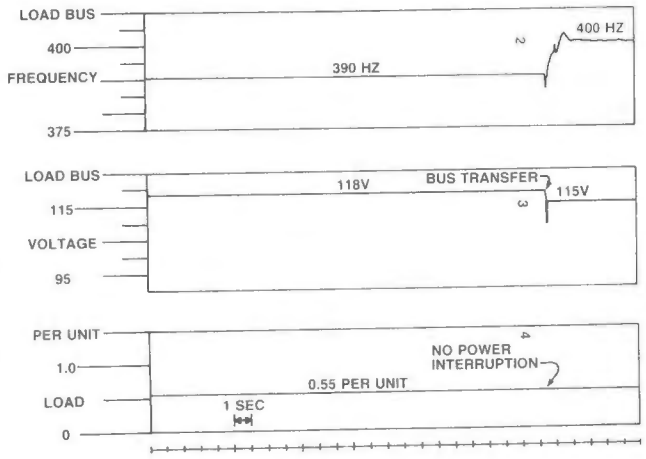

Figure 8. No-Break Power Transfer

Conclusion

In modern aircraft with advanced avionics, power interruptions associated with the transfer of loads from one source to another can cause the avionics systems to be upset, requiring manual reset. This can adversely affect aircraft operations.

The techniques to minimize or eliminate these interruptions exist and have been demonstrated in production equipment. Advanced implementations with minimum transients and maximum flexibility can be used with techniques similar to those required for parallel system operation. In systems using microprocessor full authority digital control of speed and voltage, implementations can be realized with negligible effects on system part counts and hardware complexity.

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SESSION 24 STANDARDIZED MODULAR AVIONICS

Chairmen:

Ken Ricker
ASD/AXP

John A. Wyatt
Department of Defense
OUSDRE

This session addresses the challenges of modular avionics and examines aspects of standards, packaging, partitioning and design.

84-2745

COMMON MODULAR AVIONICS: PARTITIONING AND DESIGN PHILOSOPHY

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Abstract

Next-generation avionic hardware has recently been described by the term common modules. Numerous on-going and pending Air Force avionic programs are actively studying the definition of standard modular hardware. This paper will examine the design objectives and definition criteria for common modular hardware that will perform digital processing functions in multiple avionic subsystems. It is not the authors' intent to propose a specific group of module functions, but rather to describe the criteria that should be considered during the definition of standard modules.

Introduction

Military avionics appears to be on the verge of a change in the methods used to design, purchase, and support the hardware. This change involves the use of standard printed-circuit card sized modules to create subsystems which are currently represented by unique black boxes, or Line Replaceable Units (LRUs). The large amount of interest in common modules can be seen in the many Air Force programs examining the concept, including: Pave Pillar, Advanced Tactical Fighter, ICNIA, Common Signal Processor, and VHSIC 1750.

Module Applicability

The areas of avionics that can potentially use modules are bounded by establishing limits on the type of functions that common modular hardware would perform. In current avionic systems, for the most part, information flows between processing nodes in digital form and can be processed by common digital hardware. So the criteria for common module applicability will be that the function to be performed is digital, or the module is an interface to an analog portion of the aircraft environment. This does not preclude the packaging of analog functions or special digital circuits in a modular chassis, but generic common modules will be predominately digital processing functions.

Module Definition Process

The definition of criteria for partitioning avionic processing functions into modules will be derived in a three stage process, as illustrated in Figure 1 and described in the body of this paper.

First, the weapon system-level objectives of modular hardware usage are defined. Second, these objectives are analyzed to determine the overall modular design goals that will produce the desired weapon system-level objectives. And third, these overall modular design goals are analyzed to produce specific partitioning criteria for the definition of modular hardware. Therefore, if a module set is defined using the specific partitioning criteria the desired weapon system-level objectives should result.

Weapon System-Level Objectives

There are three primary weapon system-level features that common modular avionic hardware should produce. These are:

1. Increase Supportability. Modular hardware should increase avionic supportability by reducing the overall number of required spare part types, and by decreasing the role of ground-based test equipment in avionic maintenance.

2. Reduce Life Cycle Costs. Common modular hardware should reduce design, acquisition, and support costs by using common standardized hardware that can be procured from multiple sources and can function in multiple avionic subsystems.

3. Increase Upgradability. Modular avionics should increase the ability to upgrade operational hardware by allowing module by module growth of the limiting portion of a modular subsystem.

Overall Modular Design Goals

The weapon system-level objectives of modular hardware, described above, can now be broken down into overall design goals for

the modular hardware. These fall into four categories:

1. Reduce Test Equipment Requirements. The supportability of aircraft avionics can be increased by reducing the amount of equipment that must be deployed with a group of aircraft. This concept involves a reduction in the role of the Avionics Intermediate Shop (AIS) test equipment used to isolate hardware failures. In a modular support environment, a failed module could be removed on the flight line and returned directly to a depot repair facility. This would allow improved aircraft deployment, reduced vulnerability of deployed assets, and lower maintenance manpower requirements. While elimination of the AIS (i.e., two-level maintenance) appears very desirable, a more realistic goal is to reduce the size and number of the required AIS test stations.

2. Have A Large Number of Subsystem Applications. In order to increase supportability and reduce life cycle costs a common module should have multiple applications among the subsystems on an aircraft. This reduces the number and diversity of spare part types. It also produces larger production runs for a piece of hardware, thereby lowering procurement costs through economies of scale. In addition, there will exist a large quantity of developed hardware for use on a new subsystem, which will reduce the amount of new hardware that must be designed.

3. Design for Architectural Growth. To increase subsystem upgradability the inter-module communications structures should have large growth capabilities. This would allow a flexible upgrade potential for operational hardware by accommodating future communications requirements over the existing bus structure. Therefore additional new or existing module types could be added to a subsystem without impacting the rest of the modules in the subsystems.

4. Standardize for Technology Transparent Implementations. In order to reduce costs and increase upgradability modular hardware should be standardized independent of internal hardware implementation, a feature called technology transparency. This method for standardizing hardware involves defining the functional, interface, and physical features of a module, but not the internal hardware architecture or component technology. Technology transparency would allow multiple vendor sources for a particular type of module and more flexibility in procuring replacement hardware for older equipment.

Specific Partitioning Criteria

Having established the weapon system-level objectives and overall modular design goals, specific partitioning criteria can now be derived. This is done by analyzing the overall modular design goals described above to determine how modular hardware can directly implement these goals, which will then produce the desired weapon system-level objectives. The specific modular partitioning criteria are as follows:

1. Meet a Cost/Removal Rate Relationship. To achieve the overall modular design goal of reducing the test equipment requirements, the two criteria that drive the avionic maintenance methods need to be examined: cost and removal rate. The Avionics Intermediate Shop (AIS) is used to maintain current aircraft primarily because the removed hardware either costs too much or is removed too often. In order to establish a cost/removal rate relationship for avionic hardware, current F-16A/B Line Replace Units (LRUs) will be examined. A plot of the spares unit cost versus Mean Time Between Removal (MTBR) is shown in Figure 2.

The plot is divided into three areas of maintenance suitability. The first is above the $50/removal-free flight hour line, where all of the LRUs are maintained using organizational, intermediate, and depot levels of maintenance. The LRUs require these three levels of maintenance because the cost of the spares for the depot repair pipeline that would be needed if the AIS were not used, exceeds the life cycle costs for using the AIS eqipment. The second area is located between the $50/hour and the $2/hour line, and in this area it is feasible to maintain LRUs without an intermediate test and repair capability. In this area the decision on maintenance level is based on criteria such as an LRU's flight criticality. The third region is below the $2/hour line where virtually all of the LRUs are maintained without an intermediate shop. The few AIS-maintained LRUs in this region are flight or survival critical.

From this data it can be concluded that if modular avionics is to be maintained without extensive intermediate test equipment then the cost/MTBR relationship must fall below $50/hour and if possible below $2/hour. Additional analysis has shown that it is desirable to have a minimum 2000 hour MTBR to reduce the spares requirements to a desirable level.

2. Provide Increased Fault Isolation Capabilities. The second key factor required to achieve the reduced test equipment goal is to be able to identify a failed module in the aircraft. This requires extensive built-in test capabilities that occur at multiple levels, i.e. chip, module, subsystem, and system. This type of hierarchical testing approach is necessary to allocate and effectively use the amount of hardware and processing time required to identify a failed module with near 100% probability.

An example of the type of techniques and

capabilities that will be needed in a modular maintenance environment is described below. At the chip level, testing involves techniques such as on-chip monitors and signature analyzers to identify hard failures. Fault and status information is then communicated to a device resident on each module. This device is used to activate and monitor chip-level testing, as well as providing a uniform module interface to the higher maintenance levels. The subsystem level has a test controller which has the capability to interpret failures and to store specific failure information in a bad module for use at the depot repair facility. The highest level is the system maintenance processor which would be used for centralized storage of failure data and to provide an interface to flight-line maintenance personnel.

The above description is intended to be a representative approach to fault detection and isolation in a modular environment. It is not intended to be inclusive, but more to indicate that built-in test should be a significant consideration from the beginning of any modular design effort.

3. Define an Open Architecture. In order to achieve the overall modular design goals of a large number of subsystem applications and architectural growth potential, module partitioning must produce an open architecture. The concept of an open architecture means that there are no inherent limiting factors in the module definitions or in the communications structure which preclude the addition of new functions to an existing module set.

Without tight coupling between modules, it is relatively easy to insert new functions into the module set, by merely defining the communications required between the new module and the existing set. This provides some degree of protection against built-in obsolescence by removing most of the factors which restrict growth, such as peculiar inter-module input/output or control signals. For example, adding a new high speed serial terminal to a module family will require a new high-speed interface module, but the parallel interface between the new module and the existing modules should not be impacted. Proper system partitioning will also prevent the inter-module bus from becoming a bottleneck when adding new functions.

An open architecture really entails a system design methodology where a core group of processing functions are used in specific subsystem implementations as much as possible. Unique elements such as I/O and special signal processors are defined and implemented as needed and subsequently added to the list of modules.

4. Define Modules to be Autonomous Functions. In order to meet the overall modular design goals of a large number of applications, architectural growth, and technology transparency the modules should be partitioned into autonomous functions. An autonomous, or stand-alone function means that the module has a clearly defined interface and the capability to operate without close coupling to any other particular module.

Breaking a system into autonomous functions enhances several facets of its design and operation. First, development is less risky because parallel design efforts can be implemented. Traditional approaches to avionic hardware design require close coordination between all design groups to ensure interface compatibility. Partitioning a system into stand-alone functions creates narrow, well defined areas of interaction between those functions, which has benefits to both hardware and software development. Secondly, partitioning into stand-alone functions creates the maximum opportunity for commonality by reducing the coupling between different parts of the hardware. This provides subsystem designers with a set of existing building blocks in much the same manner as commercial integrated circuits provide standard functions to the circuit designer.

Partitioning for autonomous functions removes many of the technology dependent interfaces between modules, therby promoting card level interoperability and module set growth capabilities.

5. Utilize Information Hiding Concepts. To produce the overall modular design goals of architectural growth and technology transparent implementations requires the use of information hiding concepts. Information hiding is the generic term used to describe the interface between software components and the hardware they execute on. The requirement to make the software implementation independent of a particular hardware configuration is apparent in many standardization programs, such as the MIL-STD-1750 and MIL-STD-1862 computer Instruction Set Architectures.

Information hiding is implemented by extracting from system software all the information which is specific to a given system or hardware implementation. Then the use of this information is relegated to the lowest level possible, so that these details become hidden from the system programmer. An example of this technique is the ISO/Open Systems Interconnect model for telecommunications network control. Each layer in this model is insulated from its neighbors, providing a transparent view to the user of those layers which are not involved in the actual communications process. In other words, if a communications function is not concerned with the formulation or interpretation of the concepts of a message, then the information used to implement that function is not visible to the creator or end user of the message contents.

Information hiding can be applied to other functions in a similar manner. When this

technique is extended to encompass the rest of a computing systems resources, such as I/O and memories, it becomes a powerful tool for promoting software commonality and preventing duplication of effort in development.

Additional Partitioning Information

It is worthwhile to note at this point the difference between the concepts of an open architecture, partitioning for stand-alone functions, and information hiding.

Open architecture is a system-level design methodology which places constraints on both hardware and software designs from the top down. Partitioning for autonomous functions is a module hardware design constraint used to preclude the creation of unique technology dependent interfaces. Information hiding is a hardware/software interface design methodology which attempts to increase the degree of hardware independence exhibited by system software. Though related, the three concepts apply at different levels within the system design process.

Conclusion

This paper documented the weapon system-level objectives, overall modular design goals, and specific partitioning criteria for modular avionics. This process was described independent from a particular level of component integration or system processing requirements. Consequently the described objectives, goals, and criteria should be independent from a particular time-frame of implementation, and therefore apply to both current and future modular design efforts. It is hoped that the ideas presented herein will provide criteria to quantify the benefits and design objectives of a modular avionic environment.

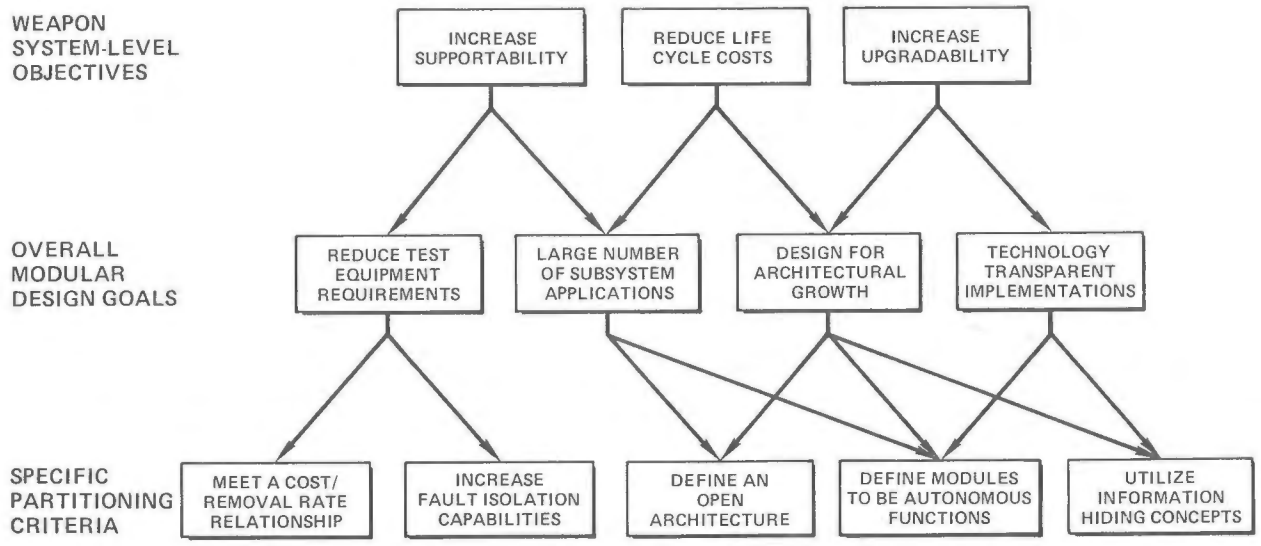

Figure 1. Modular Definition Process

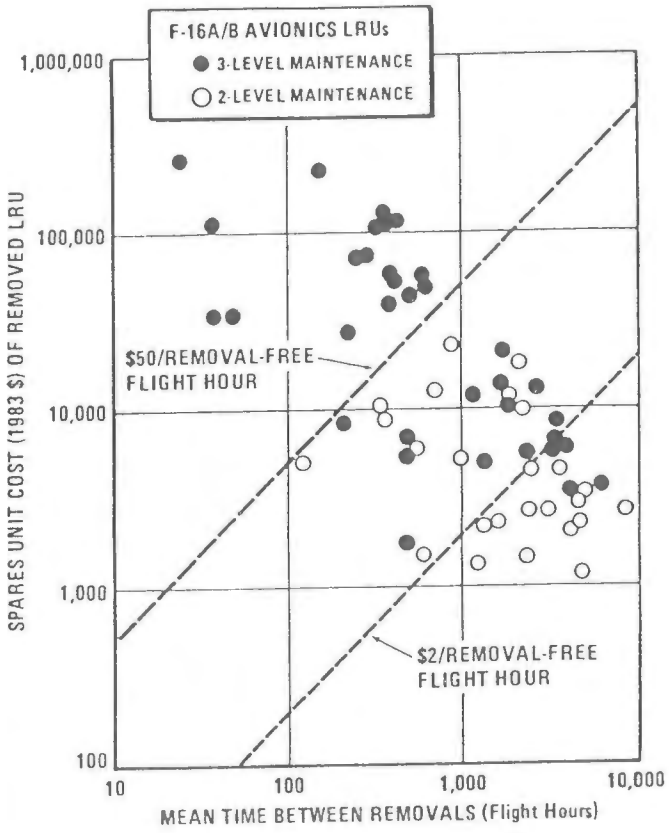

Figure 2. F-16A/B LRU Cost vs MTBR

MODULAR STANDARDS FOR EMERGING AVIONICS TECHNOLOGIES

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Abstract

The word "standardization" evokes strong reactions, both positive and negative, within the avionics community. To some designers, the existence of standards makes their job easier. Standards provide logical building blocks for the design and make interfaces with other systems of the aircraft easier to accomplish. Other designers feel the standards encumber their design freedom and thus inhibit technological progress. The development of standards within a highly technological community is, therefore, a very controversial endeavor.

This paper reviews approaches to and proposes modular standards for the integration of new avionics technologies into production aircraft and major retrofit programs. Physical and functional partitioning concepts used in the military and commercial avionics communities are compared, including LRU and SRU packaging concepts, multifunctional equipments, and integrated racks. Compatibility with emerging technologies, such as VHSIC and fiber optics, is also addressed. Ongoing programs sponsored by the Government and industry are described. Specific topics addressed include PAVE PILLAR and the Navy Standard Electronic Module (SEM) program.

Introduction

The word "standard" has often evoked either words of praise or a fusillade of criticism. On the one hand, standards are purported to make the job of designing and integrating systems easier by creating logical building blocks and defining standard interfaces. On the other hand, however, designers argue that standards can very quickly constrain freedom of design, thus inhibiting technological progress. Standardizing can also cause inefficiencies. It often inhibits the optimal way to perform a function, design a system, or develop an interface. An example of inefficiencies resulting from standardizing is the physical packaging of avionics functions. By imposing a packaging standard, simple functions are often allocated too much space while complex functions must often be divided between packages. From a logistician's paradigm, standardization has many advantages; reduced support costs, increased market competition (lower acquisition costs), and less spare parts stockage problems. On the other hand, operations personnel often voice concern about having to adapt missions to equipment and "living without" unique capabilities available in the form of specially designed equipment. In addition to questions of content and relevance of standardization, the timeliness is often cited as being inappropriate: standards are either developed too early or subsequent to hardware development. In summary, standardization appears to suffer from three problems: acceptance by the technological community of the concept of a standard, the correct content definition (caused by lack of user and designer input), and timeliness.

The Air Force PAVE PILLAR program, implemented to develop new concepts in avionics, is using a new approach to standardization. It is addressing the three problems of acceptance, content, and timeliness in developing the standards for the next generation of avionics. The goal is to use a more structured and open approach in developing standards for modular avionics. The central theme being pursued is a military version of the method followed by commercial airlines in developing avionics standards (referred to as "ARINC Characteristics"). That is, to use early and open participation from industry in developing the standard. In addition, to address the timeliness issue, the standard will be developed concurrently with hardware. As more information on the modular avionics systems become available, the standard will become more specific with the content and level of detail determined by the hardware designers.

Background

Before we can begin to discuss the modular avionics standard and what we have accomplished thus far, a definition of the modular avionics concept is appropriate. What is it? Probably the best way to describe what we mean is to examine the characteristics of an avionics module, the basic building block of modular systems. These characteristics can best be categorized into technical, employment, and acquisition features.

- Technical. The avionics modules proposed by the avionics manufacturers are, for the most part, complex and digital. They fall into the categories of processors, memories, interface units, and controllers. The functions performed by the modules are signal and data processing, storage, and transfer. These functions are common to many subsystems.

- Employment. Avionics modules will be replaceable on the flightline. They will thus represent the lowest level of fault isolation and detection at the flightline level. In terms of current systems, you might visualize an avionics module as a complex shop replaceable unit (plug-in circuit board) packaged to withstand a flightline environment. This implies the aircraft built-in test will need to exhibit capability on the order of the automatic test equipment found in today's field shops.

- Acquisition. The modules will have the characteristics of multiple vendor interchangeability, multiple applications across systems and aircraft, and plug-in compatibility with other systems and modules via standardized buses. This may mean changing roles for prime contractors, subcontractors, and the Government.

For the avionics modules described above to have interchangeability, plug-in compatibility, and multiple applications, they will have to have been designed for use with a standard set of interfaces. The Air Force will realize two benefits from this standardization. The first is cost. Quite simply, the judicious application of standardization has, historically, resulted in decreased costs. This conclusion has been verified by recent experiences in programs such as Form, Fit, and Function Inertial Navigation System (F^3 INS) and Combined Altitude Radar Altimeter (CARA)(1). Second, standardization provides for new system growth as well as allowing backfit benefits to older systems. This is an important element of standardization because it becomes a means of establishing technology transparency for new technology insertion into our weapon systems.

There are currently three standards development programs relevant to advanced avionics. In interface standards, the SAE-AE9B committee is formulating a high-speed bus standard. This requirement is crucial to further development in modular avionics. Every advanced avionics architecture relies extensively on a high speed data bus for its inter- and intramodule interfaces. The second standards development program is in software. MIL-STD-1750A standardizes the instruction set for data processors and at least one manufacturer has recommended developing a standard instruction set for vector processors. Higher order languages are also in development. MIL-STD-1589B, the Jovial language standard for embedded computers, will eventually be replaced by MIL-STD-1815, the Ada language standard. The third standardization effort, and the one of concern in this paper, is the module packaging or "form and fit." ARINC Research has been examining advanced 1990s avionics architectures, projections of VLSI/VHSIC technologies, and retrofit requirements to develop a standard for packaging avionics modules.

Existing Module Program

For some time, the Navy has conducted a standardization effort for packaging electronics modules. That program, Standard Electronics Modules (SEM), has been used extensively as a baseline in developing the Air Force module standard. There are, however, differences between Navy SEM and the modular avionics standard in function complexity, level of repair, and technology base.

The functions envisioned for the avionics modules are orders of magnitude more complex. This has created problems in accepting the physical dimensions called for in the SEM program.

The modules, because of the lack of a higher level enclosure, are also expected to be exposed to a much harsher environment than that of the SEM concept. This environment includes such natural elements as rain, salt spray, heat, and cold as well as the man-made elements of chemical, biological, and radiological warfare. SEM, as currently implemented does not provide protection from these elements at module level. Another higher level of packaging protection was always assumed.

The technology base has changed significantly since the SEM program was initiated. One impact has been on the connector requirements. Projected avionics modules will require a low insertion force connector with at least 250 pins. Blocks of pins will also need to be removable to allow installation of twinaxial, coaxial, and fiber optic interconnections. The current SEM "blade and fork" connector does not have this feature.

Although there are some shortfalls in applying the SEM standard to advanced avionics modules, there could be significant benefits in modifying SEM, where necessary, to accommodate the Air Force avionics module requirements. The savings to DoD would be significant if such a program could be established.

Development Approach

The approach to developing the new module standard has been one of full industry participation. For the initial development process, many of the industrial sites involved in advanced avionics development were visited. Those sites included the five airframe manufacturers developing system designs for the Air Force PAVE PILLAR program, the six lead DoD VHSIC contractors for data on their current and projected capabilities and applications, and many electronic systems firms for current packaging techniques and requirements.

After initial investigations of functions likely to be partitioned as modules, parameters were identified for possible inclusion in the standard. They were categorized as either compatibility or functional parameters. Compatibility parameters are those necessary for establishing the physical, thermal, environmental, and electrical interface to aircraft and other systems, and functional parameters are those describing the characteristics of the module function. The compatibility parameters are considered as appropriate for standardization while functional parameters cannot be standardized at this point without significant constraints on design. Table 1 shows the parameters and their respective categories. The physical, thermal, and environmental parameters will be standardized first.

Compatibility Parameters				Functional Parameters (Not Covered by Module Standard)	
Physical	Thermal	Environmental	Electrical	Interoperability	Interchangeability
Form Factor	Heat Transfer Mechanism	TREE	Power Supply Characteristics	Data Bus Protocols	Throughput
Type of Enclosure	Power Dissipation	EMI	Fault Indicator	BIT Protocol	Memory Size
Connector		EMP	Data Bus Interfaces	Data Rates	Access Time
Weight		ESD	Fault Definition/ Isolation Interface (BIT Requirements)		Software
Hold-Down/ Extraction Technique		Humidity			
Cards per Module		Pressure			
Insertion Force		Vibration			

Table 1. Parameter Classification

Some of the electrical and all of the functional parameters, being strongly dependent on system design and integration, will not be covered in the initial standard. There is, in fact, some question that the functional interchangeability parameters will ever be standardization candidates. These types of parameters begin to restrict the design engineer and can constrain innovation.

Full industry participation began this June with the first open forum. The forum provided industry the opportunity to determine content and format of the standard. Beginning with a very skeletal straw man standard, the 225 participants identified and addressed many of the complex issues and determined some of the format and content of the standard.

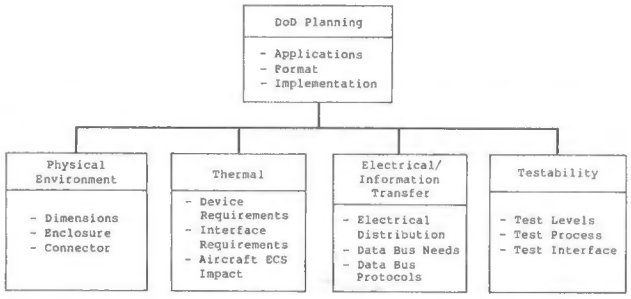
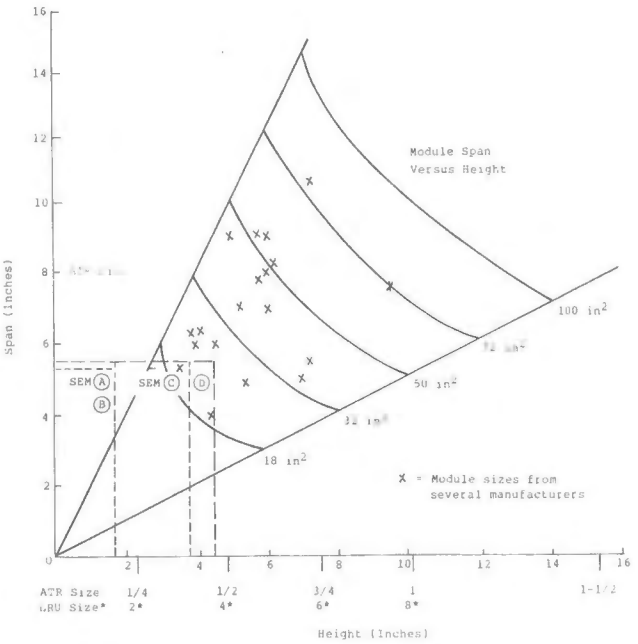


Figure 1. Open Forum Working Groups and Responsibilities

Development Progress on the Modular Avionics Standard

The forum consisted of four technical working groups with each being responsible for specific areas, as shown in Figure 1. The planning group, composed of representatives from the three services and DoD, will be spearheading the coordination required of the standard among the services.

The physical group tackled the difficult problems of dimensions, enclosure, and connector. While not all physical characteristics of the module were prescribed, considerable progress was achieved in defining physical dimensions. In preparing for the forum, we collected considerable data from industry on physical module dimensions. As is apparent in Figure 2, many of the manufacturers had their own ideas on module size. These data show the module sizes for the PAVE PILLAR advanced avionics. This figure, showing the Navy SEM sizes and ATR and LRU sizes from commercial and military standards, is an indication of the many industry positions at the start of the forum. Despite the dispersion of data, the working group decided upon two basic sizes as shown in Figure 3. These two sizes, while allowing sufficient board area for mounting complex functions, also provide for compatibility with Navy SEM sizes, commercial ATR characteristics, and the new military packaging standard for LRUs. These sizes are thus compatible with commercial, Air Force, and Navy packaging. What this means to industry is reduced costs in development and manufacture of modules; for the Government, it means reduction in costs through improved spares stocking and a broader competitive base. Figure 3 shows the relationship between the ATR sizes, Navy SEM sizes, military standard enclosures, and the agreed module sizes. Other consensus was established in the use of one-eighth inch thermal ribs on the module side. This size will



*Denotes LRU size, from draft MIL-STD-XXX, Air Force Avionics Installation Standard.

Figure 2. Current Avionics Circuit Board Sizes

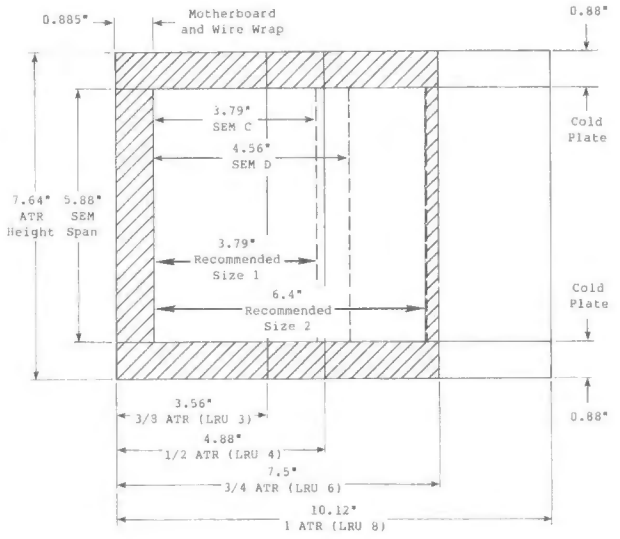


Figure 3. SEM, Open Forum Dimensions, and Commercial and Military Sizes

enable use of heat pipe technology. The retention/extraction method should provide a clear indication of connector pin engagement, and a nonhermetically sealed conductive enclosure will be needed for protection against harsh environments.

Although the physical working group successfully decided some of the key issues on form and fit, there were concerns raised. One of the major issues still requiring resolution is the connector. There was no agreement on type (e.g., twist pin or blade and fork), number of pins (e.g. 250 or 300), insertion force, or keying scheme. Other physical characteristics that will need further study are fault indicator (location, type, and size) and hold-down and extraction mechanism.

The thermal working group, although concerned about the exclusion of forced air flow-through cooling, concentrated on conduction cooled modules. A later provision in the standard may allow the use of modules cooled by flow-through techniques. Flow-through cooling has favorable thermal transfer characteristics, but makes standardization difficult. Three difficulties are:

- Incompatibility with conduction-cooled modules
- Constraining aircraft environmental control systems (ECS) to air cooling. (Advanced system designs have suggested that the use of a closed-loop liquid-cooled ECS may be required in future high performance aircraft.)
- More complex designs than conduction-cooled modules

The thermal working group also concluded that the thermal rib should be one-eighth inch thick to allow the use of heat pipe technology.

Some of the parameters proposed in the straw man standard were discarded as being inappropriate. Many felt, for example, that trying to specify a maximum junction temperature would cause undue constraint without achieving the higher reliability that was needed. Other parameters, such as power density, will need further investigations before they can be finalized.

The electrical working group established pin counts for data bus, power, and ground needs, established the types of modules that would be enveloped by the standard, and characterized the signal types that would be used by the standard modules. The group also decided a standard backplane requirement should not be specified in the standard.

There was little pre-forum information distributed on testability. Even with a lack of information, the working group formulated some testability guidelines for the module. These include a requirement for on-module fault recording in non-volatile memory, defining levels of testability, and developing testability goals for the module program. There was considerable discussion on how module built-in-test (BIT) should be specified. Many felt module BIT should be totally self sufficient at 100 percent fault-detection capability. Others discounted a 100 percent self-sufficient BIT and tried to establish a lower level. As a result, a decision on the level could not be reached. Testability will require much more effort before a standard requirement can be established.

Future of Avionics Installation Standards

The standard will no doubt continue to evolve with the physical, thermal, electrical, and testability characteristics being much better defined as the first module is developed. That still

leaves a question as to whether functional characteristics can or should be standardized. It is expected that many of the commonly used functions such as memory, data processors, and I/O modules will become de facto standards (that is, standards resulting from an informal process of marketplace demand, usage, and acceptance). The microcomputer industry has many examples of this type of standard (e.g., RS 232, Centronics parallel interface). The avionics module functions will be shared among many avionics subsystems. For example, the radar processing function could be shared by the flight control processing function with one system providing back-up or redundancy to the other. This would increase the fault tolerance of the entire avionics suite. However, sharing highly integrated standard resources will not be without its problems.

One problem posed by the new approaches of partitioning and sharing of resources will be in acquisition management. The traditional roles of Government, prime contractor, and subcontractor will no doubt change. There will be a major role established for a systems integrator. The proper responsibilities and interrelationships among Government, prime contractor, and subcontractor will need to be decided.

Another problem created will be the need for test and qualification of the standard avionics modules. The Navy SEM has an extensive testing and qualification program at the Naval Weapons Support Center (NWSC), Crane, Indiana. The expense of establishing and operating such a facility is an excellent justification for establishing a tri-service program.

Finally, the use of the advanced avionics modules and the goal of eliminating intermediate maintenance support equipment will require extensive software on board the aircraft with all the development and maintenance costs associated with software.

In spite of these problems, there are tremendous benefits to be realized from standardization. The commercial airlines have been using LRU or box-type packaging standards, such as the ARINC 600 characteristic, for years with a great deal of success. The Air Force is now going a step beyond the current commercial packaging with the packaging guidelines for the modular avionics standard.

Summary

Avionics systems are about to undergo drastic changes in the partitioning of functions and judicious sharing of resources. These changes have the potential to significantly improve reliability and maintainability and to reduce costs.

Such changes, though, need to be effectively managed and controlled by the establishment of guidelines for the system designers. This standard will provide such guidelines. By meeting packaging and selected interface rules, new systems can be compatible. The degree of compatibility will depend on a steady, well planned standards development program supported by active industry participation.

Reference

(1) Stewart Baily, "F^3 Standardization -- Does It Work?", 5th Digital Avionics Systems Conference, Seattle, November 1983.

Biographies

William Radcliffe is a Senior Engineer in the Advanced Systems Program of ARINC Research Corporation. He is currently project engineer for the development of advanced avionics integration standards. Previously he was associated with acquisition programs at the USAF Systems Command, Aeronautical Systems Division. Prior to that, he was an Air Force avionics technician. He has experience with Doppler radar, inertial navigation, and embedded computer systems on various aircraft. Mr. Radcliffe received a bachelor's degree in industrial engineering from New Mexico State University in 1973 and a master's degree in industrial/systems engineering from Ohio State University in 1981. He has also completed graduate work in computer engineering at Wright State University.

Mr. Donald J. "Joe" Boaz is currently with the Air Force at the Air Force Avionics Laboratory. He has over 25 years of system design experience in both industry and the government, including the Naval Tactical Data System, Titan II, the Army's Main Battle Tank Program, Apollo Guidance System, Transit Satellite Navigation System, GEANS Inertial Navigation System, and IFFN Fusion. More recently, he has been involved in modular avionics standardization and other designated issues associated with the PAVE PILLAR program. Mr. Boaz received a bachelor's degree in electrical engineering from the University of Illinois in 1957.

84-2749

HIGH DENSITY MODULAR AVIONICS PACKAGING

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Abstract

Next generation avionics system requirements are discussed and a high density modular packaging approach specifically designed for airborne systems is presented. Design information and test data are given for the packaging system and prototype hardware.

High Density Modular Avionics Packaging

There has been a great deal of discussion recently concerning the standardization of electronic funtions and packaging to improve the utility of future military systems. The Air Force, Army, and Navy have all expressed desires for a practical standardization of common functions to reduce development time and cost while improving reliability, maintainability, etc., through volume production of proven elements.

The standardization of IC functions and DIP packaging revolutionized electrical design and manufacture and was sufficient for many years. New systems however, have reached extraordinary levels of complexity and require a higher level of functional integration and standardization for practical program execution. Standard modular functions with common electrical and mechanical interfaces will provide the building blocks of next generation avionics systems. Pave Pillar, VHSIC, and many other programs are providing the keystone technologies for these future systems.

The packaging technology is a key element to the success of these endeavors and a revolutionary change in the hardware must occur to simultaneously meet all of the new system requirements. Some of the new hardware trends are:

Increased Packaging Densities - New systems require a 4X-6X improvement in packaging density ($IC's/in^3$). This is typically accomplished with leadless chip carriers and surface mount interconnect technology.

Improved Electrical Performance - Faster system speeds and low energy circuits require low capacitance, controlled impedance interconnects, and low noise power distribution.

Improved Thermal Management - The increase of component densities and the reduction of component junction temperatures requires an order of magnitude improvement in heat transfer efficiency.

Improved System Testability - Sufficient Built-In-Test must be provided in the system to fault isolate individual functional modules.

Fault Tolerant Architectures - System reconfiguration with redundant functional elements must be provided for failsafe system operation.

Two Level Maintenance - Faulty modules must be capable of flight line replacement with subsequent depot repair. This poses severe environmental requirements on the small functional subassemblies.

Reduced Life-Cycle Cost - Future systems will be unaffordable without significant reductions in development, manufacturing and maintenance costs. Proven elements must be commonly used across system boundaries to avoid redevelopment, requalification, etc. System reliability must be improved.

This combination of system requirements can only be met with a modular standardization of system architectures, hardware, and software components. The development of universally accepted standards will be a slow, tedious, and iterative process involving many technologies and organizations. Definitive resolution will be impossible in some cases due to the inaccuracy of technology predictions and military cultural trends. But, decisions must be made and standards must be adopted with the hope of evolutionary acceptance by a worthwhile majority.

History has shown that the longest lived technologies and standards are the simplest in nature and thus adaptable to evolutionary growth. The same will be true of avionics standardization. The simplest concepts and techniques which meet the key requirements will be the ones that will last.

Any standards which are levied at this time must be supported in the near term by existing technologies in a producible format and they must be simple enough to adapt to future technologies and manufacturing methods.

Texas Instruments has developed a simple modular packaging architecture to meet the requirements of next generation avionic systems and contemporary manufacturing processes.

This packaging scheme was developed as a common focal point for the various packaging technologies within TI and has been modified for compatibility with the military standards developed for the Air Force by ARINC.

High Density Standard Modules (HDSM's)

HDSM specifications simply define a "form and fit" standard for a variety of module sizes which are compatible with standard ATR case sizes (1/2, 3/4, and 1) and integrated racks. A module is typically constructed of two surface mount circuit boards as shown in Figure 1. The modules are conduction cooled to edge-clamped cold plates and can be used with or without covers. Ejector handles are provided for easy removal and installation of the modules in a flight line environment.

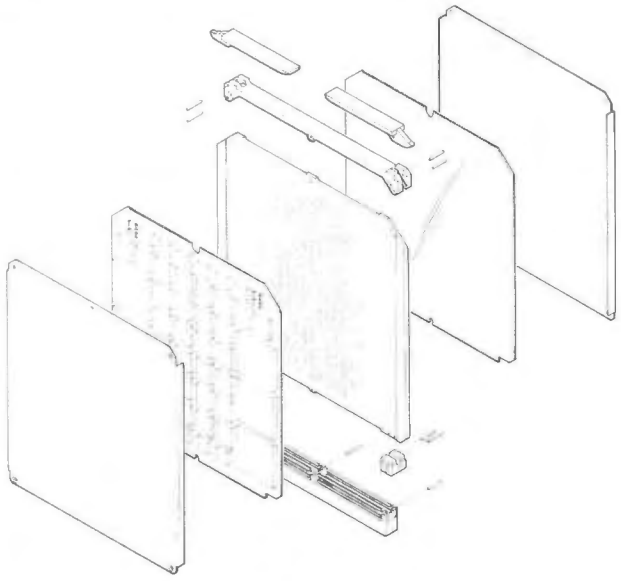


Figure 1. Exploded view of HDSM.

HDSM Form Factor

HDSM's are available in three basic form factors with incremental thicknesses. The three sizes are shown in Figure 2. A Size-4 module will fit in a Size-4 LRU (1/2 ATR), and so on for the other module sizes. The widths of all the modules is common at 5.875 with different heights as shown in the figure.

The thickness of each module is allowed to vary incrementally to accommodate various device sizes and circuit assemblies. Most chip carrier modules will be less than .50 inches thick. RF and other special modules will be thicker. For any given system a common module size and standard spacing should be chosen for simplicity. The choice of module size is a function of avaliable space, the size of the circuits to be packaged, and the size of other standard function modules which may be used in the system. Most of the functions studied to date (90% +) fit nicely on a Size-6 module of either .48 inch thickness for digital circuits or .98 inch thickness for RF and special circuits.

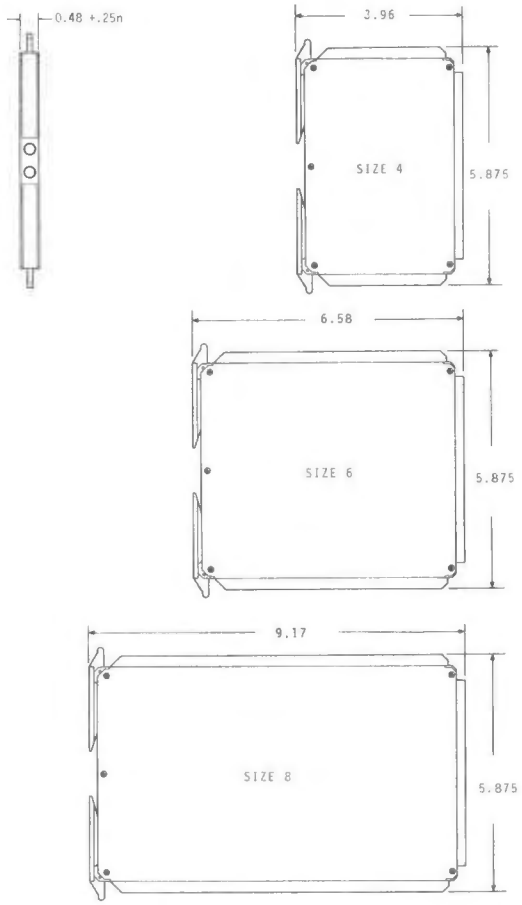


Figure 2. HDSM sizes.

There are two mounting ribs on each module located on the centerline or offset depending on the module size and type. Each rib extends .27 inches from the edge of the module and is .125 inches thick for clamping to the cold plate. This design is intended to provide a simple means of extending the thermal plane straight into the mounting ribs. This approach is easiest and cheapest to manufacture plus it is very adaptable to all types of conduction media including metals, graphite, or heat pipes.

Multiple ribs and multiple board assemblies within one module are not recommended due to the manufacturing and maintenance complications but can be accomodated with volume, weight, and cost penalties.

Time and real hardware experience will determine if one module size predominates. A premature decision on a particular form factor could significantly impede the overall system development especially if too small a module is specified.

HDSM Thermal Management

The center mounting plate serves a dual role as mechanical support structure and conduction cooling media. It must be designed to meet the mechanical requirements of the circuit board materials and the thermal requirements of the circuit design. In modules that use polymer circuit boards with leadless chip carriers, the mounting plate will often be made of a low expansion rate material such as Copper/Invar/Copper or Graphite to control the stress in the solder joints. If ceramic or controlled TCE circuit boards are used, the mounting plate may be made of aluminum or other more conventional materials.

Special considerations must be taken to ensure adequate heat transfer from the IC junctions to the module mounting ribs. Appropriate device packages must be used to accomodate the specific power dissipation and the components should be properly placed on the module to avoid hot spots. Higher power components should be placed near the edges of the modules and spread out as much as possible. And finally, the materials and the thermal cross section of the circuit boards and mounting plate must be appropriately chosen.

Size-6 HDSM's have been fabricated which effectively cool up to 50 watts per module (40 watts avg.) in a MIL-STD-XXXX AIDS enclosure. The test modules were fabricated with aluminum structural components and ceramic circuit boards. Junction temperatures did not exceed 105°C with a maximum cooling air temperature of 71°C. Figure 3 illustrates the thermal model for an HDSM with a comparison between predicted and measured data. Typical dissipations of 40 watts per module should be easily handled in most system applications. Higher dissipations are achievable with the use of heat pipes and/or liquid cooled cold plates in the future.

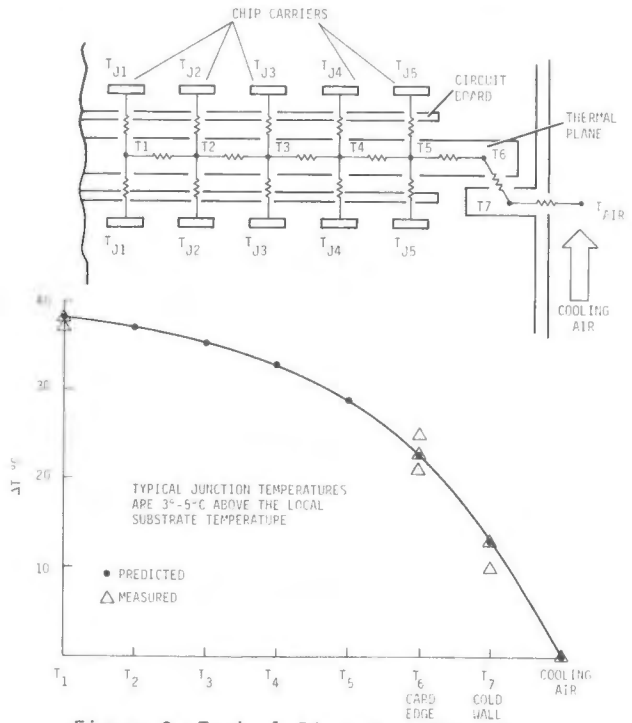


Figure 3. Typical 50 watt module in a MIL-STD-XXXX enclosure.

HDSM Connector

A standard module connector is the single most important element in a module standard. The connector must be versatile and easy to use with any type of module.

The HDSM connector family offers a variety of contact types and quantities in the same basic shell design. The connector is designed for surface mounting on both the module and motherboard sides with alternate terminations available as an option. The basic design offers up to 304 high reliability twist-pin contacts in four rows on .050 inch centers. Figure 4 illustrates the HDSM connector.

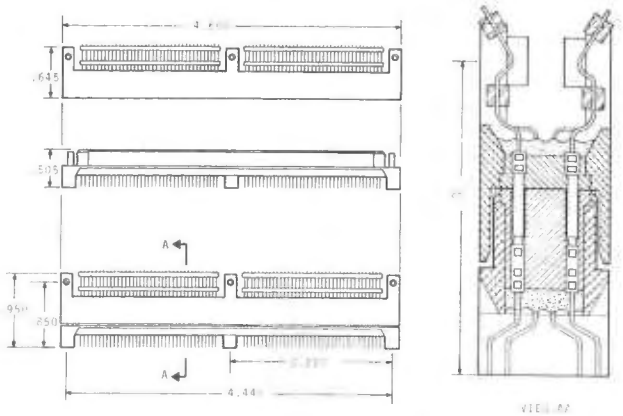


Figure 4. HDSM connector.

Different modular inserts may be specified to include coax, fiber optic or other special contacts. There are four modular inserts in each connector as shown in Figure 5.

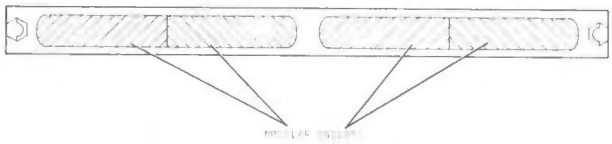


Figure 5. HDSM connector with modular inserts.

The standard inserts which are currently available are listed below:

Insert #1 - 76 twist pin cavities
Insert #2 - 6 coax contact cavities
Insert #3 - 4 coax or fiber optic cavities

Any of the inserts may be partially or fully loaded and installed in the connector shell in various configurations to suit the requirements. Any individual contact may be replaced.

The module connector is attached to the thermal plane with three press fit pins. The connector will slide on the pins (± .010 inches) to improve mating and relieve tolerances in the chassis and motherboard. The connector leads are surface soldered to both sides of the module. Flying leads are available for all contact types and Flex circuits may also be used to interconnect the contacts to the circuit boards.

The motherboard connector is attached with three screws which are inserted behind the motherboard into the connector. The contact leads are surface

soldered (butt joint) to the top of the motherboard. Coax and Fiber Optic leads extend through the motherboard and are routed and/or interconnected behind it. Mini wirewrap pins on 50 mil centers are available for the motherboard connector. These pins are tedious to use but do provide prototyping capability if required.

Low force contacts are used in the HDSM connector with a maximum total insertion force of 55 lbs. for the 304 contact version. This insertion force translates to approximately 14 lbs at the handles (7 lbs each).

Six position rotatable keys are provided to personalize each unique module connector. The keys are programmed during module and backplane assembly. No contacts will mate unless both connector halves have the proper keying. Typical connector specifications are given in Table I. HDSM connectors are available from MALCO, South Pasadena, California.

GENERAL	THE HDSM CONNECTOR IS GENERALLY IN COMPLIANCE WITH THE REQUIREMENTS OF MIL-C-55302.
DIMENSIONS	4.60 LONG X .35 WIDE X .86 (INCHES). (SEE FIGURE 8)
CONTACT COMPLEMENT	304 TWIST PINS, OR 20 COAX CONTACTS, OR 16 FIBER OPTIC CONTACTS, OR A MODULO COMBINATION THEREOF.
INSERTION FORCES	LESS THAN 3.0 OZS. PER TWIST PIN, LESS THAN 1.0 LBS. PER COAX CONTACT, LESS THAN 1.0 LBS. PER FIBER OPTIC CONTACT.*
CURRENT CAPACITY	3 AMPS/TWIST PIN.
CONTACT RESISTANCE	LESS THAN 8 MILLIOHMS/TWIST PIN.
DIELECTRIC WITHSTANDING VOLTAGE	500 VRMS, 60 HZ @ SEA LEVEL, 300 VRMS, 60 HZ @ 70,000 FT.
USER CONTACT BANDWIDTH	DC TO 500 MHZ.

*FIBER OPTIC CONTACTS WILL ACCEPT CABLE DIAMETERS UP TO 2.25mm O.D.

TABLE I HDSM connector specifications.

HDSM Performance Specifications. Table II summarizes the HDSM performance parameters. Data is for aluminum chassis modules with ceramic circuit boards and leadless chip carriers.

	SIZE-4	SIZE-6	SIZE-8
BASIC DIMENSIONS (INCHES)	3.95 X 5.85 X .86	6.40 X 5.85 X .93	9.15 X 5.85 X .98
USEABLE CIRCUIT AREA(IN^2)	15 IN^2 EACH SIDE	28 IN^2 EACH SIDE	41 IN^2 EACH SIDE
IC COMPLEMENT (.15 INCH BODY SPACING)	UP TO 100 20 PIN LCCs	UP TO 215 20 PIN LCCs	UP TO 316 20 PIN LCCs
WEIGHT (TYP.) WEIGHT (TYP.) WITH COVERS	.62 LBS .75 LBS	1.00 LBS 1.25 LBS	1.45 LBS 1.75 LBS
POWER DISSIPATION	25W MAX 20W TYP	50W MAX 40W TYP	75W MAX 60W TYP
DELTA T JUNCTION TO CASE (DIE)	14°C TYP 20°C MAX	14°C TYP 20°C MAX	14°C TYP 20°C MAX
CONNECTOR	SEE TABLE I		
WARPAGE	156 TYP	156 TYP	156 TYP
ENVIRONMENTAL	MIL-E-5400, CAT. II, CLASS 2X OR BETTER		

TABLE II HDSM specifications.

HDSM Application Requirements

Circuit Applications

Digital, RF, and Power Supply circuits are currently under development in an HDSM-6 form factor. The interconnect media and internal packaging approach are different in each case but the HDSM interface standards are maintained. Different circuit applications will continue to require a variety of package types, interconnect techniques, and internal cooling schemes for optimal performance. There is no packaging panacea expected in the near future to bridge the gap between all electrical technologies. Tradeoffs must be made and the appropriate hardware implementation must be chosen to support the electrical and thermal requirements of each different functional category.

HDSM's will support most surface mount circuit applications with little or no modifications. Special applications will require special provisions inside the module but are usually compatible with the overall architecture and cooling scheme. Figures 6, 7, and 8 illustrate Digital, RF, and Power Supply applications. Preproduction units will be completed in 1985.

System Considerations

HDSM's are designed for analog and digital interconnection on a common surface mount backplane with RF, fiber optic, and other special interconnect behind the backplane. The extremely high routing densities required in the motherboard are much more achievable with a surface mount design than with through-the board leaded designs. The absence of extended leads allows more routing channels for a fewer number of layers and easier impedance control.

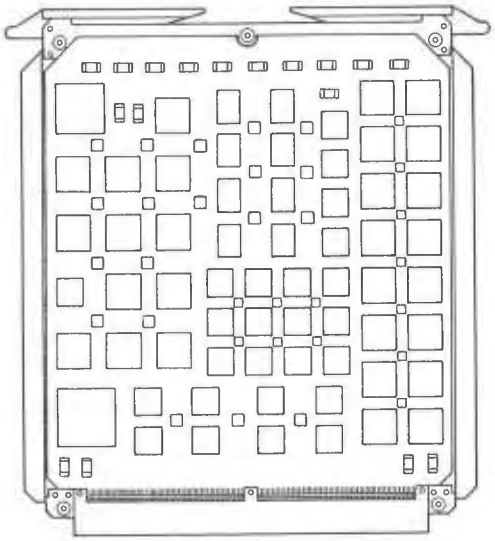
High density modules require a more efficient heat sink design to handle the higher power densities. Entry length boundary layers and large surface areas are required to provide the high efficiencies without a high pressure drop. Liquid cold plates can handle higher heat loads more efficiently but are not practical for all applications.

The modules must be firmly clamped to the heat sinks with wedge-type clamps or an equivalent mechanism to assure a low impedance thermal path. The HDSM ejector handles are designed on the same centerline as the card edge so they will not interfere with the clamping mechanism or actuator access.

Tolerance control on the machined assemblies is much more critical with high density packaging than with conventional approaches. Accurate module alignment with the heatsinks and the backplane is required for proper mating and mechanical integrity.

Power Supplies

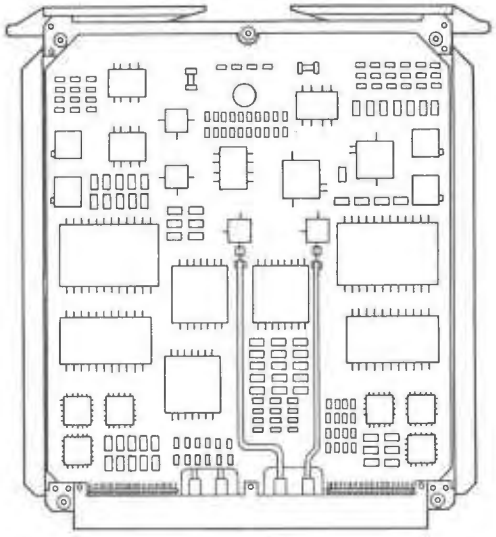
Higher power densities pose new problems in power distribution. Low voltage circuits have extremely large supply currents which must be uniformly distributed throughout the chassis. The power supply regulators should be distributed throughout the card cage wherever possible to reduce bottlenecks and improve transient response. Redundant supplies with current sharing should be used to achieve the required reliabilities. The power supplies must also be of comparable density to the rest of the system. The total volume for power supply components should not exceed 25% of the system volume. For a typical HDSM system this relates to about 10 watts/in^3 for the power supply. High density, high reliability power supplies are a key element in all system designs. The development of these units is non-trivial and must be done in conjunction with the rest of the system technologies to ensure overall system compatibility.



DATA FLOW SEQUENCER

- Distributed Task Controller
- Custom Bit Slice Processor
- 6 MHz Clock Frequency
- 134 IC's in Leadless Chip Carriers
- Controlled Impedance Ceramic Thick Film Circuit Boards
- 50 watts Dissipated Power
- HDSM-6 (.48 inches thick)
- 152 Pin HDSM Connector
- 1.0 lbs Total Weight

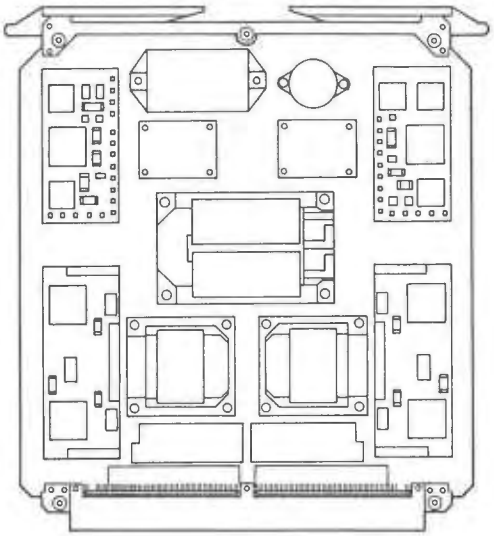
Figure 6. Data Flow Sequencer.



I/Q DETECTOR @ A/D CONVERTER

- Two Channel Coherent Detector
- 6 bit 100 MHz A/D
- Custom, Flatpack, and Hybrid packages
- Controlled Impedance G-10 Multilayer Circuit Board
- 46 watts Dissipated Power
- HDSM-6 (.73 inches thick)
- 152 pin HDSM Connector with 6 Coax
- 1.5 lbs Total Weight with covers

Figure 7. I/Q Detector @ A/D Converter.



HIGH DENSITY POWER SUPPLY

- High Efficiency Switching Regulator
- 10 watts/in^3 Power Density
- 270 VDC Input (MIL-STD-704C)
- 5 VDC Output: -40 amps normal
  -60 amps overload
- Parallel Output Capability with Current Sharing
- Continuous Monitoring of Power Status and Critical Module Temperatures
- 80% efficiency typical
- 50 watts Dissipated at 40 amp output
- HDSM-6 (.48 inches thick)
- 152 pin HDSM Connector
- 1.5 lbs. Total Weight with covers

Figure 8. High Density Power Supply.

System Testability and Maintenance

In addition to higher reliability, next generation avionics require improved fault isolation and simpler maintenance procedures in order to reduce the cost of ownership. Each system must be able to localize faults to individual replaceable modules. This can either be done with built in test circuitry in each functional module or by a maintenance node in the system which can exercise all of the modules and evaluate their performance. Most systems will probably use a combination of these two methods to achieve fault isolation. Module status must be available to the system monitor via the system maintenance bus.

After a faulty module is identified it needs to be replaced as quickly as possible in order to avoid system down time. Flightline replaceable modules (LRM's) are desired for optimal maintenance procedures.

Repairable modules will use depot level test equipment to isolate faulty components.

This approach will require a radically different equipment bay design and environmentally resistant modules. Integrated racks, such as the one shown in Figure 9, have been proposed to house the modules with convenient access through removeable front covers or doors. There are many trade-offs which must be made to determine if this type of approach is compatible with all of the system requirements and if so what the ideal configuration will be.

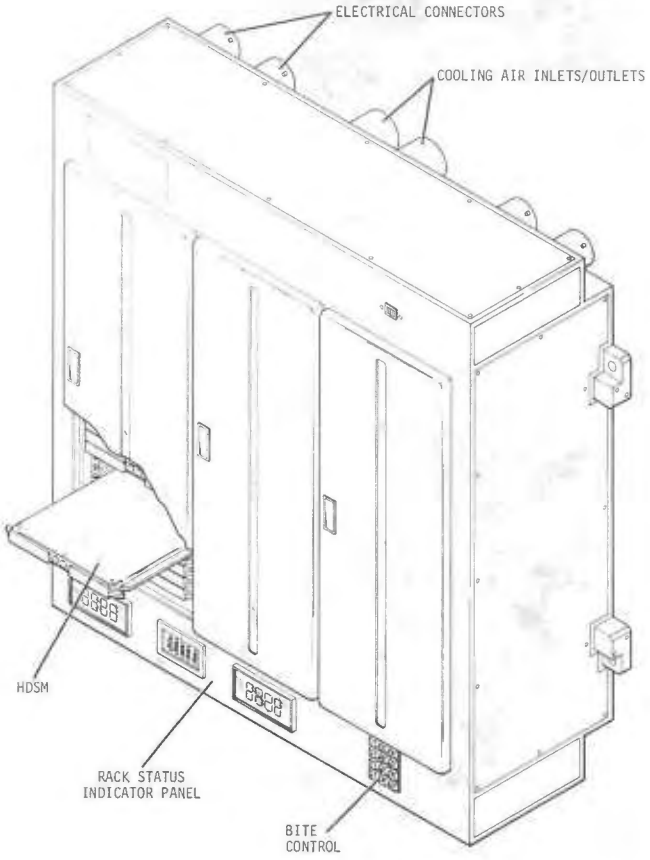


Figure 9. Integrated rack.

Modules which are compatible with flightline replacement will have to be more substantial and environmentally resistant than previous electronic subassemblies. HDSM's are designed to incorporate removeable metal covers which serve as electrical and mechanical shields. The covers add approximately 25 percent to the weight of the modules and would be used only on line replaceable modules or when electrical shielding is required. The HDSM connector uses a rugged metal shell with recessed contacts to resist abusive handling. High density module connectors will never be as rugged and environmentally sound as LRU-type bulk connectors but will survive in a two level maintenance environment if certain precautions are observed. Special electrical filtering and terminations must also be incorporated inside the modules to prevent damage from static discharge and EMP.

Specific requirements for environmental resistance will need to be generated as the two level maintenance scheme develops. It is impractical to expect each individual module to handle all of the environmental conditions which are exposed to a system. The impact of the environmental requirements must be distributed across the system to minimize the risk of this new approach. Again, a simple overall system approach is required which is flexible enough to evolve with the other technologies.

Prototype Hardware

An integrated HDSM demonstration system is currently under construction and will be completed in 1985. The system will include digital, RF, and power supply modules in a MIL-STD-XXXX enclosure with a high density surface mount backplane. Figure 10 illustrates the HDSM demonstration system. Future efforts will be geared towards the development of an integrated rack for true two-level maintenance capabilities.

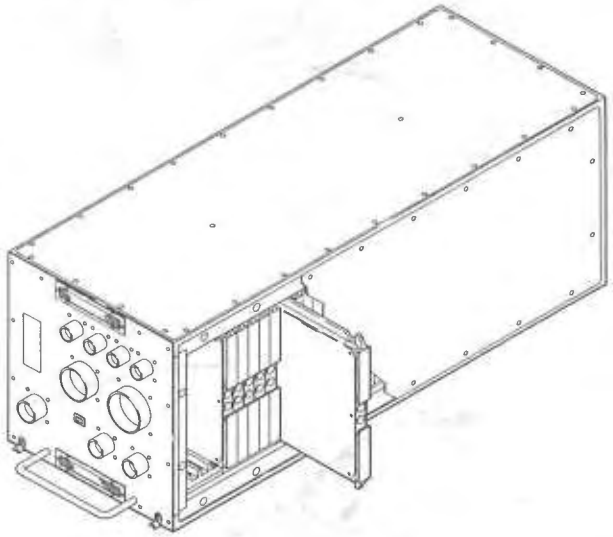


Figure 10. LRU demonstration system.

Some examples of prototype high density packaging hardware are shown in the following figures. These functional units were used to evaluate various technologies during the development of HDSM's and the related system hardware.

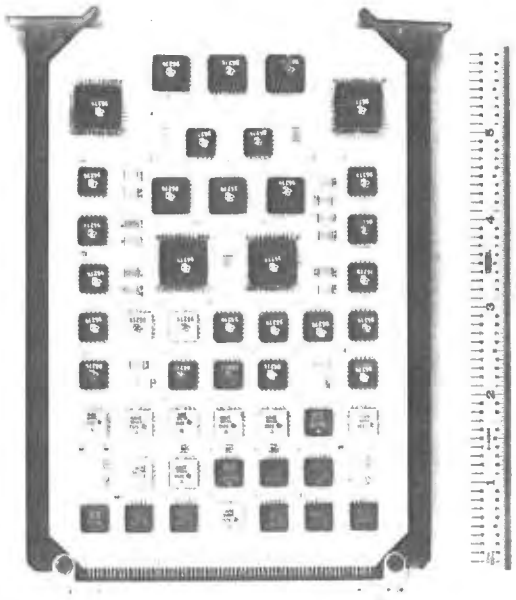


Figure 11. TTL digital circuit module which operates at a 35MHz clock rate on controlled impedance ceramic circuit boards.

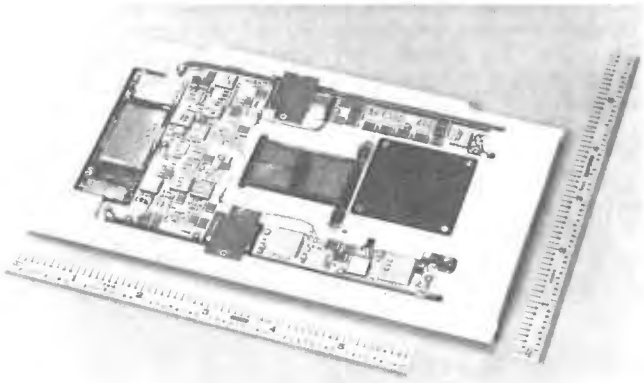


Figure 12. High density switching power supply with four low voltage outputs and an overall power density of 10 watts[3].

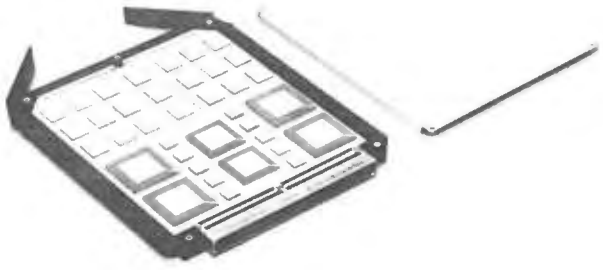


Figure 13. Prototype HDSM used for electrical and environmental evaluation.

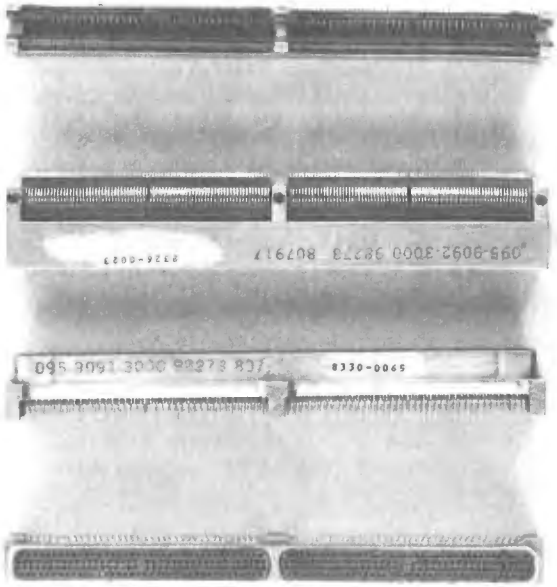


Figure 14. HDSM connector.

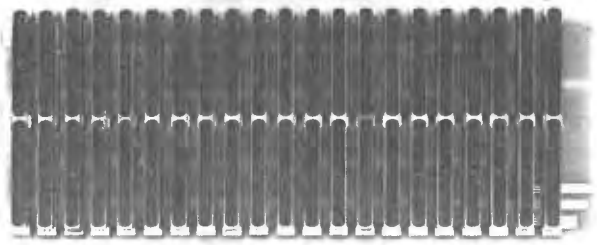


Figure 15. HDSM connectors integrated into a high density surface mount mother board.

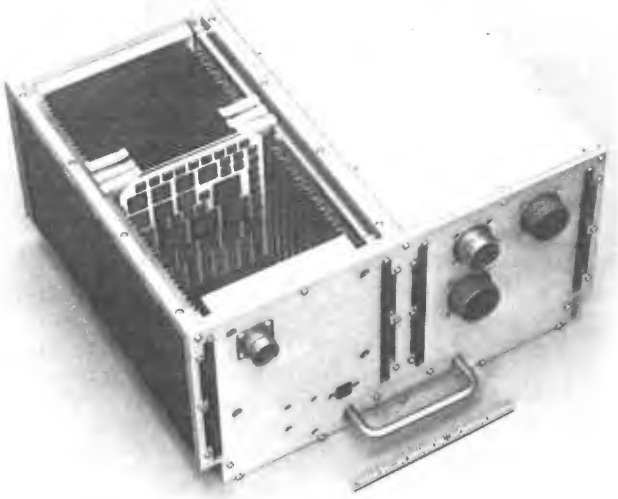


Figure 16. Prototype high density LRU with high efficiency heatsinks.

MODULAR AVIONICS PACKAGING STANDARDIZATION

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and

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Advanced Avionics Packaging Branch

ABSTRACT

Advanced integration technologies such as high speed data busing, Built-In-Test (BIT), Very Large Scale Integration (VLSI) and Very High Speed Integrated Circuit (VHSIC) provide an opportunity to further integrate military avionics systems. These new technologies can be severely limited if placed in conventional avionics system architectures. To fully utilize the benefits of these technologies, modular packaging standardization across multiple functions, multiple systems, and multiple airframes is needed. New methods of packaging this new generation of avionics are necessary to capitalize on benefits such as common resources, improved maintainability, increased reliability and reduced life cycle costs.

INTRODUCTION

Historical Approach. Historically, avionics have been designed, procured, and maintained as discrete 'black boxes', each dedicated to a specific function. Little control has been placed on the details of internal design. Each piece of equipment is treated as a new development yielding individual and inefficient thermal control, little commonality, and the need for additional trained maintenance personnel. This approach to avionics packaging has resulted in low reliability, poor maintainability, spares shortages, and a dependence on the avionics intermediate maintenance shop and its highly skilled personnel and complex test equipment. All of these factors have contributed to excessive avionics equipment Life Cycle Costs (LCC).

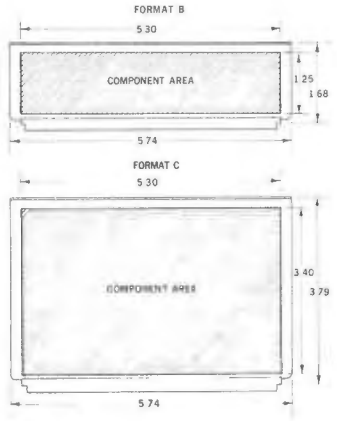
One proven method of diminishing the rate of increase of these life cycle costs is to implement a common modular packaging design strategy for common, generic, and widely used applications. This converging of diverse packaging methods toward a common set of standard interfaces on multiple levels of modular packaging elements produces increased reliability, improved maintainability and a reduced cost of ownership.

Essential ingredients to a modular interface standard are form and fit standardization, flexibility, non-proprietary parts or processes, proven reliability, interchangeability, and adaptability to future technologies. An interface standard must not impose unreasonable requirements on the designer. The developer must be free to use its expertise within these guidelines to insure a competitive advantage.

Modular Avionics Packaging. The Modular Avionics Packaging (MAP) Program addresses the packaging aspects of future military avionics systems with the objective of improving reliability, maintainability, supportability and reduce equipment life cycle costs. The MAP Program is tasked with identifying, developing, and implementing avionics packaging concepts that satisfy the stringent high density, lightweight, high reliability, and improved maintainability requirements of military avionics systems. These program objectives are oriented toward technology rather than a specific system; therefore, emphasis is placed on state-of-the-art packaging techniques usable for both future and retrofit applications.

The MAP Program approach addresses multiple levels of integrated modular avionics packaging. These levels are represented by the Standard Avionics Module (SAM), the Standard Enclosure (SE), and the Integrated Rack (IR). Each level represents a discrete set of interface standards and designed, developed and tested hardware configurations which follow a modular approach to avionics packaging.

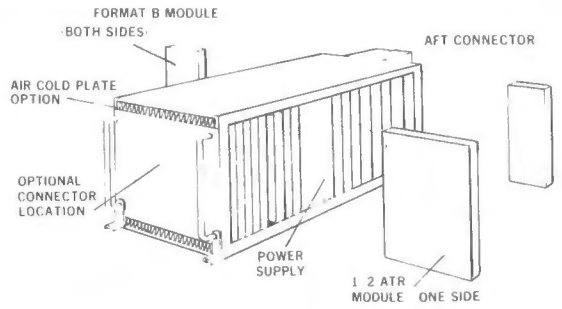
At the module level, the program standard module formats are established with sufficient circuit area, component mounting options, thermal dissipation methods, and electrical interfaces to allow their use in many military avionics systems. (Figure 1) The Format B module fits neatly into the 1/4 ATR (2 Modular Concept Unit (MCU)) enclosure. Several Format B standard functional modules are documented, qualified and sourced, ready for immediate application to new avionics



STANDARD AVIONIC MODULES
Figure 1.

system developments. The Format C configuration is designed for a 1/2 ATR (4 MCU) enclosure and facilitates a variety of component mounting technologies and circuit areas. Several avionics systems in the development stage are using the Format C as the packaging design strategy. Within these systems, functions such as data processors, signal processors, memory, bus interfaces, analog to digital and digital to analog converters, various radio frequency and analog devices and many others are being developed. The technologies on these modules range from discrete components to VLSI and VHSIC.

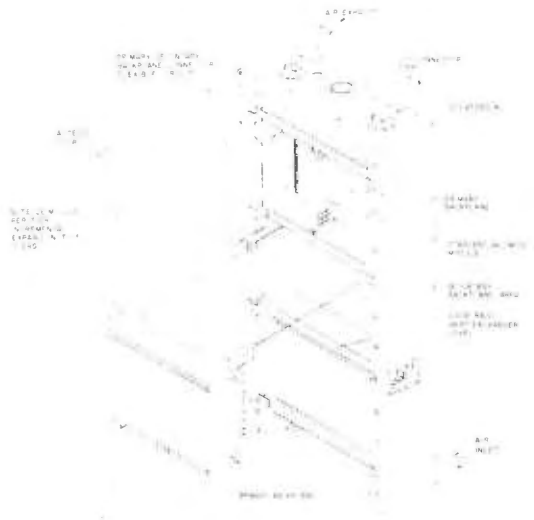
At the enclosure level, a family of modular, high density, thermally efficient Standard Enclosures has been developed. (Figure 2) These Standard Enclosures are designed to provide the electrical, thermal, environmental, and mechanical interface between the Standard Avionics Module and the airframe. The enclosures are compatible with the Air Force sponsored MIL-STD-XXXX and cover the 2, 4, 6, and 8 MCU configurations. The 1/4 ATR (2 MCU) enclosure may be combined with the 1/2 ATR (4 MCU) enclosure to form a 3/4 ATR (6 MCU) enclosure and two 1/2 ATR enclosures may be combined to form a full ATR (8 MCU) enclosure. This allows the efficient packaging of the Format B and Format C modules in a variety of enclosure configurations to meet individual system requirements. The initial design is forced air cooled but is also adaptable to self cooled or liquid cooled applications. These enclosures are suited for many future as well as retrofit applications.



STANDARD ENCLOSURE CONCEPT

Figure 2

The Integrated Rack is designed to package multiple systems or subsystems within a single enclosure which provides the necessary thermal, environmental, mechanical, busing and power interfaces. (Figure 3) This design permits weight and volume savings, the use of common busing techniques, and module level maintenance. The MAP developed IR is divided into two to five tiers. Each tier consists of the heat exchanger/module retainer mechanism, primary backplane, and standard avionics modules, all totally enclosed and removable as an assembly. System busing, power and inter-tier connections are provided through a secondary backplane. The IR is designed as a forced air cooled enclosure although it is also adaptable to other cooling technologies. The IR is a modular enclosure suited for many future avionics system applications permitting further avionics system integration with increased reliability, improved maintainability, and a reduced cost.



INTEGRATED RACK WITH AIR-COOLED GUIDE RAIL

Figure 3

BENEFITS OF MODULAR AVIONICS PACKAGING

Low Risk Design. Each time a new system is designed, the system designer is called upon to analyze the thermal and mechanical characteristics of the proposed system. This step, although crucial to the reliability and performance of the system, is often times not given the consideration warranted at this most critical design point. This stage frequently adds an element of risk which is eliminated through the use of modular packaging standards having known performance and proven reliability. In the development of the MAP standard modules, enclosures and racks, the thermal, environmental and mechanical effects were carefully researched and proven through the design, manufacture and test of hardware. When these modular packaging specifications are used to package the system in the early stages of the design, the risk of the production version not meeting the expectations of its designer is dramatically reduced. Several of the modules used in the early stages of design may be used in the production version of the equipment. (Figure 4) This common set of modular interface requirements provides low risk design with sufficient flexibility to package many different systems, during several phases of the design process.

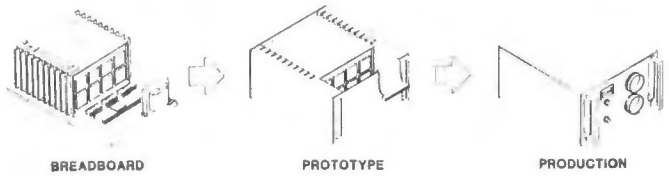


Figure 4

Technology Independence/Common Functions. With the evolution of modular packaging standardization, functional commonality is inevitable. This aspect of modular standardization has benefits reaching all aspects of system design and support. Functional commonality permits such benefits as off the shelf functional elements and enclosures for breadboard/brassboard design, qualified multiple sources, and common functional modules between systems. These effects considerably impact the design and support of avionics equipment. The obvious benefits to the system designer are the availability of functional hardware, reduced design costs and reduced development times. The benefit to the military is realized mainly in the support phase of the equipment life cycle. This savings is seen in the availability of common functional modules used in multiple systems yielding increased operational capability of the equipment at a reduced cost. This savings is realized through the economies of mass production, a decrease in associated system documentation, and a reduced dependence on the avionics intermediate shop.

Multiple sourcing of functional modules is accomplished by using functional specifications within a specified mechanical, thermal and electrical envelope. Functional interchangeability is insured at the specified interfaces and is not concerned with how that function is performed. This permits the module developer unlimited latitude in component selection and circuit design. The only requirement on the module developer is that the module will perform as specified, with qualified reliability, and is built within the specified module envelope. Technology independence is thus achieved by the fact that the components, circuitry, and the technologies required to execute the specified function are subject to improvement by the module developer or a competitive source.

Improved Maintainability. With support costs of avionics increasing almost exponentially, perhaps it is time to re-evaluate the traditional methods of military avionics equipment support. New technologies require an advancement in integrated avionics architectures. The insertion of new technologies into existing architectures severely limits the positive impact these technologies can have on performance, reliability and maintainability. New system architectures call for resource redundancy, fault tolerance, dynamic reconfiguration and mission dependent configurations. These requirements demand an alternative to the traditional methods of packaging and maintaining avionics systems. The use of a multi-level modular packaging approach significantly changes the way in which avionics systems are designed and maintained.

Avionic systems are currently developed, procured and maintained at the 'black box' or enclosure level. As the cost of these enclosures skyrockets, it has become increasingly difficult to keep the spares pipeline sufficiently stocked with the correct number and type of spares. When multiple sources supply a particular black box to a fit, form, function specification, each one requires its own set of unique spare parts and assemblies. This proliferation of spare types has grown to extremely unmanageable proportions. The additive effect of this increase in the number and type of spares is devastating.

This area provides an opportunity for a significant improvement in avionics system maintainability. Traditionally, when a piece of avionics equipment fails, the entire unit is removed from the aircraft. Much of the failed system still functions correctly and only a small portion has actually failed. One viable solution is to repair the system by replacing only failed modules instead of the entire enclosure. This method of system maintenance provides an alternative to keeping entire systems or black boxes in the spares pipeline.

In order to implement a module level maintenance program, integration techniques such as modular packaging concepts, advanced busing, VLSI/VHSIC, self-diagnosis and fault isolation must be exploited. The use of advanced busing techniques dramatically decreases the equipment failures historically attributed to the cables and connectors which account for a significant portion of the total system failures. VLSI and VHSIC technology will permit an increase in functional density providing more capability to be packaged into smaller volumes with fewer external connections. This phenomenon permits the packaging of discrete complex functions onto a single module. Fault diagnosis and isolation through the application of built-in-test (BIT) enables the replacement of failed modules in a system without the dependence on expensive test equipment and skilled maintenance personnel. By applying these technologies to module level fault isolation, replacement, and spares inventorying, the cost and time required for maintaining avionics equipment is drastically reduced. These objectives can be achieved through the application of the MAP standard module formats in conjunction with the Standard Enclosure and the Integrated Rack.

Data Package Maintenance. Data package maintenance is the process of documenting equipment updates, revisions, and repairs. The use of modular avionics aids in this process by taking advantage of existing documentation and modular design. Much of the labor required for data package maintenance is redundant and is eliminated through the use of existing functional and mechanical documentation.

Life Cycle Costs. Life Cycle Costs (LCC) include all of the costs associated with the design, development, procurement and support of a piece of avionics equipment. This LCC can generally be broken down into development/procurement costs and operational support costs. These two categories of cost account for the total equipment cost.

The system development cycle may span months or years depending on the complexity of design, the available technology and available hardware. The cost of system development may be reduced by decreasing the length of the design cycle. This is easily accomplished through the use of standardized modular packaging methods. By having reliable hardware and functional elements available, the designer is able to take advantage of existing technologies where applicable. Integrating the available hardware and functional

components into the design requires that less time and resources be spent on redundant design and thus more time and resources are made available for the development of system unique functions. By procuring much of the hardware and functional modules from competitive sources, the system designer takes advantage of shorter lead times and lower pricing. Using this method of design, the transition from brassboard to production is made smoothly due to the existence of qualified sources for hardware and functional modules. These effects are multiplied if the design effort is an update or enhancement to an existing system which uses a similar modular packaging approach. This allows many of the same functional entities to be reused or slightly enhanced. This permits simplified configuration updates by adding or changing functional modules within a system.

The second category of life cycle costs is the operational support costs. These costs are often a large portion of the total LCC, however, they are seldom given the attention needed in the early stages of the design process. The evidence of this oversight is seen in the poor reliability and poor maintainability of the majority of deployed systems. Reliability is improved by using a proven modular packaging strategy and by instituting a strict quality assurance program to assure thermal and mechanical design adequacy. This cost savings attributed to more reliable equipment is realized by a reduction of costly maintenance actions and down time during the equipment life span.

Many avionics maintenance costs are reduced or even eliminated through the implementation of modular avionics packaging. The overall effect of maintenance at the module level is a considerable reduction in avionics support costs. This effect is greatly multiplied with the advent of high inter-system commonality of functional module hardware. Spares are purchased in large quantities for use in multiple systems taking advantage of the effects of competition and the economies of mass production. (Figure 5) The total number and cost of unique spare types to be inventoried is significantly reduced. This affects not only cost but perhaps even more crucial, increases the operational capability of the equipment. This type of maintenance approach

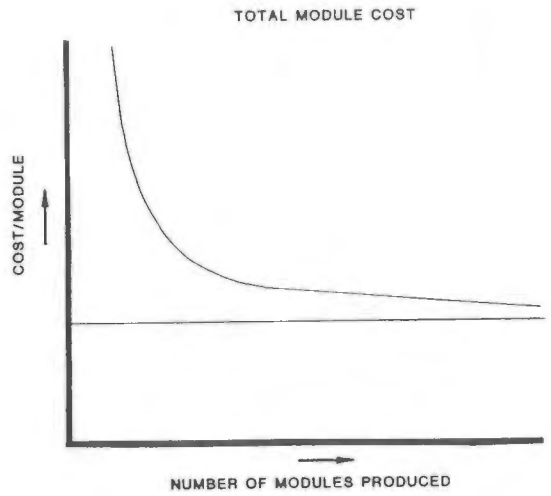


Figure 5

has also shown a reduction in the overall skill level of the maintenance personnel, thereby further reducing support costs. Another obvious benefit of this form of maintenance is a reduction in the complex, cumbersome, and extremely expensive test equipment now required to maintain today's avionics. By establishing new maintenance policies, isolating and replacing failed modules, and inventorying spares at the module level, much of the excessive operational support costs have been eliminated.

The opportunity for a reduction in avionics support costs through the use of modular packaging strategies is ripe for exploitation. Steps need to be taken, however, to revise maintenance policies, develop self-diagnostic avionics, establish modular interface standards, and continue to increase the reliability and reduce the burden of avionics support.

APPLICATION OF MAP

The Modular Avionics Packaging (MAP) Program provides a modular approach to avionics packaging at multiple levels. These levels are represented by the Standard Avionics Module, the Standard Enclosure (SE) and the Integrated Rack (IR). Avionics packaging design criteria have been developed to evaluate the level to which MAP should be applied. These criterion cover design areas such as weight and volume allocations, technology independence, logistics, operational environment, and life cycle cost impact. The modules are the foundation of the MAP approach and are the least common denominator across many unique systems. The standard avionics modules may be applied apart from the SE and IR, however, these avionics enclosures were developed specifically to provide the necessary interface between the modules and the airframe with known performance. These standard modular packaging methods are intended for common, generic, and widely used applications and must be properly applied to yield the anticipated benefits.

Documentation is in place in the form of military standards, specifications, and design data packages. The module formats are designed, qualified and sourced. The final results of the design, manufacture and testing of the SE are documented and available. A detailed design data package and a military specification for the family of standard enclosures will soon be ready for production or competitive procurement. A military specification for the IR is now in the final stages of coordination. Preliminary specifications, design data packages, and detailed thermal and environmental data are currently available for the SE and IR for initial system design and evaluation.

Through the use of military documentation and systematic evaluation of the packaging design, the MAP approach to packaging avionics can be effectively applied. The MAP Program is ready to meet the needs of current and future avionics system design and to assist in the development of modular packaging standards that will increase military aircraft operational effectiveness and reduce the avionics equipment life cycle costs

CONCLUSIONS

The benefits of modular packaging standardization have been proven in other areas of complex military electronics systems. Avionics packaging can apply similar packaging techniques, design practices, and maintenance policies that have in the past yielded increased reliability, low risk packaging design, improved logistics posture, technology independence through common functional modules, and realize an appreciable decrease in operational support costs. A 'business as usual' attitude in the design of avionics will yield small, incremental improvements in aircraft readiness and expense. Emerging technologies provide an opportunity for significant increases in operational effectiveness. However, new policies are needed to design, build and maintain avionics systems that address logistics factors as well as performance. A blending of advanced integration techniques and modular interface standardization must be utilized to capitalize on the benefits of modular avionics packaging.

84-2748

GENERAL DYNAMICS CONVAIR DIVISION TOTALLY RECONFIGURABLE EMBEDDED COMPUTER

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Abstract

Modern avionics platforms require data processing systems that are extensible, maintainable, and affordable. A general purpose embedded computer system is being developed for cruise missile and launch vehicle avionics applications. Major development objectives include implementation of DoD embedded computer standards, a functionally flexible and modular design, and a producible system that is maintainable, reliable, and cost effective. The hardware elements are described along with the details of their functional interfaces and the overall system architecture. An integration and maintenance support system is described. Software support and the implementation philosophy are also discussed.

Introduction

Major DoD and NASA programs continue to provide the aerospace industry with new challenges in avionics system design and implementation. Modern weapon and space vehicles require avionics systems that provide the vehicle with greater autonomy, permit the vehicle to be adapted to new missions, and allow the vehicle to operate under a multitude of environmental conditions. A major element of such avionics systems is the "embedded class," general purpose digital computer.

Today's avionics applications require embedded computer systems that exhibit performance characteristics and capabilities that rival state-of-the-art minicomputers while simultaneously conforming to traditional avionics platform constraints. In addition, major DoD weapon systems (e.g., cruise missile) that involve large numbers of vehicles characteristically require embedded computer systems that are reasonably affordable, highly maintainable, and capable of being upgraded or enhanced to meet new mission requirements or to extend the weapon's effective lifetime (1).

The Totally Reconfigurable Embedded Computer (TREC) project is an ongoing effort aimed at developing an embedded system capable of satisfying the general purpose computer requirements of modern weapon system avionics platforms, partcularly those of the cruise missile. The major objectives of the TREC development effort include:

1. Conformance to the physical contraints typical of cruise missile applications.
   - — Weight and volume dimension
   - — Power consumption
   - — Environmental conditions
2. Compliance with DoD embedded computer standards to enhance maintainability, enhance supportability, and reduce life cycle cost.
   - — MIL-STD-1750A: Instruction set architecture standard
   - — MIL-STD-1553B: Interface standard
   - — MIL-STD-1589B: JOVIAL high-order language standard
   - — MIL-STD-1815A: Ada® high-order language standard
3. Achievement of a high degree of system flexibility and modularity to allow the computer's capability to be tailored to the application.
   - — Memory capacity and types (i.e., RAM, PROM, etc.)
   - — Processing throughput
   - — Number of I/O channels
   - — Operating system memory requirements

The TREC system is designed around the Fairchild F9450 microprocessor chip set, which implements the MIL-STD-1750A instruction set architecture (2). The computer hardware architecture is defined in terms of five logical subsystems:

1. Master processor subsystem
2. Slave processor subsystem

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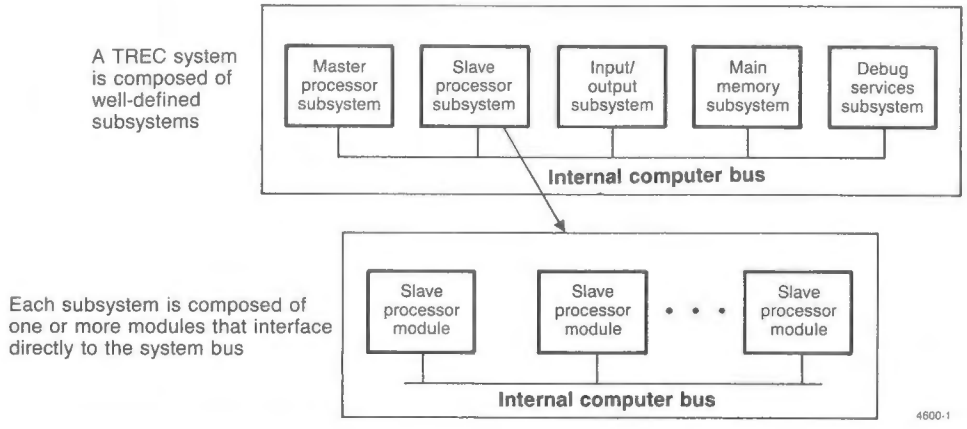

Figure 1. TREC's bus-oriented design enhances functional modularity.

3. Main memory subsystem
4. Input/output subsystem
5. Debug services subsystem

As shown in Figure 1, each subsystem consists of one or more hardware logic modules. A hardware module is a collection of logic, which performs some well-defined function and occupies a single "position" on the Internal Computer Bus (ICB). The ICB is a parallel signal highway containing an address/data bus, bus mastership handshake signals, interrupt request signals, and various special purpose control and status signals.

The first four subsystems listed above make up the operational TREC system. The extent of the slave processor, main memory, and I/O subsystems is application-dependent. For example, a minimal application may require only a few kilowords of main memory, a single I/O channel, and no slave processors,while a maximum application may require a few hundred kilowords of main memory, dozens of I/O channels, and several slave processors. Configuring a TREC hardware system is accomplished by "plugging" the appropriate hardware modules into the ICB.

The principle element of the debug services subsystem consists of an interface between the ICB and the Debug Monitor Loader (DML) system. The DML system consists of a firmware-controlled "black box" interfaced to a commercial minicomputer. The DML system permits a user to upload and download TREC memory, control the operation of the TREC processor(s), determine the health of the system, and perform debug and monitor operations.

TREC system and support software efforts are aimed at permitting application software to be developed in the JOVIAL HOL for the near term with support for the Ada HOL to follow. Assembly language programming support is in place and is used extensively in the development of TREC system software and stand-alone hardware diagnostic programs.

Hardware Description

Internal Computer Bus

The backbone of the TREC system is the Internal Computer Bus (ICB). The ICB is a parallel communications highway that provide the electrical interface between the hardware modules that compose a TREC system. By definition, a hardware module interfaces to the individual bus lines through single-signal conductor paths. From a bus viewpoint, a hardware module is defined in terms of maximum bus line loading and minimum bus line drive capability.

The ICB contains a 20-bit address bus and a 16-bit data bus. Address control signals permit each 20-bit address to be qualified as either an instruction memory address, a data memory address, or a Control/Status Register (CSR) address. (Note: in keeping with the 1750A XI0 command structure, only the lower fifteen address lines are meaningful when a CSR address is placed on the bus.) Therefore, a ICB bus master may address up to one megaword of instruction memory, one megaword of data memory, and 32,768 CSR addresses. Bus slaves are required to activate an address status signal upon decoding an address that they recognize. This indicates whether or not an address, placed on the bus, by a bus master, is "valid." The master processor subsystem monitors the "valid address" status signal and raises an error flag if an invalid address is placed on the bus by any bus master.

Data transfers between bus masters and slaves (e.g., the master processor and a memory module) is accomplished via the 16-bit data bus. A data bus status signal is provided to permit bus slaves to indicate when they are ready to move data to/from the data bus. The data bus will therefore accommodate bus slaves of various different reaction times. Dual data strobe signals are provided to permit eight-bit data transfers to be performed. One data strobe signal controls the movement of data on the lower eight lines and the other controls the movement of data on the upper eight lines. Sixteen-bit transfers are accomplished by the simultaneous control of both data strobe signals.

Mastership of the ICB is controlled through a dual set of bus request/grant daisy chains. Bus master priority is determined by combining the request/grant chain that the bus master resides on and its relative physical position within the chain. A bus request on the higher priority level will preempt any bus master that has gained bus control via the lower level. The ICB supports this mechanism by providing a special control signal, which when activated forces any low-priority-level bus master to relinquish bus control.

Other ICB signals include:

- Four prioritized interrupt request lines through which I/O channels may generate interrupt requests to the master processor. Each request line supports multiple I/O channels via the "wired-or" concept. Channel priority within a level is software determined as the interrupt acknowledge mechanism is software controlled.
- A single interrupt request line is provided to permit slave processors to generate interrupt requests to the master processor. Like the I/O interrupt lines, the slave processor interrupt request line supports multiple slave processors.
- Three fault indicator lines that permit modules of the main memory, slave processor, and I/O subsystems to signal the master processor that an error condition exists.
- Two bus clock signals that permit modules to synchronize actions and events.

Various other signal lines are provided to accommodate elements of the debug services subsystem and the system power supply.

Master Processor Subsystem

The master processor subsystem is the central controlling element within the TREC hardware suite. It is designed around the MIL-STD-1750A compliant Fairchild chip set. The F9451 MMU is used in conjunction with the F9450 CPU to provide the master processor with the full addressing capability of the ISA standard. The master processor (under control of the appropriate software) controls the actions of all other TREC hardware modules, resides as the primary bus master, and is the principle manager of events on the internal computer bus.

Within the master processor subsystem, the F9450-F9451 combination provides:

- The instruction execution unit
- 1750A TIMER A
- 1750A TIMER B
- The complete set of 1750A page registers
- The 1750A fault register
- The 1750A interrupt recognition mechanism

Additional master processor elements include:

- A programmable 32-bit mission timer
- Generation of the system clocks
- Bus master arbitration
- A secondary bus master watchdog timer
- A data transaction watchdog timer
- An auxiliary fault register
- Logic to support software-controlled built-in-test

The 32-bit mission timer is fully programmable and includes a corresponding 32-bit alarm register. The timer tick rate is programmable to a maximum frequency of one tick per microsecond. The alarm register is software settable and, when enabled, will generate an interrupt request to the master processor CPU when the timer value matches that of the alarm register.

The master processor subsystem includes the circuits necessary to generate the system clock signals. The clock signals include a high-frequency clock used for the timing of events on the ICB and a one-megahertz fixed-frequency clock for general use by the system modules. Both clock signals are bussed within the ICB.

Bus arbitration is controlled by circuitry within the master processor. The arbiter accepts requests for bus mastership through the two bus request lines of the ICB. Bus requesters using the high priority bus request level have precedence over requesters using the lower priority level. If the arbiter receives a bus request on the high-priority level, any active lower level bus master is forced to relinquish bus mastership and the higher priority requester is granted use of the bus. Preemption is accomplished via a "bus release" signal within the ICB. The bus grant signals are daisy chained so that within a level, the priority of the requester is determined by its position within the bus grant daisy chain.

Bus requests can be inhibited from reaching the arbiter at the discretion of controlling software. This is accomplished via the 1750A defined DMA enable/disable discrete. In addition to this mechanism, the master processor contains a watchdog timer, which permits bus masters other than the master processor to maintain bus control for a maximum period of approximately one millisecond. If this time interval is exceeded, the watchdog timer will activate the "bus release" signal on the ICB and force the current bus master to relinquish control of the bus.

The master processor contains a second watchdog timer for monitoring the length of data bus transactions. If a bus slave forces any bus master into a prolonged "wait state," the watchdog timer will timeout and automatically generate the "data ready" ICB status signal referred to earlier. This causes the bus master to complete (i.e., abort) the data transfer transaction.

The master processor subsystem contains the logic necessary for recording various system-level fault conditions. The basic elements include the 1750A defined fault register contained within the F9450 and an auxiliary fault register external to the CPU. The CPU's fault register operates as defined by the 1750A standard. The ICB I/O channel fault and memory fault signals are interfaced directly to the main fault register. The previously discussed invalid address fault is also recorded directly by the main fault register.

The auxiliary fault register records the occurence of timeouts in the two watchdog timers. It also monitors the ICB slave processor fault signal. The occurrence of any of these fault conditions will set a corresponding bit within the auxiliary fault register. The setting of any auxiliary fault register bit causes a bit in the main fault register to be set. The 1750A defined "machine error interrupt" is generated by the setting of any bit within the main fault register, thereby permitting the master processor CPU to take the appropriate action upon the occurrence of any fault condition. To ensure the timely handling of faults, the ICB "bus release" signal is automatically activated by the occurrence of any major fault condition. This allows the CPU to gain and maintain mastership of the ICB immediately following fault detection.

The master processor contains additional logic to permit software to test the integrity of various subsystem elements. Examples include circuitry permitting the software to test the bus arbiter and the bus master watchdog timer.

Slave Processor Subsystem

The slave processor subsystem consists of the entire collection of slave processors. A TREC system may contain one- or multiple-slave processors or none. Each slave processor is functionally identical. Slave processors differ only in memory configuration and the ICB addresses at which their memory and CSR devices reside. Each slave processor is an independent data processor consisting of a CPU (F9450), memory, and a well-defined functional interface to the remainder of the system.

The central element of a slave processor is the F9450 CPU. Each slave processor may contain up to 64K words of instructional memory and 64K words of data memory. The data memory array is dual-ported permitting full-time access by both the slave processor CPU and any ICB bus master; i.e., the master processor CPU or an I/O channel DMA device. A slave's instruction memory is electrically isolated from the ICB while the slave CPU is executing instructions. Access to this memory array by ICB bus masters can only be accomplished after a formal request for access is made to the slave by the master processor. Upon granting access, the slave CPU becomes inactive and the instruction memory array becomes electrically "attached" to the ICB. During this time, the slave's instruction memory is addressable on the ICB within the ICB (i.e., master processor's) instruction memory address space. When the access request is removed, the slave's instruction memory "disappears" from ICB view. This mechanism permits a slave's normally private instruction memory to be downloaded (or read) with data received through a TREC I/O channel. When downloading is complete and ICB access is relinquished, the slave CPU can fetch its instruction stream without competing with other devices for memory access.

A slave's data memory is fully accessible by both the slave CPU and ICB bus masters. Accesses to this memory are arbitrated on a per-memory-cycle basis. A "collision" simply introduces "wait states" into the latecomer's memory cycle. This "dual port" nature causes a slave's data memory array to be continuously addressable on the ICB within the ICB (master processor's) data memory address space.

The functional interface between a slave processor and the master processor subsystem is supported by a group of control and status registers residing within the CSR address space of the ICB (master processor). This register set is augmented by the ICB "slave processor interrupt" signal. The control and status registers permit the master processor (under control of the appropriate software) to control and monitor the state of the slave as well as generate interrupts to the slave CPU. Conversely, a combination of status registers and the "slave processor interrupt" signal permit a slave to interrupt the master CPU as well as identify the nature of the interrupt request.

The functional interface also supports the Debug Monitor Loader system. Support includes a programmable breakpoint controller that monitors address cycles made to the slave's instruction memory array. When enabled, the breakpoint controller will interrupt slave CPU execution when a match between the programmable breakpoint condition register and the slave instruction memory address bus occurs. This permits a DML system user to single-step a slave CPU or cause the CPU to run to a specified instruction address breakpoint.

Main Memory and I/O Subsystems

The main memory and I/O subsystems comprise the remainder of the operational TREC system. The main memory subsystem consists of the memory modules used to populate the memory address spaces of the master processor. Module designs include a 256K-word RAM/PROM/EEPROM module and an error detecting-correcting (EDC) RAM module. The 256K-word module permits memory of any of the three types to be allocated to either the instruction or data memory spaces in increments of 8K word blocks. The EDC module will detect a single- and double-bit errors and correct single-bit errors. Detection of an uncorrectable error is reported to the master processor through the ICB "memory fault" signal.

The I/O subsystem consists of the collection of modules containing I/O channels. Each I/O module interfaces directly to the internal computer bus and is controlled by the master processor subsystem. Input/output

channels are defined as either "DMA-type" or "memory window-type" depending upon how their I/O data is buffered. DMA-type channels contain ICB bus masters capable of taking control of the internal computer bus for the purpose of transferring data to/from ICB data space memory. Since the data memory of all TREC processors (master and slaves) is addressable on the ICB, a DMA-type I/O channel can move I/O data directly to or from its absolute location in TREC memory. Window-type I/O channels buffer their I/O data in I/O module resident memory arrays whose addresses are mapped into the ICB (master processor's) data memory address space. Input/output channels of this type do not compete for mastership of the ICB; therefore, they do not consume bus bandwidth.

All I/O channels contain a well-defined functional and electrical interface to the internal computer bus. In addition, all I/O modules contain a number of control and status registers, addressable in the ICB CSR address space, which permits the master processor software to control and monitor the operation of the module's I/O channels. The functional interface between I/O channels and the master processor has been standardized some what across all I/O module designs to provide a significant level of commonality among software I/O driver routines.

System Architecture

The TREC system is designed to function in both stand-alone and federated computing system environments such as the one depicted in Figure 2. Support for the stand-alone environment is characterized by the TREC's ability to contain multiple processor elements, a large amount of memory, and a significant number of I/O channels. As a result, missile avionics platforms may employ the TREC as the sole general purpose data processor, without giving up the ability to support future growth. As new sensor and reaction devices are integrated into the avionics platform, the TREC's memory, throughput, and I/O capability can be expanded to accommodate the new devices and their associated control software and mission algorithms.

The TREC system may be integrated into federated computing environments that are based upon the commonly used 1553B interface standard. The TREC's 1553 bus interface module is an intelligent design, which can be software configured to operate as a bus controller, a remote terminal, or a bus monitor. In addition, the interface module will support a number of distinct 1553 protocols. As in a stand-alone application, the ability to tailor the TREC's capability permits individual network nodes to be optimized to the local environment and the computing requirements of the particular node (Figure 3).

System Topology

The TREC system can best be described as a variable-number nonhomogeneous multiprocessor system. The advantages associated with this type of multiprocessor architecture are listed below:

- Bus bandwidth saturation does not occur as additional processors are added to the system.

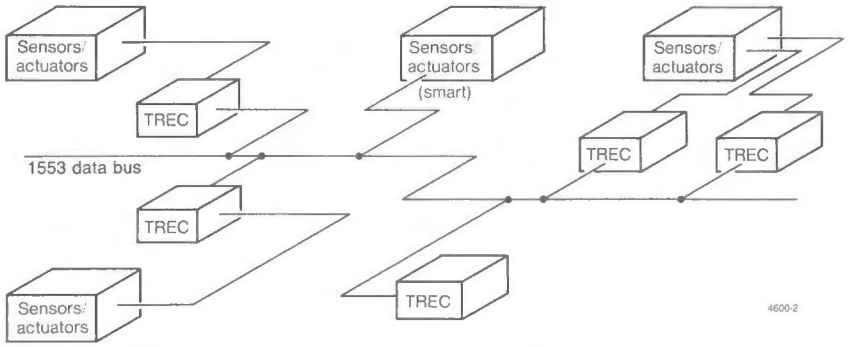

Figure 2. TREC may be tailored to either stand-alone or federated computing system environments.

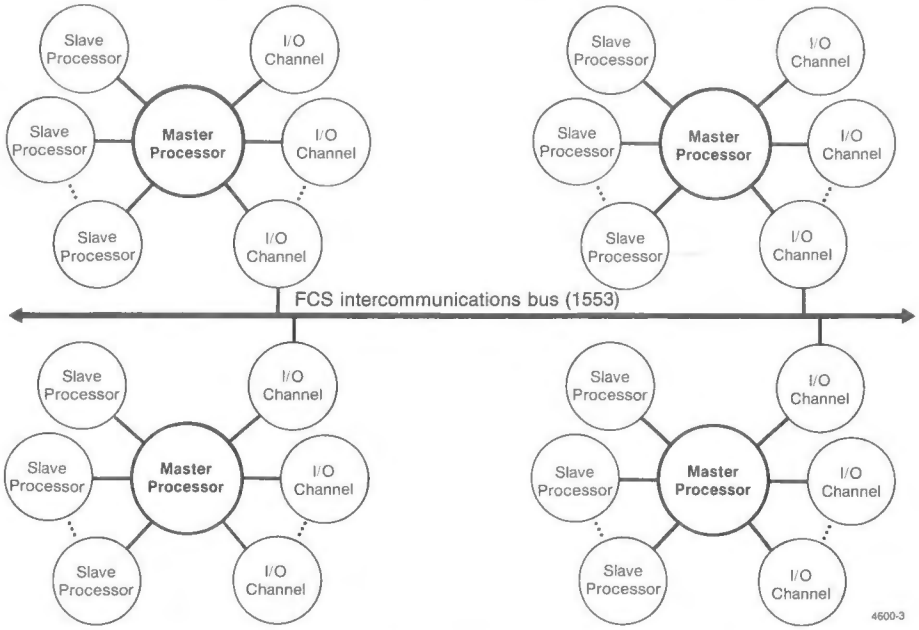

Figure 3. TREC supports the design of powerful, yet optimized, federated systems.

- Additional processors may be added to an existing system with minimal hardware and system software impact.
- Uniprocessor software support tools (e.g., compilers) may be utilized if necessary.
- Software duty cycles are highly deterministic; i.e., the amount of real time required for a particular code sequence to execute is nearly a constant.

The major disadvantage of a nonhomogeneous multiprocessor architecture is that it does not support internal fault tolerance techniques as readily or as completely as does a homogeneous multiprocessor system.

As depicted in Figure 4, the TREC system is a strictly nonhomogeneous architecture with the master processor subsystem uniquely occupying a centralized position.

- Control of all I/O channels is performed by the master processor.
- Only DMA-type I/O channels compete with the master processor for mastership of the internal computer bus.
- All I/O channel interrupts and faults are serviced by the master processor.
- All system memory elements, whether residing in main memory, on an I/O module, or a slave processor module, are addressable by the master processor.

I/O Data Transfers

Under control of the master processor, DMA-type I/O channels may be programmed to transfer their data to or from either the main memory array or the data memory array of any slave processor. This permits real-time data to be transferred directly into or out of the data memory of that processor element on which the algorithm associated with the data is executing.

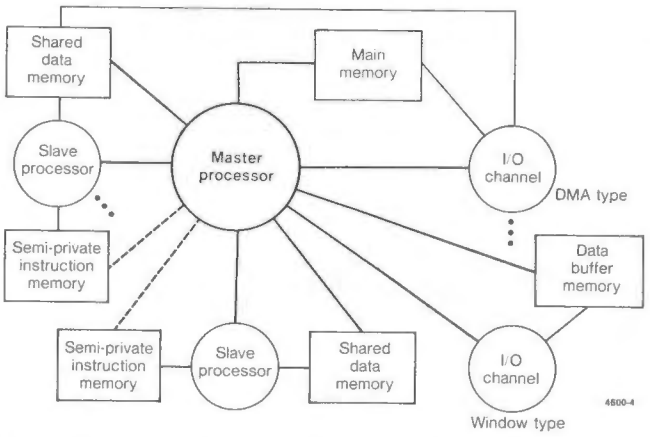

Figure 4. Although a highly nonhomogeneous multiprocessor master, TREC is designed to simplify data flow.

Window-type I/O channels require the services of the master processor in the physical movement of data between the system processors and the I/O channel. The window-type design is preferred for I/O channels characterized by low frequency, low volume data-rates since its implementation is typically not as complex as a DMA-type channel design.

Interprocessor Communication

The slave processors ability to interrupt the master, and vice versa, coupled with the fact that each slave shares access to its data memory array with the master processor, provides the basis for interprocessor communication. The master and each slave must run under the control of its own local executive. No processor element can execute the instructions of another during normal operation. The instructions executing on the master and those executing on any slave can, however, communicate directly through memory. The ability to reference common data objects facilitates the use of traditional "test-and-set" instructions and memory-based semaphores for master-slave process synchronization and provides a simple method of passing data values between processes executing on the master and a slave. In addition to simply sharing access to memory, the TREC system has been designed to permit slave software to generate master processor hardware interrupts. Conversely, master processor software can generate interrupts within any slave. It is through this mechanism that the master processor facilitates interprocessor communication between slaves as well as the propagation of I/O completion interrupts to a slave processor that is sending or receiving data through a system I/O channel.

Debug Monitor Loader System

The Debug Monitor Loader (DML) system, as shown in Figure 5, is a collection of specialized hardware and software elements providing a powerful console interface to the TREC system. The principle elements of the DML system include a commercial UNIX-based minicomputer, a microprocessor-based service module, and the software elements that control the minicomputer and service module.

The minicomputer is a Tektronix 8560 software development system. Hosting the UNIX operating system, the 8560 provides a programmer's environment with all the standard UNIX utilities as well as an assembler and linker for developing 1750A object code. A utility developed in house, referred to as the DML supervisor, runs under the UNIX operating system and controls the 8560 during a DML session. The supervisor controls the user console that provides the DML command menus and information displays. User commands are communicated to the service module to initiate a DML function and the resulting information obtained from the service module is formatted for

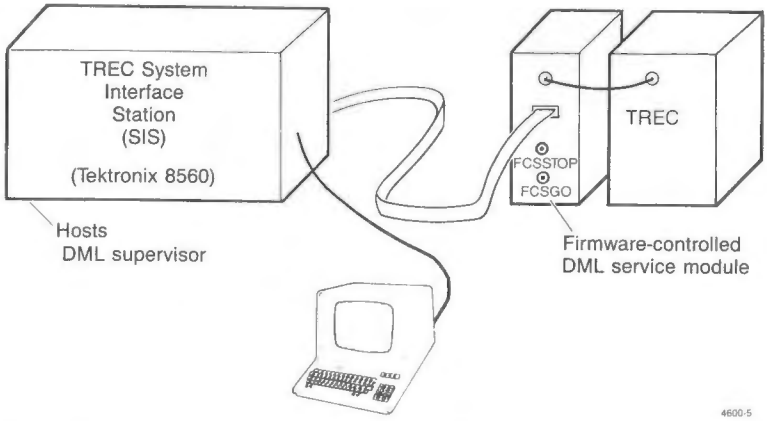

Figure 5. The Debug Monitor Loader (DML) system places sophisticated debug capabilities at the user's fingertips.

display on the user's console terminal. An operational session logging capability is made available by the supervisor. When this option is selected, the supervisor creates a disk file of all user command selections and their resulting information displays.

The DML supervisor communicates with the service module over a standard RS232 interface. The service module controls and communicates information to and from the TREC through a direct interface to the internal computer bus. The interface to the ICB permits the service module microprocessor to control and monitor the state of ICB signals as well as take control of the ICB's address-data bus. In addition, the interface permits the TREC's master processor to access a block of memory residing within the service module. This block of memory is used to pass commands and internal master processor CPU register information between the master processor and the DML system. The memory block appears to the master processor as a group of register elements addressable in the CSR address space; i.e., accessible via 1750A XI0 commands. Connecting the DML system to any TREC configuration simply causes a predefined set of CSR space elements to appear as valid addresses on the ICB. There are no dependencies on TREC memory configuration or useage.

Support for the DML system is built into the master processor's powerup firmware. The firmware detects the presence of the system by attempting to access the service module's memory block located in the master processor's CSR address space. An invalid address error signals the absence of the DML system and CPU execution is transferred to a predefined "start" address. If the DML system is present, CPU execution is transferred to the DML support routines contained in the powerup firmware.

The DML service module consists of microprocessor and various support devices, memory, a serial I/O interface for connecton to the minicomputer, dual ICB breakpoint controllers, and the logic necessary to interface the module to the TREC's internal computer bus. The service module is firmware-controlled giving it the character of an intelligent "black box."

The service module accepts commands from the supervisor program and returns any response information associated with those commands. Nearly all DML commands are carried out directly by the service module without any involvement on the part of the TREC processors. The only exceptions are the commands to start and stop the TREC processor execution. These commands are signaled by specially defined interrupt levels within the master processor and slave processor. Command information and internal register contents are passed to the master processor through the previously described shared memory block located within the service module. Communication with and the control of a slave processor is accomplished through the slave's set of control and status registers. This is made possible by the service module microprocessor's ability to take control of the TREC's internal computer bus. As with the master processor, each slave processor contains DML support routines within its powerup firmware.

The DML system permits the user to load TREC memory, monitor system operations and events, and perform a multitude of debug operations. A few of the available DML operations are listed below.

- Determine system resources (amount of memory, number of slaves, etc.).
- Test the integrity of random access memory.
- Emulate I/O and slave processor subsystem interrupts and faults.
- Set master processor breakpoints (breakpoints can be set to occur on almost any ICB event).
- Single-step the master processor.
- Single-step a selected slave processor.
- Set a slave processor breakpoint and command the slave to run stand-alone.
- Examine and alter the master processor CPU registers.
- Examine and alter a slave processor CPU's registers.

In addition to performing commanded operations, the DML system automatically reports the occurrence of certain system-level events indicated by the activation of various internal computer bus signals (e.g., power fail, slave processor subsystem fault, etc.).

The DML system also supports the debugging of TREC systems residing within federated computing arrangements. As shown in Figure 6, the service modules controlling each TREC can be chained together permitting the user to simultaneously start or stop a group of TREC systems. For example, an entire group of TREC systems can be caused to stop execution upon one of them reaching a breakpoint condition.

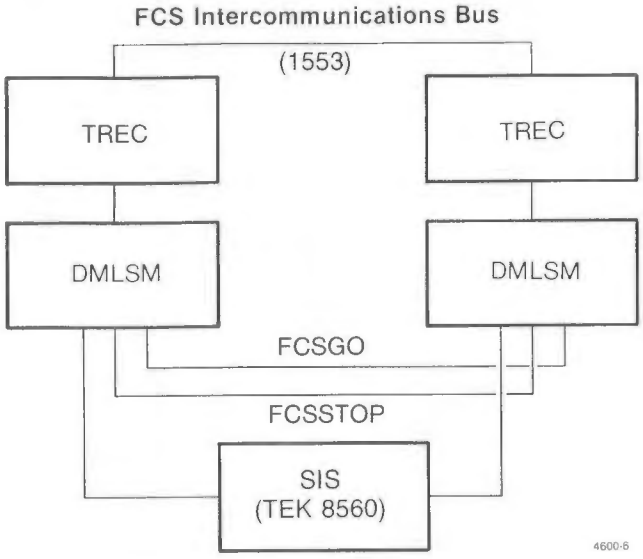

Figure 6. DML supports the Federated Computing System (FCS).

System and Support Software

Today's missile avionics software is being developed in the JOVIAL high-order language and tomorrow's will be developed in Ada. Therefore, development of the TREC system and support software is a two-phased effort. The first phase addresses the operating system and programmer tools necessary to support the JOVIAL J73 language. The support software elements include the ECSPO JOVIAL -1750A tool set and an inhouse-developed software simulation of the TREC system. A JOVIAL-compatible real-time multitasking operating system has been developed to support uniprocessor TREC configurations. The operating system has been designed to permit it to be easily extended to support TREC configurations containing slave processors.

The longer range goal is to permit multiprocessor TREC configurations to be programmed using the Ada high-order language. Much analysis and development work remains to be done before a programmer can sit down and develop critical mission software in Ada. Mapping the Ada tasking model and exception concept onto a multiprocessor system is a complex problem, which places significant impact on the design of a suitable compiler and the system software (3).

Conclusions

The TREC system is targetted for real and predicted environments typical of cruise missile and launch vehicle applications. These environments are characterized by ionizing radiation, EMI, EMP, and stringent constraints on maximum power consumption, size, weight, and heat dissipation. While being able to survive in such an environment, the candidate embedded system must also be affordable and maintainable.

Design philosophies commensurate with one group of these requirements often directly clash with the philosophies of another. The selection of electronic components typifies the problem facing the hardware designer. For example, use of high-production-volume VLSI circuits can lead to significant reductions in overall system cost, volume, and power requirements due to the amount of logic contained on such highly integrated devices. But as is often the case, many of these devices exhibit insufficient radiation tolerance and a high susceptability to EMP (4). On the other hand, custom IC designs are usually too expensive and tend to make system maintenance more difficult.

The design and implementation philosophy adopted in the development of the TREC system is one based on compromise. For example, extensive use of off-the-shelf electronic components has aided in producing a design that is reasonably affordable and maintainable. On the other hand, semiconductor technologies exhibiting low-radiation tolerance were generally avoided.

The TREC hardware modules are packaged on 5- × 7.5-inch printed circuit cards that plug directly into the internal computer bus backplane of a conduction cooled enclosure (Figure 7).

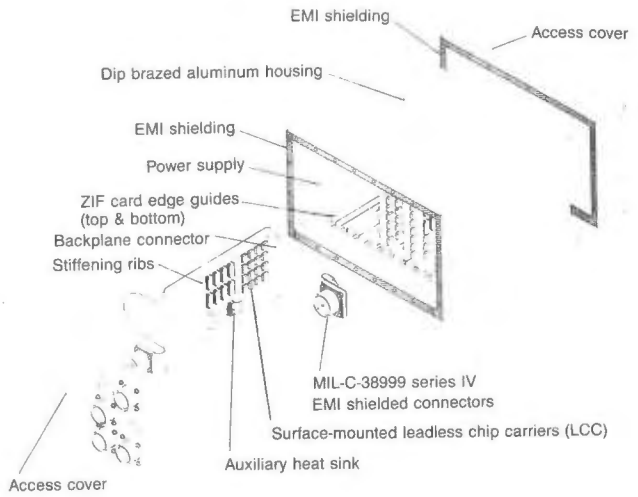

Figure 7. TREC is packaged for the avionics environment.

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(3) P.K. Rowe, "Microprocessor Interprocess Communication Using Ada, Monitors, and VME," Proceedings of the 4th AIAA Computers in Aerospace Conference, pp. 331-339: Oct., 1983.

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SESSION 25 DIGITAL PROPULSION CONTROL AND MONITORING SYSTEMS

Chairmen:

John C. Richards
General Electric Co.

Paul Adams
AFWAL/POTC

This session focuses on the equipment and techniques employed to meet the challenges faced by digital engine monitoring systems, including detection and isolation of sensor failures and operational experience with current systems.

"ACCURACIES OF DIGITAL ENGINE MONITORING PROVEN BY PERFORMANCE"

84-2753

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Abstract

The capabilities of digital electronics and microprocessor based systems have permitted the development of engine parameter measurements for gas path analysis that was not previously achieved. The certification program for the JT9D-7R4G2 engine provided the opportunity to evaluate the performance of one specific design against the sophisticated flight test instrumentation required for that exacting task. The concept to be described 1) employs highly accurate sensors, 2) is microprocessor controlled, and 3) converts raw data directly to a digital format. In all aspects, the design that was evaluated exceeded the objectives of the development team. The strengths of the technology employed are its accuracy and repeatability. The system has entered airline service and it is projected that the performance to be experienced will permit an improvement in the general accomplishments of engine condition monitoring.

Nomenclature

AIDS	Aircraft Integrated Data Systems
ARINC	Aeronautical Radio Incorporated
CIA	Communications Interface Adapter
CPU	Central Processor Unit
EAROM	Electrically Alterable Read Only Memory
EGT	Exhaust Gas Temperature
EPR	Engine Pressure Ratio (PT7/PT2)
ESN	Engine Serial Number
FIFO	First-In First-Out
LIFO	Last-In First-Out
MDAC	Multiplying Digital to Analog Converter
N1	Low Pressure Compressor Rotor Speed
N2	High Pressure Compressor Rotor Speed
PMUX	Propulsion Multiplexer
PROM	Programmable Read Only Memory
PS4	High Pressure Compressor Discharge Pressure
PT2	Engine Inlet Pressure
PT3	Low Pressure Compressor Discharge Pressure
PT7	Low Pressure Turbine Discharge Pressure
PWB	Printed Wiring Board
RAM	Random Access Memory
RSS	Root Sum Squared
SVA	Stator Vane Angle
TT3	Low Pressure Compressor Discharge Temp.
TT4	High Pressure Compressor Discharge Temp.
WF	Fuel Flow

Introduction

The ability to monitor the operating condition of a modern turbine engine has been greatly enhanced by the evolution of digital electronic systems. One of the advantages that can be offered by a digital system configured to measure the performance of an aircraft engine is that gradual changes to critical parameters can be continuously monitored. This monitoring feature permits an effective evaluation of all the engines in a fleet and can help to establish an optimum plan for the maintenance of engines. Minor flaws can be corrected before some extensive damage occurs, worn modules can be replaced and failures can be diagnosed. Trends and recent performance changes provide data well in advance of a mandatory engine change.

Several approaches for gathering data have been taken; one of these is the Aircraft Integrated Data System (AIDS) which is well over a decade old(1). Early systems did a creditable job in providing data that could be analyzed on a fleet wide base. The noise content on sensitive signals limited the effectivity of this system.

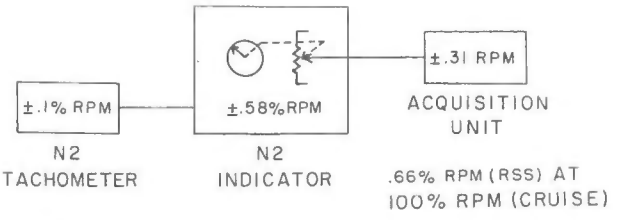
With the growth of gas path analysis, there came a need for more accurate pressure information. As these systems became more complete, their weight became significant, with the weight of airframe cables being a major contributor.

The availability of the microprocessor made possible many improvements in the system approach for turbine engine monitoring. Signal accuracies for engine pressures, turbine speeds, temperatures and geometry positions could be addressed on a system basis. The PMUX (Propulsion Multiplexer) unit can be defined as the combination of 1) engine monitoring needs and 2) electronic technology capability.

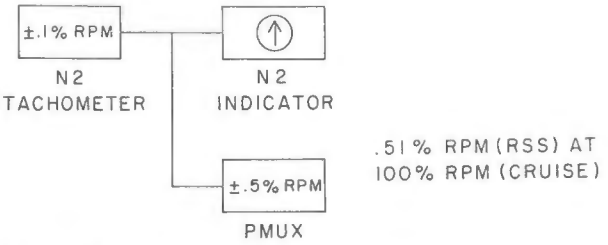
Before the advent of PMUX, engine monitoring signals were acquired by one of three methods: 1) Tapping into existing aircraft systems; 2) Providing a buffered output from an existing aircraft system and 3) installing a dedicated monitor signal source.

Tapping an existing signal is the most economical approach and is practical if accuracy and isolation requirements are met. Typical analog to digital conversion errors are between .25% and .5% of full scale and can be up to 2% of full scale for non standard signals. Two approaches of each method listed above were taken on the 747 to provide standardized outputs from aircraft systems. Figure 1 depicts an output from an engine indicator. Typical end-to-end cruise accuracy is .66% RPM (RSS) at a cruise setting of 100% RPM. The accuracy achievement of PMUX is .25% RPM at a cruise setting of 100% RPM.

*AIAA Member



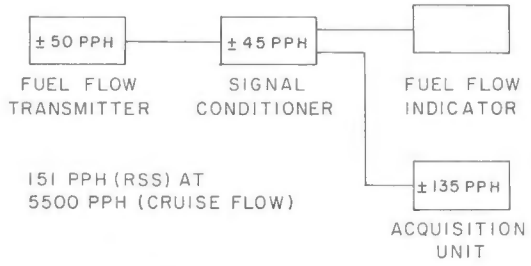
a. Tapping In



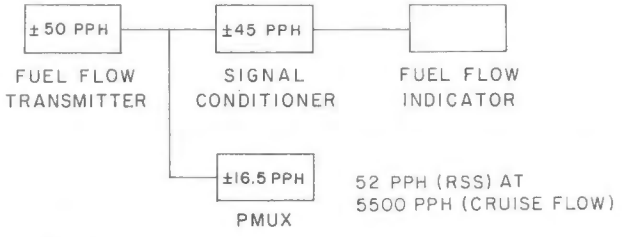
b. PMUX

Figure 1 Tapping Into an Existing System Versus PMUX

Figure 2 illustrates an AIDS engine output from a signal conditioner having a buffered output. Typical end-to-end accuracy at cruise conditions has been 151 PPH (RSS) at a fuel flow of 5500 PPH. Accuracy with PMUX is 52 PPH (RSS). Figure 3 illustrates a dedicated signal pickup of PS4 pressure. Prior to PMUX, the accuracy was 5.6 psi; with PMUX, the accuracy will be better than .75 psi at a cruise pressure of 150 psia.



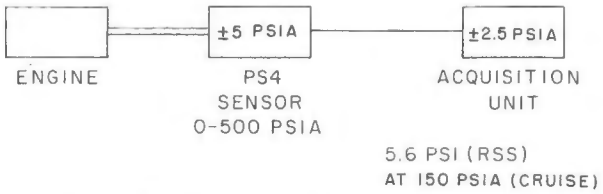
a. Buffered Output



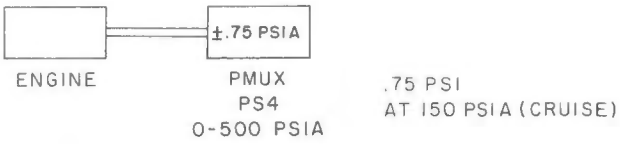
b. PMUX

Figure 2 Existing Aircraft System Buffered Output Versus PMUX

Design theory confirmed that improved requirements could be met, but the opportunity to evaluate the implementation of this theory required something like the certification of an engine when extensive flight performance could be compared to the high integrity of flight test instrumentation. The certification of the JT9D-7R4G2 engine on the 747-300 provided this opportunity.



a. Dedicated AIDS Signal Source



b. PMUX

Figure 3 Dedicated AIDS Signal Source Versus PMUX

PMUX Performance

General

The PMUX concept enjoys several advantages. It permits the direct digitizing of some signals at a location near the sensor; bypassing the previous need to accept cockpit data that was derived for crew observation. The weight of the PMUX installation is less than that of previous configurations. In the 747-300 aircraft, the PMUX installation amounted to a weight savings of over 100 pounds. This savings is attributable to a reduction in aircraft wires.

PMUX took advantage of both its location and its microprocessor base to employ a pressure sensor concept that has both the accuracy and the stability required to perform "gas path analysis." The accuracy continues day after day throughout the full temperature range of the engine location.

Past pressure sensors had an accuracy of 2-3%. For gas path analysis, an accuracy of 1% of point or better is required. The PMUX unit provides an accuracy from gas pressure to its digital data output that is better than the nominal 0.5% of point design objective. Experience to date shows a performance that is better than 0.25% of point. This will be a major improvement in the analysis associated with engine monitoring. Trend analysis requires stable performance of the pressure sensors in order that gradual changes in engine operation can be monitored.

The performance of the PMUX pressure sensors is comparable to the high precision pressure sensors that are used in engine certification. To perform engine certification, very precise sensors are located in a temperature controlled environment to maintain short term accuracy. For long term accuracy, test sensors are calibrated three or four times a week to assure accurate data during the key periods of the flight test program. In comparison, the PMUX sensors were calibrated during their production process, were installed in the severe environment of the engine strut, and never required recalibration.

Engine Certification flight testing was performed by recording data on engine pairs, two engines being used as test engines while the other two engines maintained the required aircraft flight conditions. Certification of the JT9D-7R4G2 engine was performed with the inboard engines paired and then the outboards paired. Basic engine certification involves data gathering at various engine power settings during steady state and transient operation throughout the flight envelope of the aircraft. In the accumulation of this data, six parameters on each of the four engines were acquired only through the PMUX unit (a choice that displays the confidence that has been shown for this component). In addition to these, seven signals were primarily gathered by flight test instrumentation but were also measured simultaneously by PMUX in order to obtain a calibration of the PMUX data.

Comparison measurements:	Independent measurement
Engine Inlet Pressure (PT2)	Stator Angle
LPT Discharge Pressure (PT7)	3.0 Bleed Position
Fuel Flow	LPC Discharge Pressure (PT3)
Engine Pressure Ratio (EPR)	LPC Discharge Temperature (TT3)
High pressure Rotor Speed (N2)	HPC Discharge Pressure (PS4)
Exhaust Gas Temperature (EGT)	HPC Discharge Temperature (TT4)
Low Pressure Rotor Speed (N1)	Discrete Engine Data

Table 1. Signals Monitored

The engine certification process includes the accumulation of steady state data to define and demonstrate engine performance for compliance with Federal Aviation Regulations. Calculation of flight test fuel flows are based on very accurate calibrations of flight test engine fuel flowmeters and density corrections derived from fuel temperatures and pressures measured at each flowmeter. It should be noted that the flight test fuel flow instrumentation was special while the PMUX unit operated with the production sensor. This can account for some difference in performance.

Besides providing better accuracy, PMUX also provides more capability. Measurements to date show (see Table 2) that the PMUX unit exceeds its accuracy requirements.

Signal	Required Accuracy	Achieved Accuracy
Speeds	0.5% PT	0.25% PT
Fuel Flow	0.6% PT	0.31% PT
Pressure	0.5% PT	0.25% PT
EGT	3.8 C	2.8 C
Temperatures (others)	2.2 C	2.1 C
Position (SVA)	0.3 Deg.	0.28 Deg.

Table 2 PMUX Accuracy

The production PMUX system that was installed on each of the four engines of the engine certification aircraft displayed accuracy that was comparable to the flight test instrumentation. The certification program used PMUX data to supplement flight test instrumentation while also providing a monitor of selected PMUX signals.

The stator-vane angle instrumentation was only provided by PMUX. This data is critical for evaluating any unexpected occurrences that may happen in a flight test program. A confidence in the new PMUX unit was shown by its acceptance as the only source for this data.

Flight Comparison Data

General. The flight test data evaluated was gathered at an altitude of 35,000 feet and an airspeed of .84 Mach. Engines 2 and 3 were operated at engine power settings that varied from approximately 1.24 EPR to 1.73 EPR in a series of steady state steps with the aircraft in level flight. Similar testing was repeated on engines 1 and 4 from approximately 1.26 EPR to 1.73 EPR.

The seven (7) signals that were monitored by both PMUX and flight test instrumentation have comparison records throughout the engine certification program. A review of a number of these records showed excellent correlation of data received from the PMUX and flight test instruments.

EPR Correlation. The EPR signal is a ratio of PT7 to PT2. Both the PMUX and flight test systems operate from their own pressure sensors. Flight traces are shown in Figure 4 where the scale is expanded to illustrate the small differences between the signals being compared. The correlation shows essentially identical dynamic performance in both the short and intermediate term with a difference of .000-.001 EPR (0.08%) for the 50 second test period. The Flight Test instrumentation tolerance requirement is ±0.005 EPR units or ±0.4%. The PMUX specification requirement is ±.002 EPR units or ±0.2%.

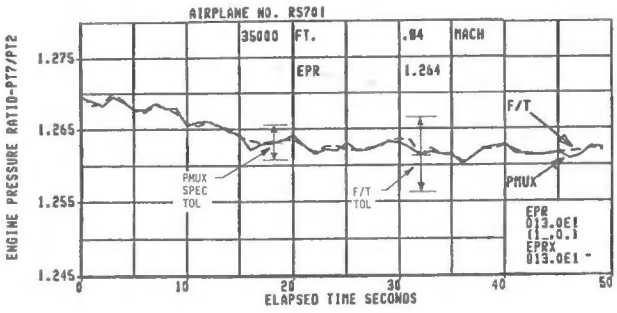


Figure 4. F/T and PMUX 1.264 EPR Comparison

Correlation of N1/N2. The N2 rotor speed data from PMUX shown in Figure 5 does not have the high frequency content of the flight test instrumentation. The PMUX unit has a signal resolution of 0.015% speed and a 0.5 second lag in signal computation. (100% N2 = 7807 RPM). Also, the PMUX data shows a speed excursion of 5 RPM (0.064% N) over the 60 second test period.

The N1 signal also displayed good correlation between PMUX and flight test data. Again the flight test data had more high frequency content and generally there was a difference of 1-2 RPM between the two signals. This is about 1/20 of the accuracy requirement and extremely close to the resolution of the digital computation.

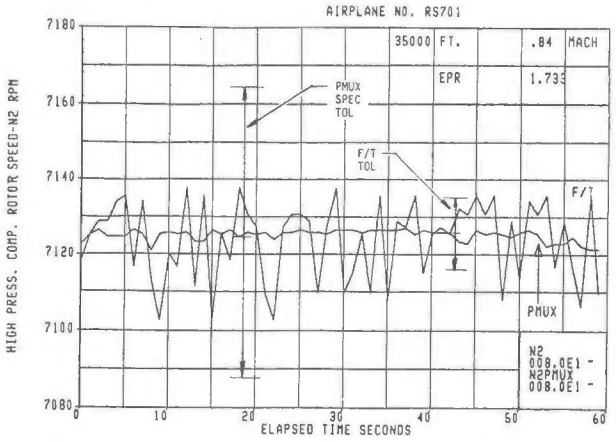


Figure 5. F/T and PMUX N2 Comparison

Fuel Flow Correlation. The requirement to measure fuel flow very accurately has two purposes: 1) to substantiate the guaranteed specific fuel consumption of the engine, and 2) to demonstrate guaranteed nautical air miles per pound of fuel for the aircraft. Fuel Flow comparisons have less meaning since the two readings are acquired from different sensors that may have a variation in their outputs. Figure 6 shows that the PMUX has a higher frequency content; however, the magnitude of these variations are a combination of sensor characteristics and actual fuel flow perturbations. Similar but more highly damped characteristics are seen in the flight test instrumentation.

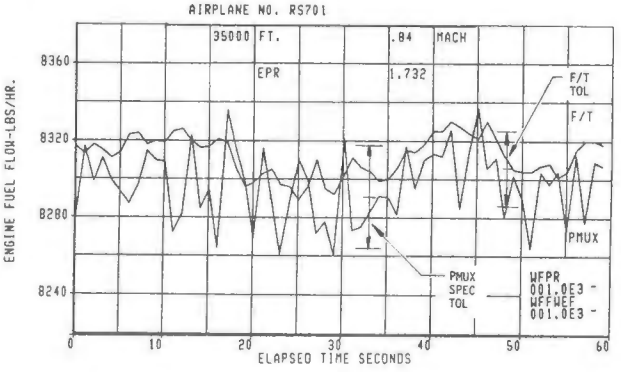


Figure 6. F/T and PMUX Fuel Flow Comparison

EGT Correlation. EGT signal comparisons are presented in Figure 7. Here there is a two degrees C offset (0.4%). Accuracy requirements are 1% for flight test instrumentation and 0.8% for PMUX. The flight test instrumentation was more damped than the PMUX signal.

Pressure Signal Correlation. Figure 8 provides comparisons of PT2 measurements. Dynamic response is similar. The two sensors have an offset difference of about .01 PSIA (0.2%). Similar performance was obtained for PT7. Here one trace was observed to have virtually two identical outputs. Figure 9 shows the correlation over a 50 second period that substantiates the dynamic performance between these two different sensors -- one mounted in the more severe environment of the strut and the other in an environmentally conditioned area in the cabin of the aircraft.

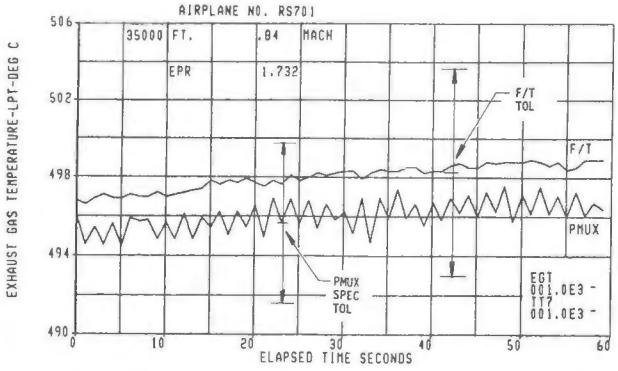


Figure 7. F/T and PMUX EGT Comparison

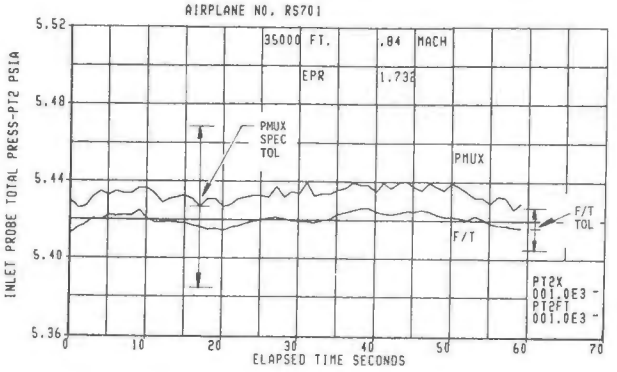


Figure 8. F/T and PMUX PT2 Comparison

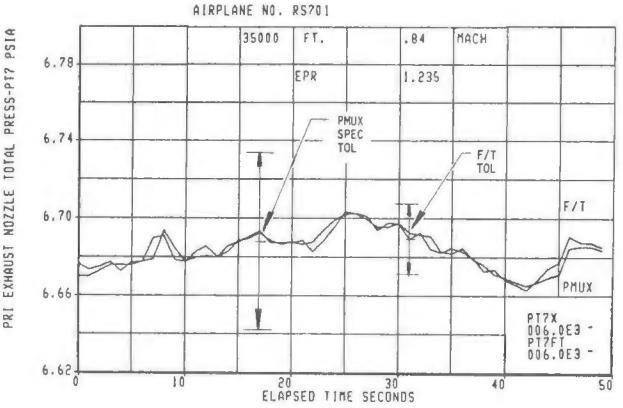


Figure 9. F/T and PMUX PT7 Comparison

PMUX Flight Data

The flight test data for the parameters that were measured only by PMUX are evaluated in pairs. The time history tracings discussed below provide additional information regarding specific engine pressures and temperatures.

The pressure sensors used for PT3 and PS4 are identical in concept with those that are compared with flight test measurements for PT2 and PT7. PT3 information for both engines 2 and 3 is presented in Figure 10. PS4 information at a high EPR condition was obtained for the same engines. In both cases the engine EPRs were different which does establish different nominal settings for the parameters being measured. The compressor discharge pressure for the engine with the higher

EPR setting was 158 PSIA and that with the lower EPR setting was 156 PSIA. Some common minor fluctuations were evident that cannot be evaluated without more in-depth analysis of additional engine data, but it probably does indicate some aircraft settling during the maneuver.

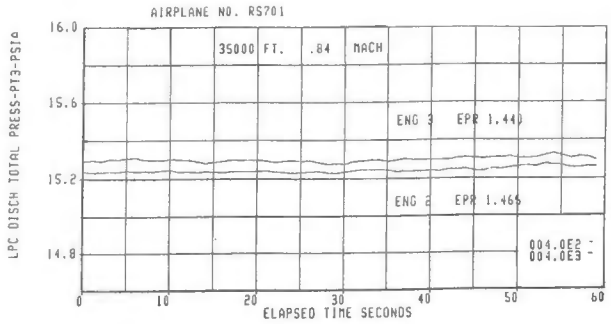


Figure 10. Engines 2 and 3 PT3 Comparison

TT4 measurements, shown on Figure 11, were also made with each engine at a slightly different EPR setting. There is a slight difference in response between the two engines which may be due to small engine-to-engine variations. The tracings provide a measure of the resolution and accuracy of the signal processing of PMUX. The higher powered engine had a temperature variation of about ±0.5 Degrees C around a nominal that was 7 Degrees C above the lower powered engine. The lower powered engine had a very docile temperature history in this test.

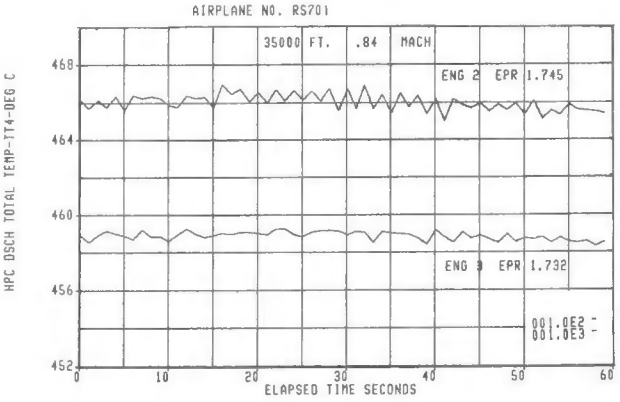


Figure 11. Engines 2 and 3 TT4 Comparison

The stator vane angle data on these engines had a reversal in dynamic signature. The higher powered engine produced a steady trace in contrast to the ±0.02 degree variation measured for the lower EPR engine. The difference between the two stator vane traces was 0.25 degrees or 0.5% of total travel.

To indicate some idea of the resolution provided by the measurements, an engine power setting from 1.74 EPR down to 1.44 EPR had a stator vane change of 1.4 degrees. The fluctuations were just over 2% or 0.08% of the total range of the stator vane angle.

Propulsion Data Multiplexer

General.

The PMUX unit (Figure 12) provides a means for compiling information from individual engines in a format that is convenient for storage and analysis. Its data output is in a standard serial digital format that can be directly transferred to flight test recordings.

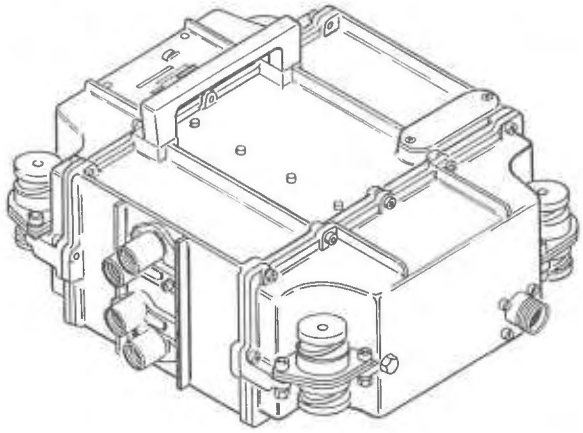


Figure 12. External View of PMUX

To accomplish the task of converting data acquired into a serial digital format, a state-of-the-art microprocessor-based system is used. The power of a digital computer permits additional features to be included in this unique electronic unit. It has built-in-test to monitor its own integrity, fault recording to help shop maintenance in the event it fails, and on-board diagnostics to help isolate a failure occurring in other components.

The PMUX is functionally comprised of: 1) an input interface, 2) pressure sensors, 3) a central processor unit, 4) a solid state memory, 5) an output interface, 6) a power converter, and 7) a maintenance memory. Also the PMUX is designed to receive ARINC 429 serial data that can expand its functional use. In addition to the serial digital output, the unit also provides an output discrete for fault identification.

The PMUX can continuously acquire signals relative to specific engine parameters. The values of these parameters indicate the characteristics or, over a period of time, the trending of engine operation. The acquired (input) signals are primarily in analog form, which are converted to digital form in the PMUX. The digitized signals are processed and those signals that are to be saved are temporarily stored in an internal memory subsystem. The PMUX memory data are then available for subsequent transmittal through the ARINC 429 serial data link. The measured engine parameters, their operating ranges, and the types of sensors that interface with the PMUX unit are listed in Table 3. Most sensor inputs are sampled once every 20 milliseconds (see exceptions in Table 3). The analog signals are converted to digital form by a 12-bit analog to digital converter. The digital speed and fuel flow signals are in the form of tachometer generator/pulse displacement signals; these signals are conditioned to logic levels and isolated from cockpit instruments. The processed signals are tied directly from their processing circuits to the CPU bus.

PARAMETER	TYPE SENSOR	OPERATING RANGE	SAMPLING RATE
PT2	QUARTZ	2 TO 30 PSIA	20 MS
PT3	QUARTZ	2 TO 50 PSIA	20 MS
PS4	QUARTZ	2 TO 500 PSIA	20 MS
PT7	QUARTZ	2 TO 30 PSIA	20 MS
TT3	THERMOCOUPLE	-20°C TO 160°C	20 MS
TT4.5	THERMOCOUPLE	-20°C TO 600°C	20 MS
EGT	THERMOCOUPLE	125°C TO 1050°C	20 MS
N1	TACHOMETER	1.5 TO 123% RPM	40 MS
N2	TACHOMETER	1.5 TO 123% RPM	40 MS
WF	MASS FLOW	615 TO 27000 PPH	300 MS
SVA	RESOLVER	-40 TO 10 ANGLE	40 MS
3.0 BLEED POSITION	POTENTIOMETER	LINEAR SCALING	40 MS
DISCRETE INPUTS	RELAYS AND SWITCHES	N/A	ONE SET PER 200 MS

Table 3 -- PMUX Input Characteristics

Long-term retention of fault data is provided by an EAROM. The CPU stores the fault data in the EAROM. The EAROM is non-volatile. That is, memory will be retained during periods when there is no power to the system. The fault data remains in the EAROM and is available to be output through the serial data link.

Configuration

The PMUX unit measures 11.8 x 10.8 x 4.3 inches, and weighs approximately 13 pounds. The housing assembly contains five stacked PWB modules (Figure 13). The polyimide printed wiring boards utilize copper heat sinks thermally clamped to the enclosure walls. Each of the five multi-layered PWB modules measures approximately 5.2 inches square.

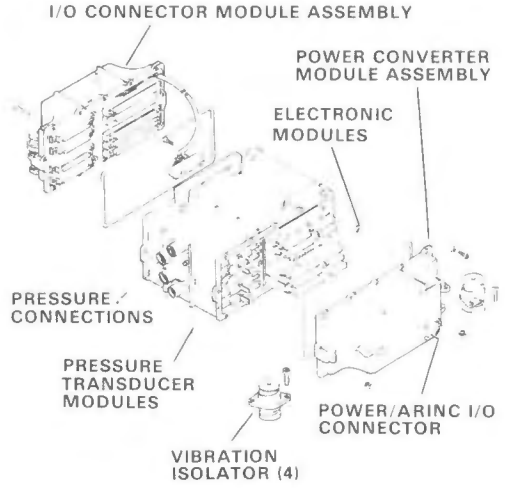


Figure 13. PMUX Exploded View

Four pressure modules are also stacked in the housing assembly. Each of the four pressure modules measures approximately 5.2 x 3.2 x 0.7 inches and weighs 0.5 pound.

The accuracy of the signals handled by PMUX has been discussed in a previous paper(2) but one signal that deserves additional attention is the pressure measurement. The PMUX unit contains four pressure sensors (two of which provide accurate measurements from which engine pressure ratio is computed) and has growth space for a fifth. The accuracies quoted include all factors from the pneumatic source to the serial digital output.

The incorporation of the pressure sensor within the PMUX provides several advantages. It establishes a more benign environment for the sensor and permits installation of all pressure sensors in a common location with system electronics. The computation of an accurate digital word for each of the sensed pressures requires the capability of a digital computer. In the PMUX, the four pressure sensors utilize the same digital computer that performs all of the functions associated with gathering, testing, converting and transmitting all available engine signals.

Pressure sensors (a proprietary design) for the PMUX are single quartz capsule, absolute pressure transducers which are employed in individual pressure subsystems that have a high percent-of-point accuracy over a wide range of pressures. The stability displayed by the sensor is probably more important -- there is no degradation of performance with time or environment.

Each pressure module contains a quartz disk that is sensitive to applied pressure. The disk responds to its pressure environment by changing capacitance. This capacitance is measured in a bridge network which is balanced by controlling an excitation voltage through a multiplying digital to analog converter (MDAC).

The pressure module, working with the main system CPU, accepts a digital feedback number applied to the MDAC to generate an excitation to the feedback capacitor until the bridge is balanced. Any error signal (bridge unbalance) is a pressure module output that runs a digital integrator until the loop is nulled.

The digital pressure signal is constant at a given pressure and temperature, but varies nonlinearly with each. In this design, calibration data(3) is taken over the pressure and temperature range of the modules. The data is processed by matching it to the theoretical performance of the module. This step employs an equation that defines the performance of the module over the complete temperature and pressure range. This complex equation is used to generate a lookup table for each digital value ("N" number) and temperature. This lookup table is then stored in a calibration memory that is located in the pressure transducer. The system CPU reads the N number and the module temperature to compute actual pressure. This configuration achieves high accuracy with no degradation with temperature.

Figure 14 is typical of the performance that has been obtained. Some sensors have given better performance but none offer any difficulty in meeting specified requirements. Figure 15 shows data for one 500 psia transducer.

ARINC 429 Output

The ARINC transmitter consists of a FIFO memory and appropriate timimg circuitry. The FIFO holds eight ARINC 32-bit words for serial transmission. Each ARINC word loaded into the transmitter buffer is received as two 16-bit data words. One of these words is output at a time through the processor Communications Register Unit interface.

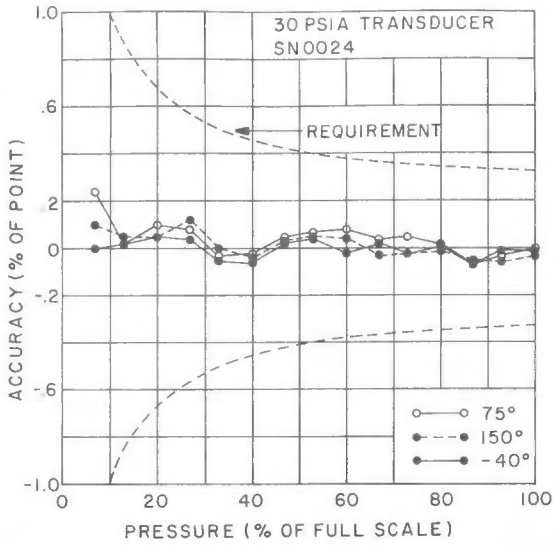


Figure 14. Typical Pressure Sensor Performance

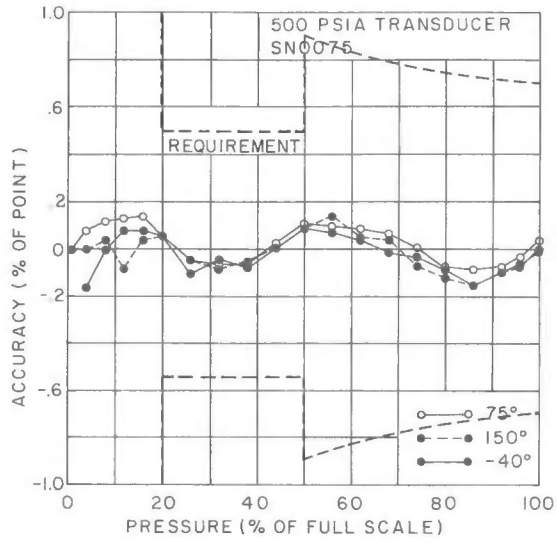


Figure 15. High Pressure Sensor Accuracy

The processor loads up to eight parcels of information at a time into the buffer which converts each of these to ARINC 429 format. An enable bit is set to start the transmitter. The stored words are transmitted, and when the buffer is empty, a signal is sent to the processor to allow a reload.

Software/Memory

Overview. Reviewing the system from its major software aspects highlights many of the same performance features from a different perspective. System memory is partitioned into blocks of 16 bit words. The program code is held in PROM occupying 4096 words (4K) of memory space. 640 words of RAM are provided for data manipulation and storage. The total memory of the PMUX system also contains 512 words of non-volatile EAROM that is used to log a fault data history. With each fault occurrence, a snapshot of key parameters is encoded to aid in fault analysis.

The system PROM is assigned as follows:

	Words	%
Initialization	137	3.35
CIA Interface	120	2.93
Control/Timing	189	4.62
Fault Logic	287	7.01
EAROM Control	684	16.71
Self Test	559	13.66
Input	1134	27.71
Output	208	5.08
Constants	775	13.93
TOTAL	4093	100%

The PMUX operates with a 200 millisecond frame time. The frame time is divided into 20 millisecond major cycles during which inputs are converted and failures are detected and flagged. During each major cycle, different sequences of modules are executed such that some inputs are measured every major cycle (e.g., fuel flow) others every other cycle (e.g., temperatures), and some only once per frame (e.g., discrete inputs). A summary of timing is shown in Table 4.

MAJOR CYCLE	SENSORS CONVERTED	DISCRETE	ARINC OUTPUT
0	N1, N2, WF, PT3, PT7 TCZ, TCG, TT4.5, HPCDT	TCC	EGT, TT3, TT4.5 HPCDT, N1, N2
1	WF, PT2, PS4, EGT, TT3 SVA, 3.0 BLD. EPR	TCAU	WF, SVA, PT3, PT7, PT2, PS4
2	SAME AS 0	TCAL	3.0 BLD, EPR, ESN, DISCRETES, STATUS
3	SAME AS 1	FHV	Reserved for expansion
4	SAME AS 0	---	Reserved for expansion
5	SAME AS 1	---	TEST OR FLAG DATA*
6	SAME AS 0	---	COMMAND ECHO*
7	SAME AS 1	---	EAROM DATA*
8	SAME AS 0	---	EAROM DATA*
9	SAME AS 1	---	EAROM DATA*

*If requested through ARINC input.

Table 4 Timing Operation

The Background Level tasks are assigned to enhance confidence in operating capabilities. In general, these tasks are not time dependent in that the utility of PMUX is not a function of the absolute rate at which these tasks are completed. However, the tasks must be completed at a rate that is high enough to provide rapid detection and orderly shutdown in the event of a failure.

ARINC 429 low speed data may be applied to the PMUX through a pair of input lines. One channel of input selection may be used to command the PMUX to perform certain self-test and display functions. For special test use, ARINC label 020 has been selected. A command word will be sent to the PMUX to order it to perform certain test functions.

Fault Data Storage (EAROM). In the event of a failure causing the "Health" discrete to be de-energized, the system will record both its status and the cause of the failure in EAROM. The EAROM is intended solely as a troubleshooting tool and, under functional operation, snapshot data stored there is not available on the continuous data stream.

EAROM allows reprogramming of individual words or this entire memory segment. An infinite number of read cycles is permitted; however, the memory chips are only guaranteed for 10,000 write/erase cycles to any location.

The philosophy employed in the partitioning and operation of PMUX EAROM involves two considerations: 1) ensuring maximum component life and 2) making sure data is copied and read back accurately.

The 1024 bytes of EAROM are divided into 32 blocks of 32 bytes each. The first block is the status block, and the other 31 are snapshot blocks. The status block stores data necessary to oversee operation of the EAROM, including flags to indicate the range of recorded faults, and a pointer to the next snapshot. If more than 30 snapshots are recorded, the EAROM will "wrap around" to save the most recent 30 snapshots.

Additional Uses

Digital systems have more capability than the basic requirements of a data multiplexer. Additional requirements can be accommodated.

Fault Interrogation. The present unit includes a serial input that is used to interrogate the maintenance memory. This feature uses one of many addresses that could increase the access to available data. It can read information that is not normally part of the output data: 1) distribution of raw outputs (non filtered), 2) sequential read of all EAROM, and 3) PMUX unit temperature. Another ability is to pass through any data that is placed on the ARINC input lines.

Output Recall. One interesting expansion of PMUX is to add a feature for historical review of engine parameters. All outputs can also be stored in a special memory. The concept is similar to instant replay of a sporting event -- the data would be continuously recorded-and-discarded until a decision is made that some data is of interest. On command, a permanent record is made of this data.

This capability would be gained by a RAM which records the latest several minutes of PMUX output data. The memory would consist of eight 64K dynamic RAM chips, refresh logic, and address decoding. The present PMUX system installed in the 747-300 has two growth slots and can accept this addition.

The object of the special recall memory is to preserve the high computational resolution of the PMUX in order to provide data for diagnosing the cause of some occurrence. The memory would use a wraparound technique to constantly preserve the most recent outputs (3.4 minutes worth if every output set is saved). Recording of these outputs can be terminated by a cockpit command or some combination of alarm logic. Data saved is then made available in LIFO fashion.

The new memory would be divided into 1024 blocks of 64 bytes (32 words) each. Of the 32 words in a block, 18 are allocated for storing one set of standard outputs, 12 more handle the expansion capability, and two are used for housekeeping tasks. One block is written for each set of outputs saved. At one block per output cycle (one per 200 milliseconds), 3.4 minutes of data are preserved. If more time is desired, blocks can be written less often (e.g., if one block is written every second, 17 minutes can be preserved.)

The logic to stop recording would not discontinue the standard output but would hold the data currently in the replay memory until a second command is received. This would cause the data contained in the memory to be sent on a dedicated label during the second half of each 200 millisecond output cycle.

Analysis of the data would be made from standard recording equipment. After the transmission is complete, the memory subsystem would return to the recording mode.

Conclusion

The microprocessor based PMUX that is an option on the production 747-300 aircraft, played a role in the certification of the JT9D-7R4G2 engine. During the certification flight testing, it demonstrated a capability to accurately gather engine data, both as a backup for flight test instrumentation and as an only source for specific engine parameters. Additionally, PMUX inputs to the flight test onboard data system allowed monitoring of numerous engine parameters to assure: real time data validity, that engine operation was acceptable during each test condition, and that engine test conditions were conducted within required tolerances.

The signal accuracy of PMUX was compared with flight test instrumentation and exhibited the ability to exceed design requirements, possibly opening the prospects for an improvement in engine gas path analysis. The exceptional performance obtained during the first four months of flight use is expected to continue in airline service.

The pressure sensor selected for PMUX has shown exceptional stability to complement its basic design accuracy. This sensor offers an improvement in the state-of-the-art; its service history will provide valuable additional information that should encourage its use in future flight test activities.

PMUX has been successful, it has introduced a new era in parameter measurement and can open the door to expansion of engine condition monitoring.

References

(1) S. G. Danielson, G. Dienger, "A European View of Gas Turbine Monitoring in Current and Future Civil Aircraft AIAA paper 79-1200, June 1979.

(2) J. A. Bluish, and W. Lorenz, "PMUX -- The Interface for Engine Data to AIDS" AIAA paper 82-1127, June 1982.

(3) F. Antonazzi, Sr., "Pressure Transducer Calibration Process", SAE Paper 811076, October 1981.

THE F110 ENGINE MONITORING SYSTEM

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Abstract

An Engine Monitoring System (EMS) is being developed at General Electric for the F110-GE-100 engine. This engine is designed for application in either F-16 or F-15 aircraft. The EMS is designed to acquire relevant engine and aircraft data during flight, process this data and provide a concise output at flightline to define recommended maintenance actions. The system also provides for the transfer of stored data from the aircraft into the USAF ground computer system for additional processing and output to the appropriate user. A description of the EMS is presented, together with a development status as of August 1984.

Introduction

Early in 1983, General Electric received a contract from the USAF for the full scale development of the F110-GE-100 engine. Included in this contract was the requirement for an Engine Monitoring System (EMS). The scope of the EMS was not only to include a data acquisition function but to transfer, process and present the data for maintenance use. More specifically, the system was required to incorporate the following features:

(a) Determination of engine limit exceedances.

(b) Isolation of the source of these limit exceedances to the appropriate level.

(c) Acquisition of data to support long term engine performance trending.

(d) Acquisition of data to enable the tracking of life-limited engine components.

(e) Indication of flightline go/nogo to reflect the engine status as determined by EMS.

(f) Ground support software to process EMS data and interface with other USAF data systems.

In addition to these specific requirements, it was recognized that for the EMS to be accepted by the user and become a fully integrated part of the engine management system, several fundamental features are essential. The EMS needs to be simple yet effective and keyed to the existing USAF maintenance organization. The resulting equipment designs need to be rugged and reliable, yet maintainable. Above all, the output products of the system must be supportive of all levels of the engine maintenance effort.

One of the most significant factors of the F110 EMS development is that despite the involvement of various disciplines due to the wide scope of the program, a single systems design organization has responsibility for all aspects. The presence of such a focal point will result in a highly integrated system approach.

Design of the EMS commenced in January 1983. The overall system approach plus the functional definition of the individual EMS components was completed in May of the same year. Sources were subsequently selected and placed on contract for the detailed design, development and qualification of the EMS components in July 1983. Delivery of the first production, qualified units are scheduled in December 1985, consistent with the F110-GE-100 delivery schedule.

System Description

At the commencement of the EMS design phase, the F110-GE-100 design was already at an advanced stage, evolving from the F101 Derivative Fighter Engine (DFE) configuration. As a result, the essential engine control and cockpit instrumentation was already in existance and only a few minor changes were proposed for the F110-GE-100 development effort. Additionally, the basic configuration of the engine electronic control (designated Augmentor Fan Temperature Control - AFTC) was also defined.

The AFTC is a full authority analog control designed with electrical connectors which allowed real time access to the engine parameters in analog form. This feature is normally utilized during engine development testing at the factory to provide a test monitoring capability and to assist in troubleshooting faults.

The above hardware configuration provided a "ready made" primary interface for the EMS, and no dedicated sensors were therefore added for EMS purposes. The resulting EMS configuration which interfaces with the AFTC consists of three hardware components; an engine mounted EMS processor (EMSP), an airframe mounted EMS computer (EMSC) and a data display and transfer unit (DDTU) - flightline equipment.

The relative locations of this hardware are shown for the F-16 application in Figure 1. The functional relationships and interface definitions are illustrated in Figure 2.

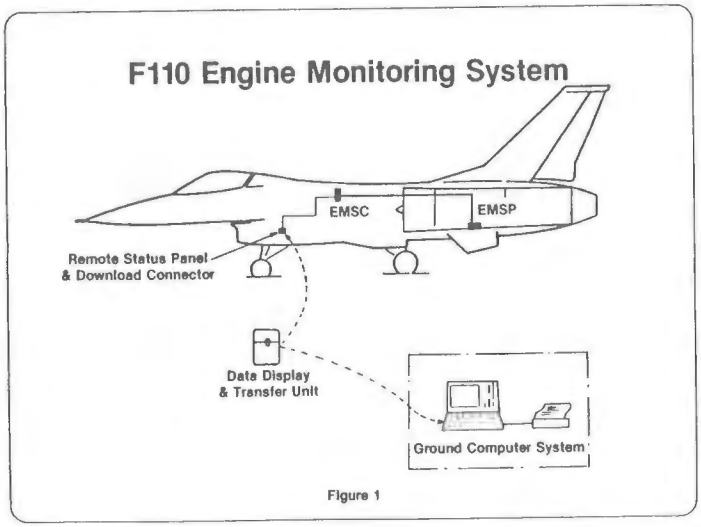

Figure 1

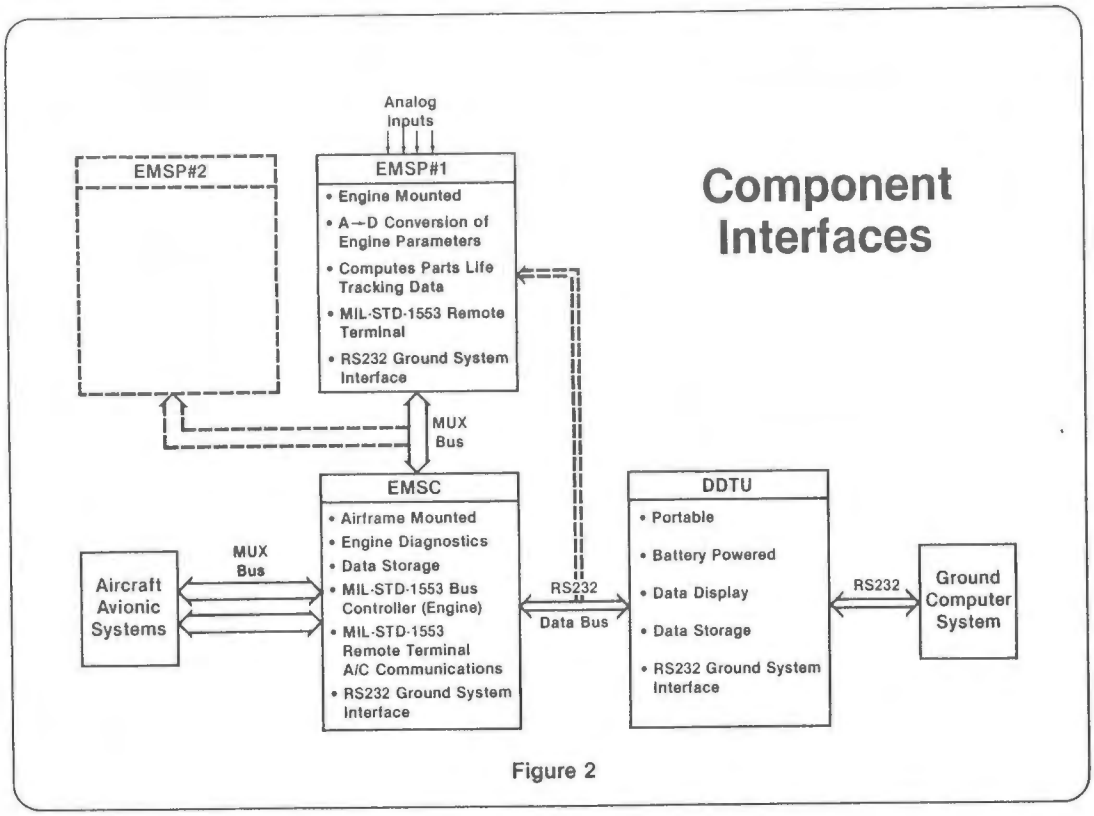

Figure 2

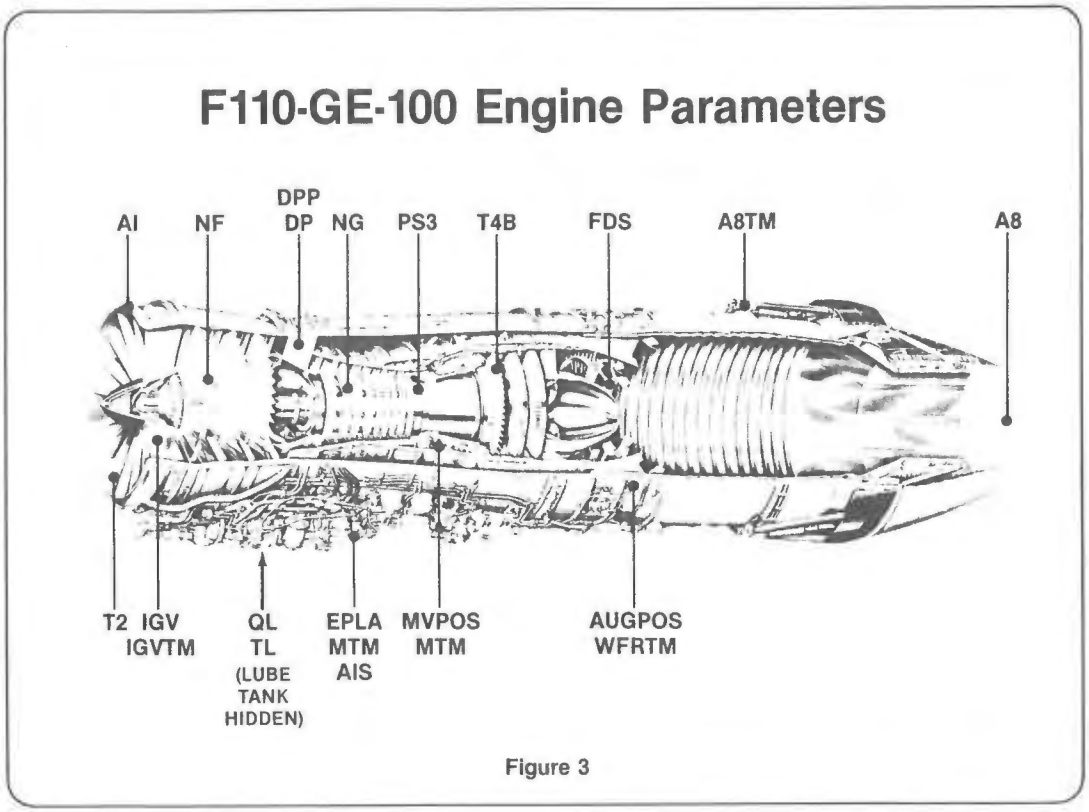

Figure 3

Data Acquisition

All of the engine parameters are available at the AFTC on two connectors which separate control and non-control parameters such as anti-ice valve position, lube temperature and lube tank level. The total list of engine parameters utilized by the EMS is shown below:

Parameter	Symbol
HP Turbine Blade Temperature	T4B
Engine Power Lever Angle	EPLA
Fan Inlet Temperature	T2
Fan Inlet Guide Vane Position	IGV
Compressor Discharge Pressure	PS3
Main Fuel Valve Position	MVPOS
Main Torque Motor Current	MTM
Fan IGV Torque Motor Current	IGVTM
Lube Tank Quantity	QL
Fan Speed	NF
Core Speed	NG
Aircraft Power Lever Angle (F-16)	APLA
Exhaust Nozzle Area	A8
Fan Duct Pressure Ratio	DPP
Fan Duct Pressure Delta	DP
Augmentor Fuel Valve Position	AUGPOS
Augmentor Fuel Valve Torque Motor Current	WFRTM
Exhaust Nozzle Torque Motor Current	A8TM
Anti-Icing Valve Position	A/I
Lube Temperature	TL
Augmentor Flame Detector Signal	FDS
Augmentor Initiation Signal	AIS

The sources of these parameters on the engine are illustrated in Figure 3. At the AFTC, all of the above are available in analog form and are routed to the engine mounted EMSP where they are multiplexed and digitized in readiness for subsequent transmission to the airframe mounted EMSC. This communication link is made by provision of a MIL-STD-1553B Mux Bus (non-redundant), for which the EMSC is the bus controller and the EMSP a remote terminal. In the case of the F-15 application, the EMSPs from both engines communicate with the EMSC on this bus.

The EMS also utilizes aircraft related parameters, in order to relate engine faults to flight conditions and assist in the diagnostic process. These aircraft parameters are listed below:

Parameter	Symbol
Aircraft Mach Number	MN
Angle of Attack	AOA
Normal Acceleration	NA
Total Engine Fuel Flow	TFF
Altitude	ALT
Weight on Wheels	WOWS
(Gear Up - F-16)	(GUL)

The above parameters are made available directly to the EMSC in digital form via the aircraft MIL-STD-1553B Mux bus (dual-redundant). Thus, the EMSC is a digital unit with both non-redundant and redundant -1553 interfaces.

Data Types

Four types of data are available from the EMS: Diagnostic Data, Parts Life Tracking Data, Trend Data and Pilot Initiated Data.

Diagnostic Data - This is parametric data saved as a result of a detected engine abnormality. This may be a major limit exceedance or an out of limit control schedule or a secondary system abnormality, low lube level, etc. In addition to detection of exceedances, the system incorporates isolation logic aimed at identifying the engine line replaceable unit (LRU) causing the exceedance. This detection/isolation logic is present within the EMSC, which also provides the storage medium for the data. Figure 4 presents an overview of the EMSC engine diagnostic logic. The amount of diagnostic data saved is dependent upon the type of exceedance or fault. When pre-event information is considered useful, as is the case with a compressor surge, then 12 data records are saved (6 seconds worth). Additionally, post event data is saved for all detections. The amount, however, is again dependent upon the usefulness to the maintenance personnel. Overspeeds and overtemperatures are considered sufficiently important that 18 data records are saved (9 seconds) after event recognition. For the majority of faults and exceedances, however, only 4 post event (2 seconds worth) are saved.

Parts Life Tracking Data - This data is computed and stored by the EMSP on a cumulative basis and is used by the ground computer systems to track life limited engine components. This tracking allows predictions for maintenance planning and spares provisioning. The data consists of engine operating times and cycles as detailed below:

- Time above T4B (5 levels)
- Engine Operating Time
- Augmentor Operating Time
- Augmentor On/Off Cycles
- Low Cycle Fatigue Counts
- Full Thermal Cycles
- Cruise - Intermediate
  - Cruise Cycles

Trend Data - This data is automatically acquired and stored by the EMSC, during the take off sequence. Four data records (2 seconds worth) are saved per flight. No further trend records are saved until the next mission.

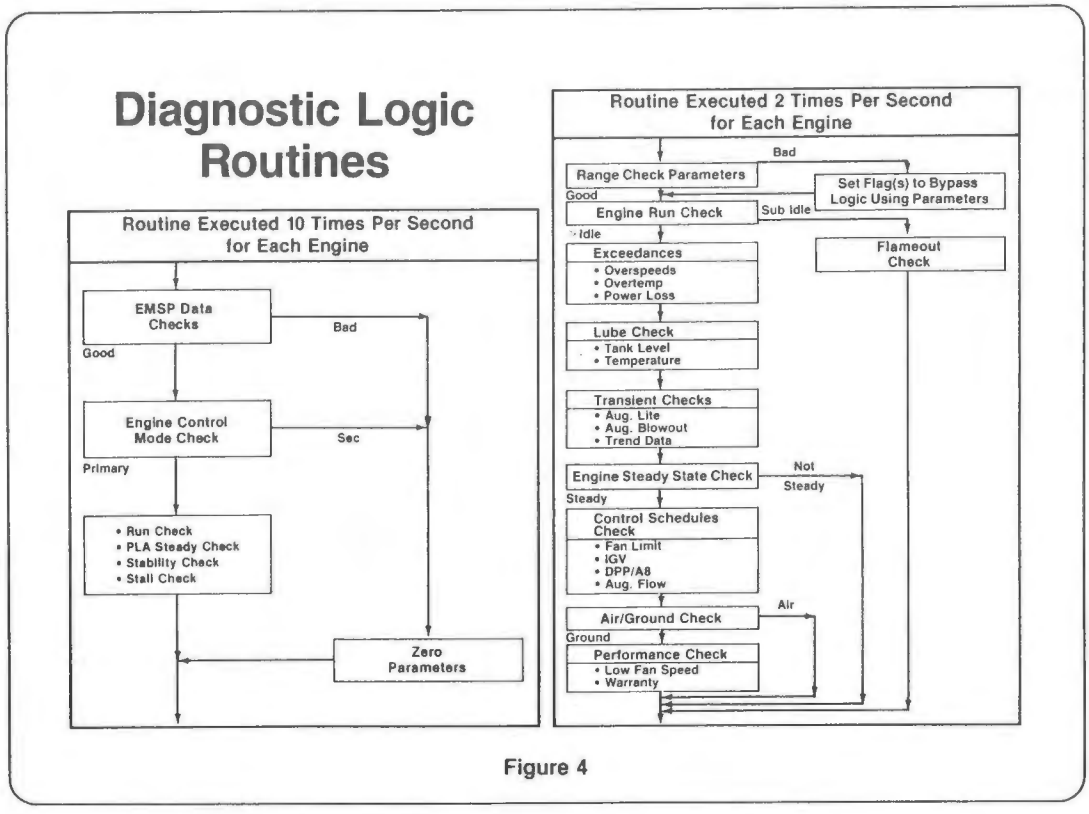

Figure 4

Pilot Initiated Data - In addition to the EMS automatically saving data as a result of an abnormality, the capability exists for the pilot to request a data save. When a cockpit switch is activated, pre event data (6 seconds worth) and short post event data (2 seconds worth) is saved. If the EMSC is in the process of saving data when the pilot makes the request, the larger of the two requests are honored i.e. data record duplication does not result.

Data Flow

The majority of the EMS data is acquired by the EMSC. The parts life tracking data, however, is computed by the EMSP and stored within that unit. This is done so that the engine usage status is always available even when the engine is not installed. However, to enable a single data download point for all the airborne data, the parts life tracking data is transmitted on a regular basis to the EMSC and the latest cumulative values stored within that unit.

All stored system data is available in the EMSC when the engine is in the installed condition in the aircraft and the EMSC is accessed by the DDTU. This device provides the link between the airborne equipment and the USAF ground computer system. In addition to temporary storage of the flight data, the DDTU provides a display. This display allows the maintenance personnel to view at flightline the detected fault/isolation message determined by the EMSC. Also displayed are overspeed/ overtemperature peak values and exceedance times when present.

The DDTU allows multiple aircraft (normally a squadron) to be downloaded before returning to the ground computer system for transfer of its stored data.

The single entry point of all data into the ground computer system occurs at the aircraft maintenance unit (AMU). At this facility, which is adjacent to the flightline, the data is formatted and processed. The exceedance and pilot initiated data is presented for display and hard copies can be obtained. The trend and parts life tracking data are subsequently transferred to the base level, engine management branch (EMB) of the maintenance organization. Whereas the AMU is typically responsible for one squadron of aircraft (24), the EMB will be the focal point for data from, typically, three AMU's plus data from the airbase test cell facility. At the EMB, the trend data is processed and displayed graphically. The parts life tracking data is formatted for transfer to the USAF's tracking system which is accomplished using the base's mainframe computer.

System Hardware

The three EMS components supplied by GE and outlined on Figures 1 and 2 are described in more detail below:

Engine Monitoring System Processor (EMSP) - The EMSP is mounted on the F110-GE-100 engine at approximately the 6 o'clock position and aft of the electronic control (AFTC) from which it receives its inputs. The EMSP is mounted on four vibration isolators and is fuel cooled. This essentially solid state device utilizes a 16 bit microprocessor and employs "plug in" multilayer printed circuit board technology. It is powered by the engine alternator and consumes approximately 30 watts under normal operation. See Figure 5.

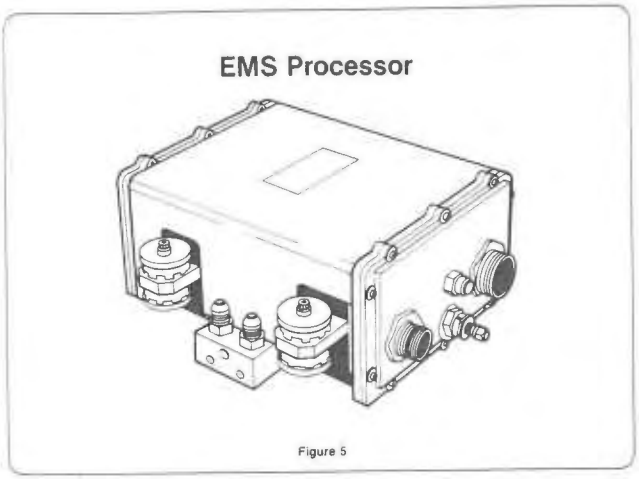

Figure 5

Engine Monitoring System Computer (EMSC) - In the F-16 aircraft, the EMSC is hard mounted in the flap drive bay. This aircraft compartment is in the center fuselage, rear of the canopy, and is environmentally controlled in that the upper temperature in the bay is limited by cooling air. For this application, the EMSC is convection cooled. In the F-15 aircraft, the EMSC is located in the left hand engine inlet diffuser area. This compartment has no environmental control. The EMSC, therefore is fed with aircraft cooling air and mounted on a vibration isolated tray. The EMSC (see Figure 6) is a 16 bit microcomputer and utilizes a similar "plug in" multilayer circuit board construction as the EMSP. It is powered by an aircrft 28V DC supply and consumes approximately 40 watts.

Data Display and Transfer Unit - The DDTU is a portable, ruggedized piece of flightline equipment (See Figure 7). It contains a 28V battery which is used to power itself and the airborne unit (EMSC or EMSP) during the data transfer operation. The DDTU has a 20 character liquid crystal display that enables fault/isolation messages (determined by the EMSC) to be displayed at the flightline. Internally, the DDTU is based on the same 16 bit microprocessor used in the EMSC, and employs the same circuit board technology. Sufficient non-volatile memory is included to allow download of a squadron (24) of F-15 or F-16 aircraft in one session.

Ground Computer System - The USAF has selected the Zenith Z100 microcomputer to provide the ground station function for the EMS. This unit is a desk top style personal computer with a built-in single 5 1/4" floppy disk drive and a 10 M byte Winchester hard disk. An Okidata dot matrix printer completes the hardware package. A Z100 system will be located at each aircraft maintenance unit (AMU) facility. Additional units will be located at the engine management branch (EMB) and at the test cell facility. All systems will be identical except for the EMB unit which will have an increased (40 M byte) hard disk capability. The software package for the Z100, to process and format the EMS data and present it to the appropriate users, is being developed at General Electric.

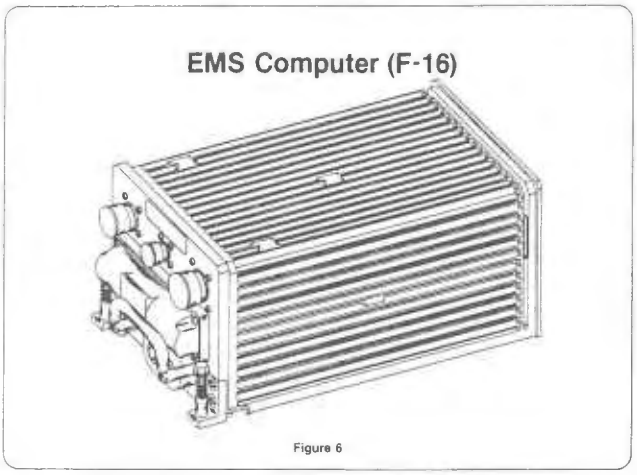

Figure 6

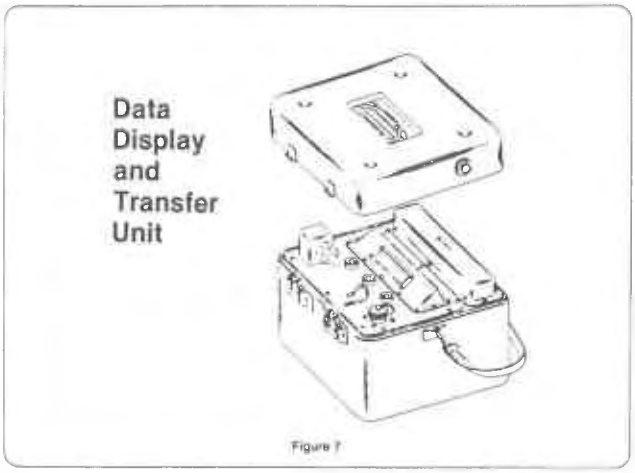

Figure 7

Development Status

As of August 1984, the development of the EMS components had progressed as follows:

EMSP - The design of this component is complete and the first two development units are available for evaluation. One unit is currently being used for system rig tests, while the second unit is installed on a factory test engine. Bench qualification of the EMSP will be completed during the last quarter of 1984.

EMSC - The design of this component is also complete and the first development unit is available. This unit will be used to monitor a factory engine test scheduled for the last quarter of 1984. Bench qualification of the EMSC is scheduled to be completed in the first quarter of 1985. In addition, EMS will be included in F-16 flight test during 1985. This flight test will have both engine (EMSP) and airframe (EMSC) units installed for evaluation.

DDTU - The design of the DDTU has been completed and a critical design review (CDR) with the USAF scheduled for October 1984. A prototype DDTU will be available to support the planned F-16 flight test in 1985. Qualification testing of the DDTU is to take place the third quarter of 1985. Production deliveries of all units (EMSP, EMSC and DDTU) are scheduled to commence December 1985.

Z100 Software - Design of this software is in progress with initial efforts devoted to completing the data interface and formatting modules. These functions are to be incorporated in October 1984 to support the planned factory testing of the EMSP/EMSC. Additional modules to support handling of the trending and parts life tracking data are planned to be in place to support the F-16 flight test. Delivered software to the USAF is required December 1985 to be consistent with the hardware deliveries.

In summary, development of the F110 EMS is proceeding on schedule. Hardware and software will be available early enough to take advantage of the extensive factory and flight test program.

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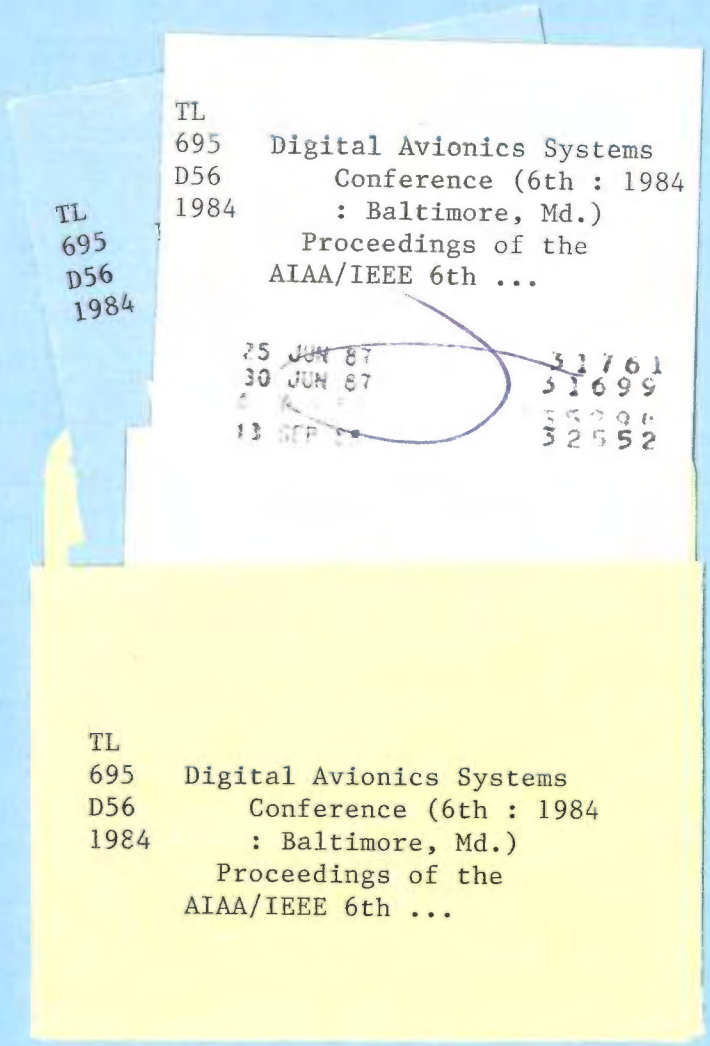

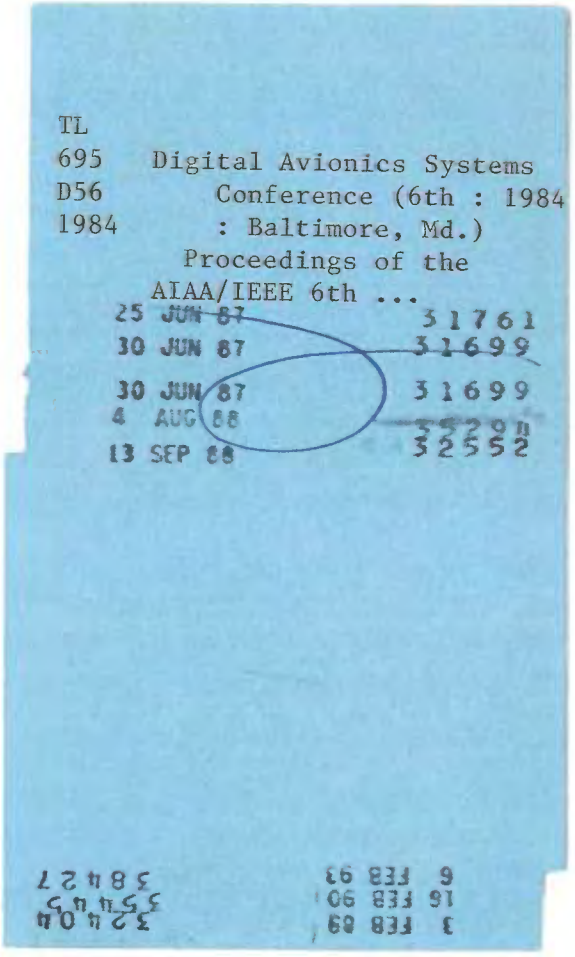
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