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Paper No. 8
Filed: December 7, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

SAMSUNG ELECTRONICS COMPANY, LTD.,
Patent Owner.

Case IPR2015-01318
Patent 8,252,675 B2

Before JAMESON LEE, PATRICK R. SCANLON, and JUSTIN BUSCH, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

On June 1, 2015, a Petition (Paper 1, "Pet.") was filed to institute *inter partes* review of claims 1–15 of U.S. Patent No. 8,252,675 B2 (Ex. 1001, "the '675 patent"). Patent Owner filed a Preliminary Response (Paper 6, "Prelim. Resp.") on September 10, 2015.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a):

> THRESHOLD.—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Having considered both the Petition and the Preliminary Response, we are not persuaded, under 35 U.S.C. § 314(a), that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing the unpatentability of any of claims 1–15 of the '675 patent on any alleged ground. Accordingly, we do not institute an *inter partes* review of any claim.

B. Related Matters

The parties indicate that the '675 patent is at issue in *Samsung Electronics Co., Ltd. v. NVIDIA Corp.*, 3:14-cv-00757-REP (E.D. Va). Papers 1, 4.

C. The '675 Patent

The '675 patent relates to a method of forming an insulated-gate transistor (independent claim 1) and a method of forming an integrated circuit device (independent claim 6). The Background of the Invention portion of the Specification does not articulate any problem with prior art methods, and the Summary portion of the Specification does not articulate what objective or advantage is achieved by the invention, relative to prior art methods. The Background of the Invention portion states:

> MOS transistors are classified as n-MOS transistors or p-MOS transistors in accordance with the channel type which is induced beneath the gate electrode. The gate electrodes of the n-MOS transistor and the p-MOS transistor may be formed of different metals so that the n-MOS transistor and the p-MOS transistor have different threshold voltages.

Ex. 1001, 1:24–30. None of the independent claims at issue requires the formation of both an n-MOS and a p-MOS transistor, much less an n-MOS and a p-MOS transistor that have respectively different threshold voltages. Independent claims 1 and 6 each require a metal gate electrode that itself comprises multiple metal layers, and claim 6 additionally specifies that the gate electrode is that of a PMOS transistor.

Aside from requiring multiple metal layers in the gate electrode, each of claims 1 and 6 requires formation of a dummy gate electrode, removal of the dummy gate electrode, and then the formation of a new metal gate electrode by deposition of multiple additional metal layers. Those additional metal layers are referred to in claim 1 as first metal

layer and second metal layer, and in claim 6 as second metal gate electrode layer and third metal gate electrode layer.

Of all the challenged claims, claims 1 and 6 are the only independent claims. They are reproduced below:

> 1. A method of forming an insulated-gate transistor, comprising:
>
> forming a gate insulating layer on a substrate;
> forming a metal buffer gate electrode layer on the gate insulating layer;
>
> **forming a dummy gate electrode layer** on the buffer gate electrode layer, said dummy gate electrode layer and said buffer gate electrode layer comprising different materials;
>
> patterning the dummy gate electrode layer and the buffer gate electrode layer in sequence to define buffer gate electrode on the gate insulating layer and a dummy gate electrode on the buffer gate electrode;
>
> forming electrically insulating spacers on sidewalls of the dummy gate electrode and on sidewalls of the buffer gate electrode;
>
> covering the spacers and the dummy gate electrode with an electrically insulating mold layer;
>
> removing an upper portion of the mold layer to expose an upper surface of the dummy gate electrode;
>
> **removing the dummy gate electrode** from between the spacers by selectively etching back the dummy gate electrode using the mold layer and the spacers as an etching mask;

depositing a first metal layer onto an upper surface of the mold layer and onto inner sidewalls of the spacers and onto an upper surface of the buffer gate electrode;

filling a space between the inner sidewalls of the spacers by **depositing a second metal layer** onto a portion of the first metal layer extending between the inner sidewalls of the spacers to thereby **define a metal gate electrode comprising a composite of the second metal layer, a portion of the first metal layer having a U-shaped cross-section and the buffer gate electrode**.

Id. at 10:59–11:26 (emphasis added).

6. A method of forming an integrated circuit device, comprising:

forming a gate insulating layer on a substrate;

forming a first metal gate electrode layer on the gate insulating layer;

forming a dummy gate electrode layer on the first metal gate electrode layer, said dummy gate electrode layer and said first metal gate electrode layer comprising different materials;

patterning the dummy gate electrode layer and the first metal gate electrode layer in sequence to define a dummy gate electrode on the patterned first metal gate electrode layer;

forming electrically insulating spacers on sidewalls of the dummy gate electrode and on sidewalls of the patterned first metal gate electrode layer;

removing the dummy gate electrode from between the spacers by selectively etching back the dummy gate electrode using the spacers as an etching mask;

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