PHOTORESIST ETCH BACK METHOD FOR GATE LAST PROCESS

BACKGROUND

[0001] The present disclosure relates generally an integrated circuit device and, more particularly, to a gate structure and method of forming a gate of an integrated circuit device.

[0002] As technology nodes shrink, in some IC designs, there has been a desire to replace the typically polysilicon gate electrode with a metal gate electrode to improve device performance with the decreased feature sizes. Providing metal gate structures (e.g., including a metal gate electrode rather than polysilicon) offers one solution. One process of forming a metal gate stack is termed "gate last" process in which the final gate stack is fabricated "last" which allows for reduced number of subsequent processes, including high temperature processing, that must be performed after formation of the gate. Additionally, as the dimensions of transistors decrease, the thickness of the gate oxide must be reduced to maintain performance with the decreased gate length. In order to reduce gate leakage, high dielectric constant (high-k) gate insulator layers are also used which allow greater physical thicknesses while maintaining the same effective thickness as would be provided by a typical gate oxide used in larger technology nodes.

[0003] There are challenges to implementing such features and processes in CMOS fabrication however. As the gate lengths decrease, these problems are exacerbated. For example, in a "gate last" fabrication process, voiding can occur when depositing a metal film into a trench to from the metal gate electrode. As gate lengths decrease, the trench also decreases in size, and depositing metal into the trench becomes increasingly difficult, and increasingly likely to form a void.

[0004] Therefore, what is needed is an improved gate structure and device and method of gate formation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] Figs. 1-3 are cross-sectional views of a semiconductor device at various stages of fabrication in an embodiment of a gate last process.

[0007] Figs. 4 and 5 are cross-sectional views of a semiconductor device during metal deposition processes of an embodiment of a gate last process.

[0008] Fig. 6 is a flowchart of an embodiment of a method of forming a gate including a gate last process according to various aspects of the present disclosure.

[0009] Figs. 7-15 are cross-sectional views of a semiconductor device of at various stages of fabrication according to the method of Fig. 6.

DETAILED DESCRIPTION

[0010] The present disclosure relates generally to forming an integrated circuit device on a substrate and, more particularly, to fabricating a gate structure as part of an integrated circuit (including FET devices). It is understood, however, that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. In addition, the present disclosure provides examples of a "gate last" metal gate process, however one skilled in the art may recognize applicability to other processes and/or use of other materials.

[0011] Referring to Figs. 1, 2, and 3 illustrated are cross-sectional views of a semiconductor device at various stages of fabrication in a gate last process. The various stages of the device are illustrated as device 100, 200, and 300 respectively. One or more features, for example of the device 100, may be included in the devices 200 and 300 and remain substantially unchanged except as noted herein. The devices 100, 200, and 300 may be intermediate devices fabricated during processing of an integrated circuit, or portion thereof, that may comprise static random access memory (SRAM) and/or other logic circuits, passive components such as resistors, capacitors, and inductors, and active components such as P-channel field effect transistors (PFET), N-channel FET (NFET), metal-oxide semiconductor field effect transistors (MOSFET), complementary metal-oxide semiconductor (CMOS) transistors, bipolar transistors, high voltage transistors, high frequency transistors, other memory cells, and combinations thereof.

[0012] The semiconductor device 100 includes a substrate 102. Formed on the substrate 102 are shallow trench isolation (STI) structures 104, source/drain regions 106 (including source/drain extension regions 108), a gate dielectric 110, contacts 112, a contact etch stop layer (CESL) 114, spacers 116, a dummy gate pattern 118, hard mask layer 120, and a dielectric layer 122.

[0013] In an embodiment, the substrate 102 includes a silicon substrate (e.g., wafer) in crystalline structure. The substrate 102 may include various doping configurations depending on design requirements as is known in the art (e.g., p-type substrate or n-type substrate) Other examples of the substrate 102 may also include other elementary semiconductors such as germanium and diamond. Alternatively, the substrate 102 may include a compound semiconductor such as, silicon carbide, gallium arsenide, indium arsenide, or indium phosphide. Further, the substrate 102 may optionally include an epitaxial layer (epi layer), may be strained for performance enhancement, and/or may include a silicon-on-insulator (SOI) structure.

[0014] The shallow trench isolation (STI) features 104 formed in the substrate 102 may isolate one or more devices from each other. The STI features 104 may include silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), and/or a low k dielectric material. Other isolation methods and/or features are possible in lieu of or in addition to STI. The STI features 104 may be formed using processes such as reactive ion etch (RIE) of the substrate 102 to form trenches which are then filled with insulator material using deposition processes followed by CMP process.

[0015] The gate structure formed using the dummy gate pattern 118 may be configured as P-channel or N-channel as is known in the art. The dummy gate pattern 118 is a sacrificial layer. The dummy gate pattern 118 may include polysilicon. In an embodiment, the dummy gate pattern 118 includes amorphous silicon. The dummy gate pattern 118 may be formed by MOS technology processing such as polysilicon deposition, photolithography, etching, and/or other suitable methods.

[0016] The gate dielectric 110 may include a high dielectric constant (high-k) material. In an embodiment, the high-k dielectric material includes hafnium oxide (HfO_2). Other examples of high-k dielectrics include hafnium silicon oxide (HfSiO), hafnium silicon oxynitride (HfSiON), hafnium tantalum oxide (HfTaO), hafnium titanium oxide (HfTiO), hafnium zirconium oxide (HfZrO), combinations thereof, and/or other suitable materials. The semiconductor device 100 may further include, various other dielectric and/or conductive layers, for example, interfacial layers and/or capping layers underlying the dummy gate pattern 118. In an embodiment, a capping layer (e.g.,

dielectric layer) is formed on the gate dielectric 110. The capping layer may adjust the work function of the subsequently formed metal gate. The capping layer may include a metal oxide (LaOx, MgOx, AlOx), metal alloyed oxide (BaTiOx, SrTiOx, PbZrTiOx), a combination thereof, and/or other suitable materials. In another embodiment, a metal layer is formed on the gate dielectric layer. The overlying metal layer may adjust the work function of the subsequently formed gate.

[0017] The spacers 116 may be formed on both sidewalls of the dummy gate structure 118. The spacers 116 may be formed of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, fluoride-doped silicate glass (FSG), a low k dielectric material, combinations thereof, and/or other suitable material. The spacers 116 may have a multiple layer structure, for example, including one or more liner layers such as liner layer 117. The liner layer 117 may include a dielectric material such as silicon oxide, silicon nitride, and/or other suitable materials. The spacers 116 may be formed by methods including deposition of suitable dielectric material and anisotropically etching the material to form the spacer 116 profile.

[0018] The hard mask layer 120 may include silicon nitride, silicon oxynitride, silicon carbide, and/or other suitable materials. The hard mask layer 120 may be formed using methods such as chemical vapor deposition (CVD), physical vapor deposition (PVD), or atomic layer deposition (ALD). In an embodiment, the hard mask layer 120 is between approximately 100 and 500 angstroms in thickness.

[0019] The source/drain regions 106 including lightly doped source/drain regions shown as regions 108 and heavy doped source/drain regions, are formed on the substrate 102. The source/drain regions 106 may be formed by implanting p-type or n-type dopants or impurities into the substrate 102 depending on the desired transistor configuration. The source/drain features 106 may be formed by methods including photolithography, ion implantation, diffusion, and/or other suitable processes. The contact features 112, coupled to the source/drain regions 106, may include silicide. The contact features 112 may be formed on the source/drain regions 106 by a salicide (self-aligned silicide) process. The contacts 112 may include nickel silicide, cobalt silicide, tungsten silicide, tantalum silicide, titanium silicide, platinum silicide, erbium silicide,

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