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**Yeh et al.**

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(54) **PHOTORESIST ETCH BACK METHOD FOR GATE LAST PROCESS**

(56) **References Cited**

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(\* ) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 60 days.

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(21) Appl. No.: **12/477,618**

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**Related U.S. Application Data**

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(60) Provisional application No. 61/096,633, filed on Sep. 12, 2008, provisional application No. 61/109,317, filed on Oct. 29, 2008.

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257/E21.64

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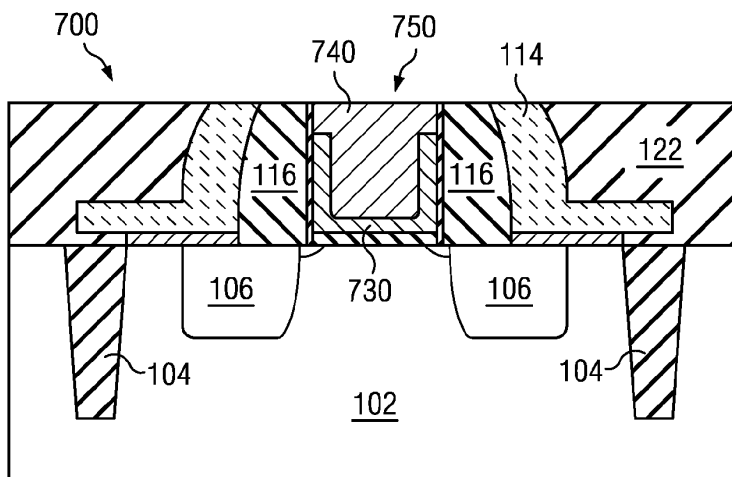
(58) **Field of Classification Search** ..... 438/703,  
438/757, 595, 785, 183; 216/108, 109;  
257/E21.626, E21.64, E21.593, E21.636,  
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(57) **ABSTRACT**

A method is provided for fabricating a semiconductor device. The method includes providing a substrate including a dummy gate structure formed thereon, removing the dummy gate structure to form a trench, forming a first metal layer over the substrate to fill a portion of the trench, forming a protection layer in a remaining portion of the trench, removing a unprotected portion of the first metal layer, removing the protection layer from the trench, and forming a second metal layer over the substrate to fill the trench.

See application file for complete search history.

**14 Claims, 7 Drawing Sheets**



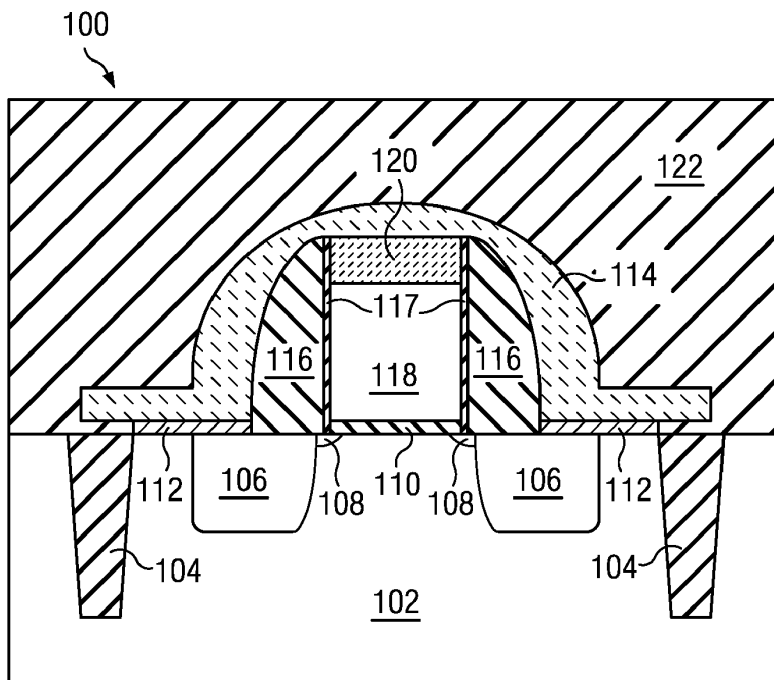


Fig. 1

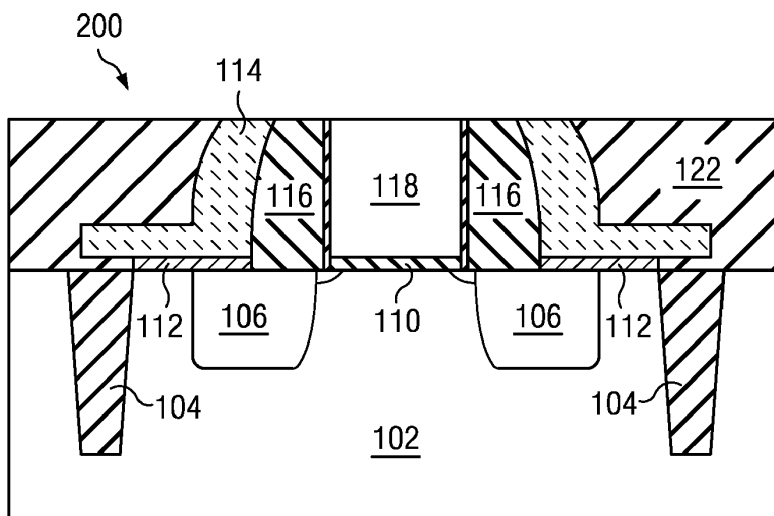


Fig. 2

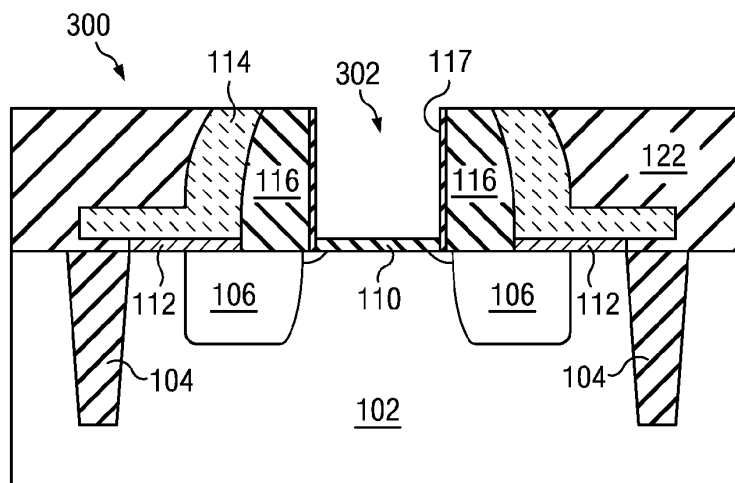


Fig. 3

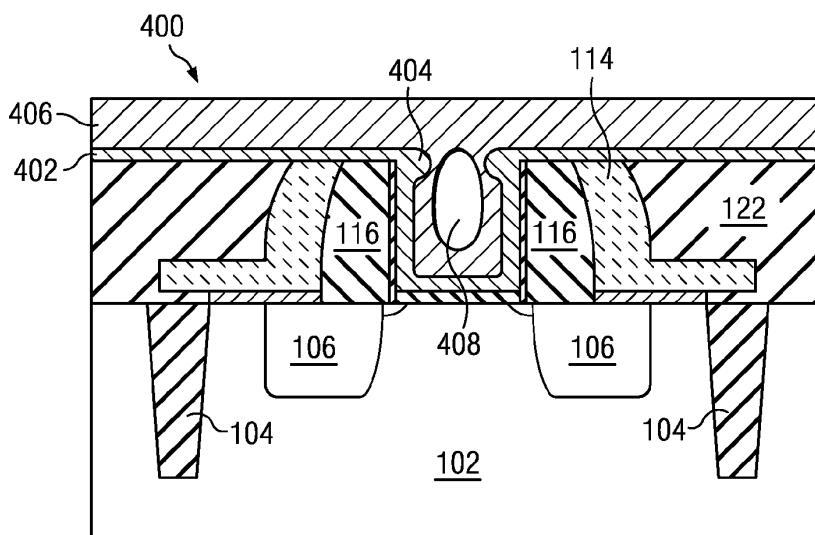


Fig. 4

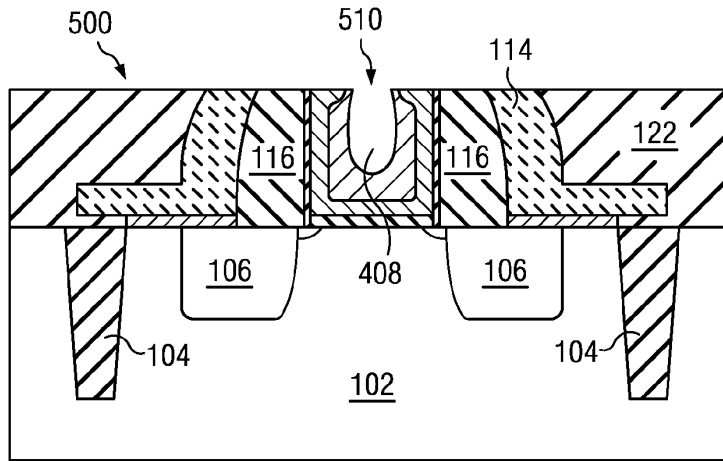


Fig. 5

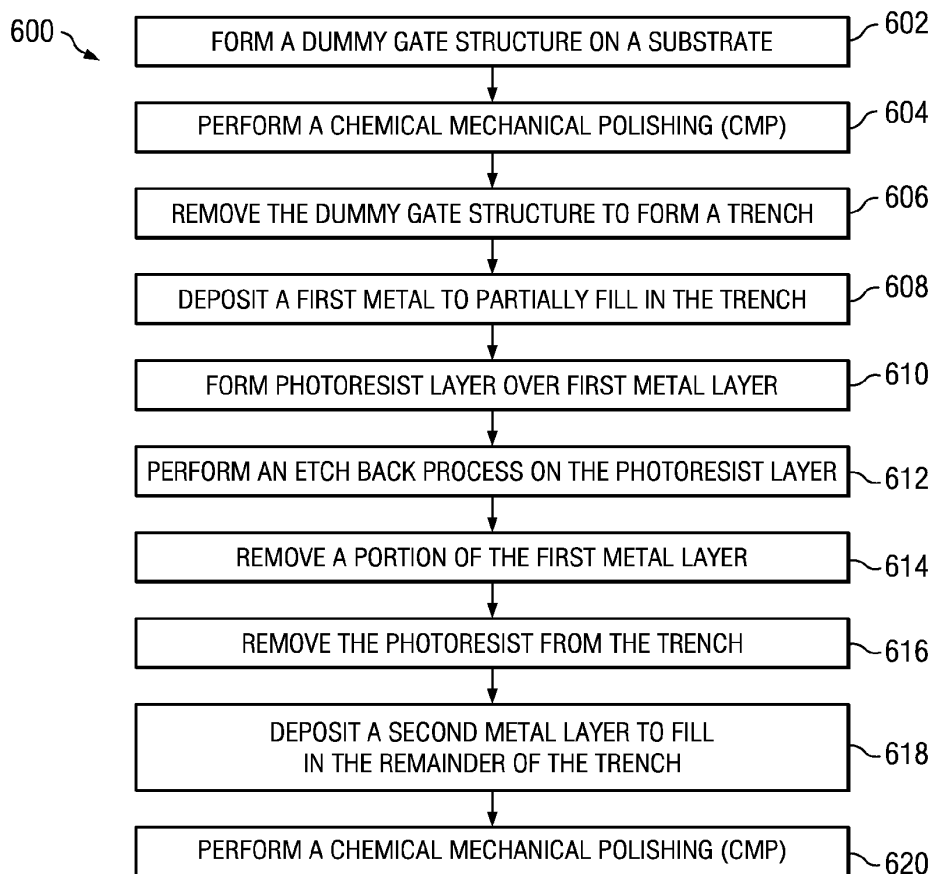


Fig. 6

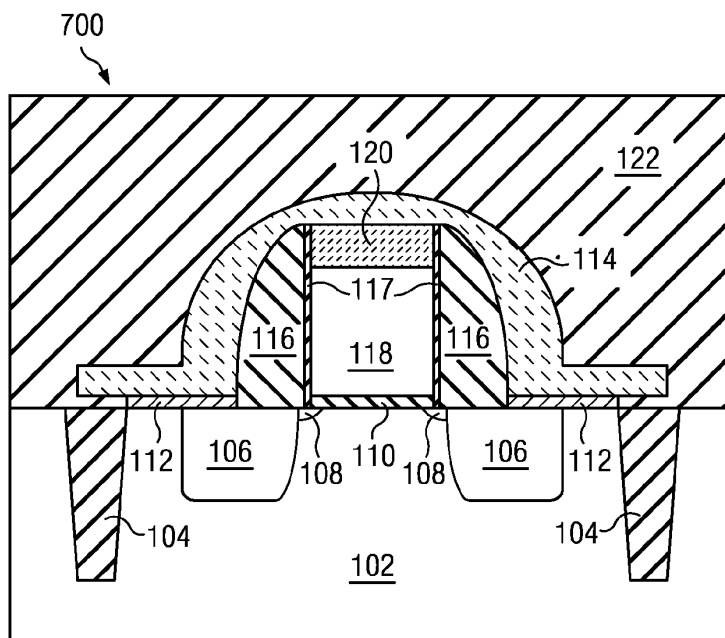


Fig. 7

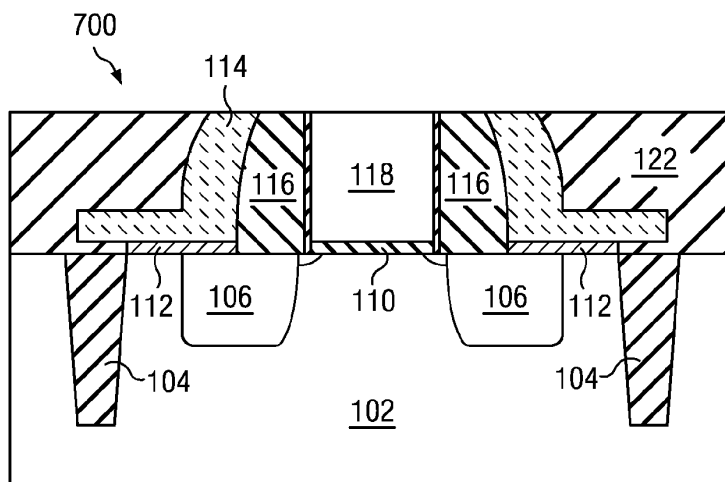


Fig. 8

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