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Paper No. 59
Filed: November 30, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
Petitioner,

v.

RAYTHEON COMPANY,
Patent Owner.

Case IPR2015-01201
Patent 5,591,678

Before JO-ANNE M. KOKOSKI, JENNIFER MEYER CHAGNON, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

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I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–18 of U.S. Patent No. 5,591,678 (Ex. 1001, “the ’678 patent”) are unpatentable.

A. Procedural History

Sony Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) for *inter partes* review of claims 1–18 (“the challenged claims”) of the ’678 patent. Petitioner included a Declaration of Dr. Richard A. Blanchard (Ex. 1002) to support its positions. Raytheon Company (“Patent Owner”) timely filed a Preliminary Response (Paper 5, “Prelim. Resp.”).

Pursuant to 35 U.S.C. § 314(a), on December 2, 2015, we instituted an *inter partes* review of the challenged claims to determine whether claims 1, 6, 7, 10, and 11 are unpatentable under 35 U.S.C. § 102 as anticipated by Bertin;¹ whether claims 5, 12, and 13 are unpatentable under 35 U.S.C. § 103 as obvious in view of Bertin and Morimoto;² whether claim 9 is unpatentable under 35 U.S.C. § 103 as obvious in view of Bertin and Ying;³ whether claims 1, 2, 4, 5, 10, 13, 14, 16, and 17 are unpatentable under 35 U.S.C. § 103 as obvious in view of Morimoto; whether claims 8 and 18

¹ U.S. Patent No. 5,202,754, issued Apr. 13, 1993 (Ex. 1017).

² JP App. Pub. No. 64-18248, published Jan. 23, 1989. Morimoto is a Japanese-language reference (Ex. 1005). Citations to Morimoto herein are to the certified English translation submitted by Petitioner (Ex. 1006).

³ U.S. Patent No. 3,864,819, issued Feb. 11, 1975 (Ex. 1016).

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are unpatentable under 35 U.S.C. § 103 as obvious in view of Morimoto and Oldham;⁴ and whether claims 3 and 15 are unpatentable under 35 U.S.C. § 103 as obvious in view of Morimoto and Bertin. Paper 6 (“Inst. Dec.”).

Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 23, Paper 22 (redacted version), “PO Resp.”), along with a Declaration of Dr. Eugene A. Fitzgerald (Ex. 2019⁵) to support its patentability positions. Petitioner filed a Reply (Paper 50, Paper 49 (redacted version), “Pet. Reply”) to the Patent Owner’s Response. An oral hearing was held on October 13, 2016. A transcript of the hearing is included in the record. Paper 58 (“Tr.”).

B. Related Proceedings

The ’678 patent has been asserted in *Raytheon Co. v. Samsung Electronics Co.*, No. 2:15-cv-00341 (E.D. Tex.), and *Raytheon Co. v. Sony Kabushiki Kaisha*, No. 2:15-cv-00342 (E.D. Tex.). Paper 3, 2; Pet. 1. The ’678 patent also has been challenged in *Sony Corp. v. Raytheon Co.*, Case IPR2016-00209 and *Samsung Electronics, Co. v. Raytheon Co.*, Case IPR2016-00739.

C. The ’678 Patent

The ’678 patent, titled “Process of Manufacturing a Microelectric Device Using a Removable Support Substrate and Etch-Stop,” relates to a method of fabricating a microelectronic device, in which the microelectronic

⁴ U.S. Patent No. 4,681,718, issued July 21, 1987 (Ex. 1014).

⁵ Pursuant to our authorization (Paper 39), Patent Owner also filed a Supplemental Declaration of Dr. Fitzgerald (Ex. 2019S).

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device is moved from one support to another during fabrication. Ex. 1001, 1:12–13. According to the '678 patent, “[t]he invention permits microelectronic devices to be prepared using well-established, inexpensive thin-film deposition, etching, and patterning techniques, and then to be further processed singly or in combination with other such devices, into more complex devices.” *Id.* at 2:9–14. Figure 1 of the '678 patent is reproduced below.

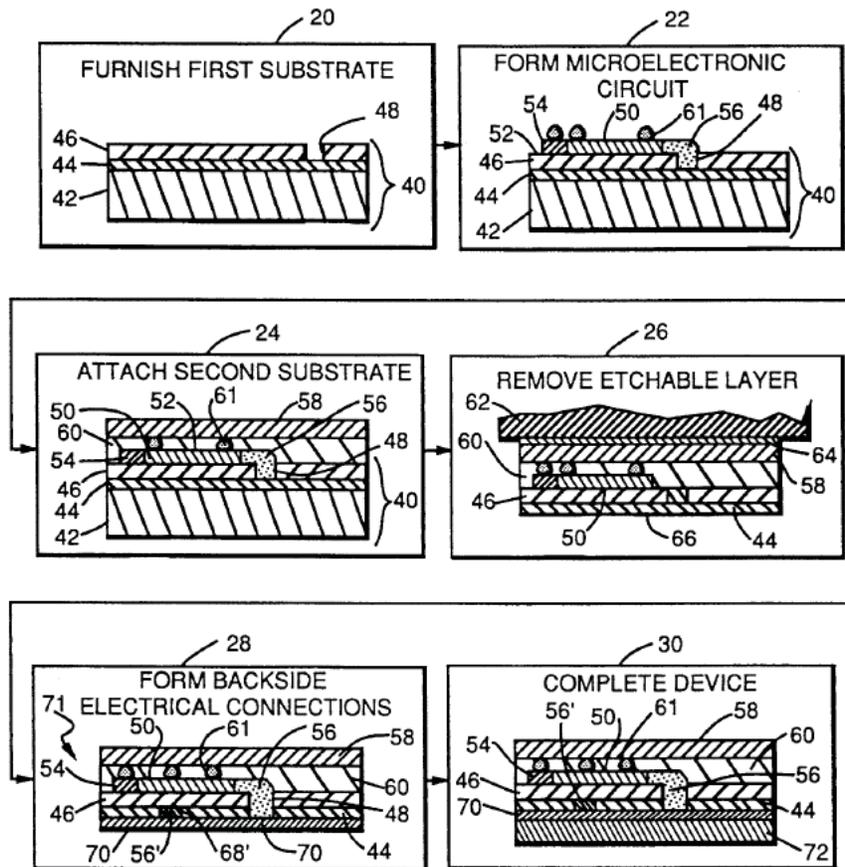


FIG. 1.

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Figure 1 is a process flow diagram of the method of the '678 patent, schematically illustrating each stage of fabrication of a microelectronic device formed in accordance with the method. *Id.* at 3:48–50. As shown in box 20, first substrate 40 is provided, the first substrate including etchable layer 42, etch-stop layer 44, and wafer layer 46. *Id.* at 3:65–4:2. As noted in the '678 patent, “[s]uch substrates can be purchased commercially,” or “prepared by applying well-known microelectronic techniques.” *Id.* at 4:2, 4:22–23. In a preferred embodiment, etchable layer 42 is a layer of bulk silicon, etch-stop layer 44 is a layer of silicon dioxide, and wafer layer 46 is a layer of single crystal silicon. *Id.* at 4:3–15.

Microelectronic circuit element 50 is formed in wafer layer 46, as shown in box 22. *Id.* at 4:37–52. The '678 patent notes that “the present invention is not limited to any particular circuit element 50,” and, for example, “can include many active devices such as transistors,” or “may be simply a patterned electrical conductor layer that is used as an interconnect between other layers of structure in a stacked three-dimensional device.” *Id.* at 4:55–56, 4:47–51.

Second substrate 58 is attached to the structure, as shown in box 24. *Id.* at 5:14–44. Second substrate 58 may comprise, for example, silicon or aluminum oxide, and optionally may include a microelectronic device deposited therein. *Id.* at 5:18–25. Etchable layer 42 is removed by etching, as shown in box 26. *Id.* at 5:45–6:9. The entire structure may be attached temporarily to base 62, which may be a piece of aluminum oxide (particularly, sapphire), to protect the structure against etch attack. *Id.* at

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