UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SONY CORPORATION
Petitioner

v.

RAYTHEON COMPANY,

Patent Owner

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**Case: IPR2015-01201**

**Patent 5,591,678**

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# SUPPLEMENTAL DECLARATION OF EUGENE A. FITZGERALD

I, Dr. Eugene A. Fitzgerald, hereby declare, affirm and state the following:

1. I submit this declaration setting forth page cites for three text books referenced in my prior declaration (Ex. 2019S), relating to issues under consideration in the U.S. Patent and Trademark Office concerning the *Inter Partes* Review of Patent No. 5,591,678. These three text books were cited to support my discussion on the background of integrated circuit manufacture, including three-dimensional integration of circuits and processes used across silicon wafers.

2. Footnote 3 in my prior declaration (Ex. 2019) cited "VLSI Technology," S.M. Sze, McGraw-Hill, New York (1983). (Ex. 2022.) My discussion on the background of integrated circuit manufacturing, including Moore's Law and advanced packaging techniques, and accompanying analysis, specifically relies upon pages 9, 51, 93, 131, 169, 219, 303, 347, and 445 of this reference. These pages have been included as part of an updated Ex. 2022R, submitted herewith.

3. Foonote 6 in my prior declaration (Ex. 2019) cited "3-D Integration for VLSI Systems", C.S. Tan, K.N. Chen, S.J. Koester, Pan Stanford Publishing (2012) ("Tan"). (Ex. 2025.) My discussion on the background of integrated circuit manufacturing, including advanced packaging techniques, and accompanying

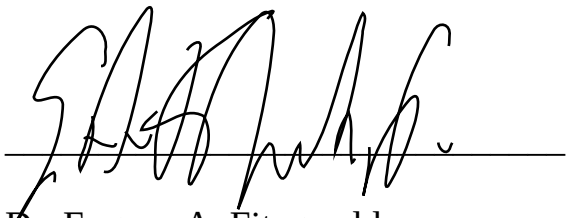
analysis, specifically relies upon pages 1-26 of this reference. These pages have been included as an updated Ex. 2025R, submitted herewith.

4. Footnote 7 in my prior declaration (Ex. 2019) cited "Silicon VLSI Technology", J.D. Plummer, M.D. Deal, P.B. Griffin, Prentice-Hall, NJ (2000) ("Plummer"); "Silicon Processing", D.C. Gupta, ASTM Special Technical Publication 804, Philadelphia (1983) ("Gupta"). (Ex. 2026.) My discussion on the background of integrated circuit manufacturing, including microelectronic processes, and accompanying analysis, specifically relies upon pages 49-92 of Plummer and pages 5-23 of Gupta. These pages have been included as updated Exs. 2026R and 2027R, submitted herewith.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of these proceedings.

I declare under the penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Date: May 17, 2016



Dr. Eugene A. Fitzgerald